Reference Manual

DOC. REV. 12/14/2007

VSBC-6

Pentium / K6-2 based SBC with Ethernet, Video, and Industrial I/O

VERSALOGIC CORPORATION

VSBC-6

Pentium / K6-2 based SBC with
Ethernet, Video, and
Industrial I/O

Product Release Notes

This page includes recent changes or improvements that have been made to this product. These changes may affect its operation or physical installation in your application. Please read the following information.

Rev 6 Release

- **BIOS**. Shipped with BIOS version 4.1.118 and later. See the VSBC-6 support web page for current BIOS release information.

Rev 5 Release

- **BIOS**. Shipped with BIOS version 4.1.115 and later. See the VSBC-6 support web page for current BIOS release information.
- **CPU.** Designed to support the Intel Tillamook chip.

Rev 4 Release

- **BIOS**. Shipped with BIOS version 4.1.107 and later. See the VSBC-6 support web page for current BIOS release information.
- **System RAM.** supports 3.3 volt SDRAM modules (PC-66 and PC-100) and EDO RAM modules.
- **CPU Fan Power Connector.** Connector J13 has been changed to a polarized style and has been moved to a better location.

Rev 3 Release

- **BIOS**. Shipped with BIOS version 4.1.103 and later. BIOS version 4.1.103 solved a Windows NT 4.0 boot problem.
- **System RAM.** Requires 3.3 volt EDO RAM modules. SDRAM is not supported in this release. System will beep continuously if powered up with SDRAM in place.
- **Power Connector.** Connector J4 was changed to a straight (vertical) connector on Rev. 3 boards. This configuration will be maintained on future versions.
- **IDE Interface.** Designed to support newer high speed IDE Type 4 and Ultra DMA drives. Not fully compatible with IDE Type 0-3 drives. See VSBC-6 support web page for additional information.

Rev 2 Release

- **BIOS**. Shipped with BIOS version 4.1.100 and later.
- **System RAM.** Requires 3.3 volt EDO RAM modules. SDRAM is not supported in this release. System will beep continuously if it is powered up with SDRAM in place.

Rev 1 Release

- Pre-production only. No customer releases.

Support Page

The **VSBC-6 Support Page**, at **http://www.versalogic.com/private/vsbc6support.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for VSBC-6 users only. It cannot be reached through our web site. You must enter this address directly to find the support page.

Model VSBC-6

Pentium / K6-2 based SBC with Ethernet, Video, and Industrial I/O

REFERENCE MANUAL

Doc. Rev. 12/10/2007

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Table of Contents

Introduction 1

Description

The VSBC-6 is a feature-packed single board computer designed for OEM control projects requiring fast processing, industrial I/O, flexible memory options, and designed-in reliability and longevity (product lifespan). It's features include:

- MMX-class processors
  - Intel Pentium MMX CPUs
  - AMD K6-2 CPUs
- 8 to 256 MB system RAM
- 256 KB level 2 cache - Rev 4
- 512 KB level 2 cache - Rev 5
- 32-Pin DiskOnChip site
- 10BaseT Ethernet interface
- PCI based video
- Flat Panel Display support
- PC/104-Plus expansion site
- Dual PCI based IDE controllers
- Dual USB 1.0 interfaces
- 4 COM + 1 LPT port
- Keyboard and PS/2 mouse port
- Industrial I/O
  - Analog input option
  - 16 channel Opto 22 compatible
  - Three spare 16-bit counter/timers
- Two RS-232/422/485 selectable ports
- Watchdog timer
- Vcc sensing reset circuit
- EBX Compliant. 5.75” x 8.00” footprint
- UL and CE compliant
- Flash BIOS with OEM enhancements
- Latching I/O connectors
- Customizing available

This Super Socket 7 compliant single board computer will accept Intel Pentium MMX, AMD K6-2 CPU chips. Processing speeds up to 400 MHz are currently available. The board is compatible with popular operating systems such as Windows CE, QNX, Windows NT/95/98, and VxWorks.

A full complement of standard I/O ports is included on the board. Additional I/O expansion is available through the high speed PCI-based PC/104-*Plus* expansion site (which supports both PC/104 and PC/104-*Plus* expansion modules).

System memory expansion is supported with a high-reliability latching 168-pin DIMM socket. Low power 3.3V 168-pin DIMM modules up to 256 MB are available. EDO and SDRAM modules (PC-66 and PC-100) are accepted (see specifications on page 3). Application programs and files can be stored on an optional bootable DiskOnChip (DOC) device. Up to 144 MB of plug-in DOC memory is supported.

The VSBC-6 features high reliability design and construction including latching I/O connectors. It also features a watchdog timer, voltage sensing reset circuits, and self-resetting fuse on the 5V supply to the keyboard, mouse, USB 1.0 and Opto 22 I/O ports.

VSBC-6 boards are subjected to a 48-hour burn-in and 100% functional testing and are backed by a limited two-year warranty.

US-based manufacturing, careful parts sourcing, and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional SBC.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 5.75" x 8.00" x 1.75"; EBX Compliant
Storage Temperature: –40° C to 85° C
Free Air Operating Temperature:
0° C to +60° C (free air, CPU fan with heatsink attached and operating)
0° C to +60° C (free air, CPU fanless version "h" operating)
Power Requirements: *(with 32 MB EDO DRAM, keyboard, and mouse)*
VSBC-6bx 266 MHz K6 CPU 5V ±5% @ 3.7 A (18.3 W) typ.
VSBC-6cx 233 MHz Pentium CPU 5V ±5% @ 3.9 A (19.5 W) typ.
VSBC-6gx 400 MHz K6-2 CPU 5V ±5% @ 4.8 A (24.0 W) typ.
VSBC-6hx 266 MHz K6-2E CPU 5V ±5% @ 3.0 A (15.0 W) typ.
VSBC-6ht 266 MHz K6-2E CPU with fan 5V ±5% @ 3.1A (15.5 W) typ.
VSBC-6sx 266 MHz Tillamook CPU 5V ±5% @ 2.3 A (11.4 W) typ
VSBC-6tp 266 MHz Tillamook CPU with fan 5V ±5% @ 2.4 A (11.9 W) typ
+3.3V or ±12V may be required by some expansion modules
System Reset:
V_{CC} sensing, resets below 4.37V typ. Watchdog timeout
DRAM Interface:
One 168-pin DIMM socket.
8 to 256 MB, 3.3 volt, parity or non-parity, EDO, ECC or non-ECC (all VSBC-6 versions)
8 to 256 MB, 3.3 volt, parity or non-parity, EDO or SDRAM, ECC or non-ECC (VSBC-6 rev 4.00 or later)
Note: Parity and ECC features are not supported by the BIOS.
Flash / BBSRAM Interface:
One 32-pin DIP socket. Accepts a 2 to 144 MB DiskOnChip device or 512 KB battery-backed static RAM chip
Video Interface:
Based on C&T 65550 chip. 2 MB VRAM standard. Resolutions to 1280 x 1024.
Optional flat panel display interface
IDE Interface:
Two channels, standard 40-pin IDE, compatible with enhanced IDE mode 4 and Ultra DMA
Supports up to four IDE devices (hard drives, CD-ROM, etc.)
Floppy Disk Interface:
One 34-pin connector, supports two floppy drives
Ethernet Interface:
10BaseT based on SMSC LAN91C96 chip. On-board RJ-45 Ethernet cable connector. Optional AUI interface
Analog Input:
8-channel, 12-bit, single-ended, 6 microsecond, channel independent input ranges:
±5, ±10, 0 to +5V, 0 to +10V. **Note:** Analog input is available only on -r versions.
COM1–2 Interface:
RS-232, 16C550 compatible, 115K baud max.
COM3–4 Interface:
RS-232/422/485, 16C550 compatible, 460K baud max.
LPT Interface:
Bi-directional/EPP/ECP compatible
Opto 22 / Digital Interface:
16 channel, full compliance, ±24 ma outputs
BIOS: General Software embedded BIOS with OEM enhancements
Field upgradable with Flash BIOS Upgrade Utility
Bus Speed:

CPU External:	66 MHz
PCI, PC/104-*Plus*:	33 MHz
PC/104:	8 MHz

Compatibility:
PC/104 – Full compliance
Embedded-PCI (PC/104-*Plus*) – Full compliance, 3.3V or 5V modules

Specifications are subject to change without notice.

Technical Support

If you have problems that this manual can't help you solve, first visit the VSBC-6 Product Support web page at **http://www.versalogic.com/private/vsbc6support.asp**. If you have further questions, contact VersaLogic for technical support at (541) 485-8575. You can also reach our technical support engineers via e-mail at support@versalogic.com.

VSBC-6 Support Website

http://www.versalogic.com/private/vsbc6support.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company, and your phone number
- The name of a technician or engineer who we can contact if we have questions
- Quantity of items being returned
- The model and serial number (bar code) of each item
- A description of the problem
- Steps you have taken to resolve or repeat the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. We will need to know what shipping method you prefer for return back to your facility, and we will need to secure a purchase order number for invoicing the repair.

Note! Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

Configuration / Operation 2

Overview

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage boards, disk drives, and other components. The circuit board must be only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an anti-static foam pad if available.

The board should also be protected during shipment or storage by keeping inside a closed metallic anti-static envelope.

Note! The exterior coating on some metallic anti-static bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the VSBC-6.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

MOUNTING SUPPORT

Warning! The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

Initial Configuration and Setup

The following list describes the recommended components and gives an abbreviated outline for setting up a typical development system.

RECOMMENDED COMPONENTS

- VSBC-6 Single Board Computer
- 168-pin DIMM SDRAM Memory Module (PC-66 or PC-100) (VSBC-6 rev 4.00 or later)
- 168-pin DIMM EDO Memory Module (VSBC-6 Rev 2 or 3)
- ATX Power Supply
- SVGA Video Monitor
- Keyboard with PS2 connector
- 3.5" Floppy Disk Drive (optional)
- IDE Hard Drive (optional)
- IDE CD ROM Drive (optional)

DRAM MODULE

- Insert DRAM module into the DIMM socket. Latch into place.

CABLES / PERIPHERAL DEVICES

- Plug video adapter cable (p/n VL-CBL-1601) into socket J11 and attach video monitor.
- Plug keyboard adapter cable (p/n VL-CBL-1602) into socket J7 and attach keyboard.
- Plug floppy data cable (p/n VL-CBL-3403) into socket J18 and attach floppy drive. ***Note!*** Floppy drive should be connected after the twist in the cable.
- Plug hard drive data cable (p/n VL-CBL-4001) into socket J17. Attach hard drive and CD ROM drive to the connectors at the opposite end of the cable.
- Plug power supply into J4.
- Attach power supply cables to external drives.
- Jumper hard drive to operate as a master device.

CMOS Setup / Boot Procedure

- Turn power on.
- Press the DEL key the instant that video is displayed (during the memory test).
- Verify correct CMOS Setup information (see table below)
- Insert bootable floppy disk into floppy drive or allow the system to boot from the hard drive.

Basic CMOS Configuration

```
+---------------------------------------------------------------------------+
|                 System Bios Setup - Basic CMOS Configuration              |
|           (C) 2000 General Software, Inc. All rights reserved             |
+--------------------------+--------------------+-----------------------+
| DRIVE ASSIGNMENT ORDER:  | Date:>Jan 01, 1980 | Typematic Delay  : 250 ms  |
| Drive A: Floppy 0        | Time: 00 : 00 : 00 | Typematic Rate   : 30 cps  |
| Drive B: (None)          | NumLock:  Disabled | Seek at Boot     : None    |
| Drive C: (None)          +--------------------+ Show "Hit Del"   : Enabled |
| Drive D: (None)          | BOOT ORDER:        | Config Box       : Enabled |
| Drive E: (None)          | Boot 1st: Drive A: | F1 Error Wait    : Enabled |
| Drive F: (None)          | Boot 2nd: (None)   | Parity Checking  : (Unused)|
| Drive G: (None)          | Boot 3rd: (None)   | Memory Test Tick : Enabled |
| Drive H: (None)          | Boot 4th: (None)   | Test Above 1 MB  : Disabled|
| Drive I: (None)          | Boot 5th: (None)   | Debug Breakpoints: (Unused)|
| Drive J: (None)          | Boot 6th: (None)   | Splash Screen    : Disabled|
| Drive K: (None)          +--------------------+-----------------+-----------+
| (Loader): (Unused)       | IDE DRIVE GEOMETRY:  Sect  Hds  Cyls | Memory    |
+--------------------------+ Ide 0: Not installed                 |  Base:    |
| FLOPPY DRIVE TYPES:      | Ide 1: Not installed                 |   640KB   |
| Floppy 0: 1.44 MB, 3.5"  | Ide 2: Not installed                 |  Ext:     |
| Floppy 1: Not installed  | Ide 3: Not installed                 |   15MB    |
+--------------------------+--------------------------------------+-----------+
Custom Configuration
+---------------------------------------------------------------------------+
|                System BIOS Setup - Custom Configuration                   |
|           (C) 2000 General Software, Inc. All rights reserved             |
+-----------------------------------+---------------------------------------+
| COM1 (03F8)               : Enabled   | COM3 (03E8) Enable/IRQ    : IRQ4    |
| COM2 (02F8)               : Enabled   | COM4 (02E8) Enable/IRQ    : IRQ3    |
| Parallel Port Mode        : SPP       | LPT1 (0378) Enable/IRQ    : IRQ7    |
| Ethernet Enable/Base      : 340h      | Ethernet IRQ (if enabled) : IRQ11   |
| Cache (L1 and L2)         : Enabled   | PCI INTA                  : IRQ10   |
| Interrupt Vector Restore  : Disabled  | PCI INTB                  : IRQ10   |
| I/O Register Base Address : 0E0h      | PCI INTC                  : IRQ10   |
| 64KB Memory Page at E000  : None      | PCI INTD                  : IRQ10   |
| Reserved                  : (Unused)  | USB Controller Enable/INT : Disabled|
| IDE 0 PIO Mode            : Auto      | IDE 2 PIO Mode            : Auto    |
| IDE 1 PIO Mode            : Auto      | IDE 3 PIO Mode            : Auto    |
|                                       |                                     |
|                                       |                                     |
+---------------------------------------+-------------------------------------+
Shadow Configuration
+---------------------------------------------------------------------------+
|                System BIOS Setup - Shadow/Cache Configuration             |
|           (C) 2000 General Software, Inc. All rights reserved             |
+-----------------------------------+---------------------------------------+
| Shadowing                 : >Chipset  | Shadow 16KB ROM at C000   : Disabled|
| Shadow 16KB ROM at C400   : Disabled  | Shadow 16KB ROM at C800   : Disabled|
| Shadow 16KB ROM at CC00   : Disabled  | Shadow 16KB ROM at D000   : Disabled|
| Shadow 16KB ROM at D400   : Disabled  | Shadow 16KB ROM at D800   : Disabled|
| Shadow 16KB ROM at DC00   : Disabled  | Shadow 16KB ROM at E000   : Disabled|
| Shadow 16KB ROM at E400   : Disabled  | Shadow 16KB ROM at E800   : Disabled|
| Shadow 16KB ROM at EC00   : Disabled  | Shadow 64KB ROM at F000   : Enabled |
+-----------------------------------+---------------------------------------+
```

Note! Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above.

Windows 95 Installation

Because of the industrial nature of the VSBC-6, a "Custom" installation of Windows 95 is recommended. Addition of ethernet and video drivers are accomplished after the operating system is fully installed.

Note! If the "custom" option is not used, the installation program will hang at the 30% and 35% points in the automatic hardware detection phase. The installation can be completed this way, however, it requires more time since a system restart is required after each of the two detection errors.

INSTALLATION OF WIN95 OPERATING SYSTEM

1. Configure a VSBC-6 with attached floppy drive, hard drive, and CD-ROM drive. Make sure no PC/104 expansion modules are installed.
2. Create a bootable copy of DOS on your hard drive. Include drivers so the CD-ROM drive can be accessed.
3. Run the setup program on the Win95 CD-ROM.
4. On the "Setup Options" dialog box, select the following:
   - ☐ Typical
   - ☐ Portable
   - ☐ Compact
   - ☒ Custom
5. On the "Analyzing Your Computer" dialog box, select the following:
   - ☐ Yes (recommended).
   - ☒ No, I want to modify the hardware list.

   Note: Steps 4 and 5 instruct the Win95 installation program to bypass the hardware detection phase.
6. On the second "Analyzing Your Computer" dialog box, you will be presented with a list of Hardware Types and Model selection options. Check and uncheck the various options as shown below:

   - ☒ CD-ROM Drive
   - ☒ Display
     - *Uncheck all models except:*
     - ☒ Chips & Technology Accelerated Display Adapter
     - ☒ Chips & Technology Super VGA Display Adapter
   - ☒ Floppy Disk Controllers
   - ☒ Hard Disk Controllers
     - *Uncheck:*
     - ☐ Plus Hardcard
   - ☒ Keyboard
   - ☒ Mouse
     - *Uncheck:*
     - ☐ Bus Mouse
     - ☐ Inport Mouse
   - ☐ Network Adapter
   - ☐ PCMCIA Socket
   - ☒ Ports
   - ☐ SCSI Controllers
   - ☐ Sound, MIDI, or Video Capture Cards
7. Bypass the "Network Configuration" dialog box by pressing NEXT.

INSTALLATION OF WIN95 ETHERNET DRIVERS

1. With Win95 running, insert *Ethernet Drivers* disk into the floppy drive.
2. Hold the ALT key down and right click on the "My Computer" icon. Note the version of Windows you are running. You will need this information for step #8.
3. Start|Run|A:\EXTRACT.BAT

   Note: This will copy files from the floppy disk to C:\VSBC-6\NET
4. Start|Settings|Control Panel|Add New Hardware
5. On the "Add New Hardware Wizard" dialog box, select the following:

   ☐ Yes (recommended).

   ☒ No
6. On the "Hardware Types" list, highlight **Network Adapters**
7. Click on the "Have Disk" button

8a. For Windows 95 version 4.00.950 or 4.00.950a

   Navigate to the *c:\vsbc-6\net\ndis3-4\ndis3\lan-only* directory

8b. For Windows 95 version 4.00.950b

   Navigate to the *c:\vsbc-6\net\ndis3-4\ndis4\lan-only* directory

9. On the "Select Device" dialog box, highlight **SMC 9000 Ethernet Adapter**
10. Enter your computer and network identification information, including adding appropriate network protocols and/or services, TCP/IP information, etc.
11. Select "Configuration" tab and highlight **SMC 9000 Ethernet Adapter**
12. Press the "Properties" button.
13. Select "Resources" tab.
14. Change the address and IRQ to the following:

    I/O address range = 340 – 35F

    Interrupt (IRQ) = 11

Windows 98 Installation

Because of the industrial nature of the VSBC-6, a "Custom" installation of Windows 98 is recommended. Addition of ethernet and video drivers are accomplished after the operating system is fully installed.

INSTALLATION OF WIN98 OPERATING SYSTEM

1. Start out with a VSBC-6 with attached floppy drive, hard drive, and CD-ROM drive. Make sure no PC/104 expansion modules are installed.
2. Install DOS on your hard drive. Include drivers so your CD-ROM can be accessed.
3. Run the setup program on the Win98 CD-ROM.
4. On the "Setup Options" dialog box, select the following:
   - ☐ Typical
   - ☐ Portable
   - ☐ Compact
   - ☒ Custom
5. Wait for installation process to complete.

INSTALLATION OF WIN98 ETHERNET DRIVERS

1. With Win98 running, insert *Ethernet Drivers* disk into the floppy drive.
2. Start|Run|A:\EXTRACT.BAT

   Note: This will copy files from the floppy disk to C:\VSBC-6\NET
3. Start|Settings|Control Panel|Add New Hardware
4. On the "Add New Hardware Wizard" dialog box, select the following:
   - ☐ Yes (recommended).
   - ☒ No, I want to select hardware from the list
5. On the "Hardware Types" list, highlight **Network Adapters**
6. Click on the "Have Disk" button
7. Navigate to the *c:\vsbc-6\net\ndis3-4\ndis4\lan-only* directory
8. Highlight NET9000.INF. Click "OK".
9. On the "Select Device" dialog box, highlight **LAN9000 Ethernet Adapter (ISA)**
10. Drivers will load from the Win98 CD-ROM
11. At the 99% mark, the system will stop because it cannot find a file. Press the down arrow in the "Copy File From" list box. Select *c:\vsbc-6\net\ndis3-4\ndis4\lan-only*. Press OK.
12. After reboot you will get an error message stating that LAN9000 is not setup properly. IGNORE THIS ERROR MESSAGE.
13. Start|Settings|Control Panel|Network
14. Select "Configuration" tab and highlight **LAN9000 Ethernet Adapter (ISA)**
15. Press the "Properties" button.
16. Select "Resources" tab.
17. Change the address and IRQ to the following:

    I/O address range = 340 – 35F
    Interrupt (IRQ) = 11
18. Enter your computer and network identification information, including adding appropriate network protocols and/or services, TCP/IP information, etc.

DOS Installation

No special installation instructions are necessary for installing DOS on a VSBC-6 system. You will use regular FDISK, FORMAT, and SYS procedures which are common to all DOS installations.

INSTALLATION OF DOS ETHERNET DRIVERS

1. With DOS running, insert the *Ethernet Drivers* disk into the floppy drive.
2. Execute A:\>EXTRACT.BAT

   Note: This will copy files from the floppy disk to C:\VSBC-6\NET

3. After installation, Ethernet packet drivers for DOS, and a PROTOCOL.INI file can be found in the following directory:

   c:\vsbc-6\net\ndis2\mslanman.dos\drivers\ethernet\smc9000

SETUP AND CONFIGURATION UTILITY

The "ISMC9000.EXE" utility can be used to change the default base address, IRQ settings, and other operational parameters of the ethernet interface:

c:\vsbc-6\net\utility/setup/ismc9000.exe

DEFAULT CONFIGURATION

The default hardware configuration works well for most DOS installations.

I/O Address = 0340
IRQ Number = 11
IRQ Line = 3

SAMPLE WINDOWS NT NETWORK ACCESS

The following files represent a minimal DOS based configuration for connecting the VSBC-6 to a Windows NT network running the NETBEUI protocol.

Note! The SYSTEM.INI file must be edited to include the computer name and workgroup name associated with your specific network environment.

Directory of A:

```
NET            <DIR>         01-01-80  5:06p NET
COMMAND  COM         54,645  05-31-94  6:22a COMMAND.COM
CONFIG   SYS             51  01-01-80  5:14p CONFIG.SYS
AUTOEXEC BAT             83  01-01-80  5:37p AUTOEXEC.BAT
```

DOS Installation (continued)

Directory of A:\NET

```
IFSHLP   SYS         4,644  05-26-95 10:57a IFSHLP.SYS
NET      MSG        76,234  05-26-95 10:57a NET.MSG
NETH     MSG       123,066  05-26-95 10:57a NETH.MSG
NET      EXE       450,342  05-26-95 10:57a NET.EXE
SHARES   PWL           622  01-01-80  5:21p SHARES.PWL
SYSTEM   INI           491  01-01-80  5:25p SYSTEM.INI
WFWSYS   CFG           840  05-26-95 10:57a WFWSYS.CFG
CONNECT  DAT             0  01-01-80  5:39p CONNECT.DAT
PROTMAN  EXE        13,782  05-26-95 10:57a PROTMAN.EXE
PROTMAN  DOS        21,940  05-26-95 10:57a PROTMAN.DOS
NDISHLP  SYS         4,468  05-26-95 10:57a NDISHLP.SYS
SMC9000  DOS        28,428  04-04-97  9:33a SMC9000.DOS
NRSETUP  EXE        33,655  08-06-93  1:00a NRSETUP.EXE
PROTOCOL INI           545  01-01-80  4:56p PROTOCOL.INI
```

A:\CONFIG.SYS

```
FILES=30
lastdrive = z
device=a:\net\ifshlp.sys
```

A:\AUTOEXEC.BAT

```
@ECHO OFF
PROMPT $p$g
PATH A:\;A:\NET
NET LOGON
NET USE I: \\SERVER\SHARE
```

A:\NET\PROTOCOL.INI

```
[network.setup]
version=0x3110
netcard=ms$ne2clone,1,MS$NE2CLONE,1
transport=ms$ndishlp,MS$NDISHLP
transport=ms$netbeui,MS$NETBEUI
lana0=ms$ne2clone,1,ms$netbeui
lana1=ms$ne2clone,1,ms$ndishlp

[ms$ne2clone]
DriverName = "SMC9X$"
INTERRUPT=11
IOBASE=0x340

[protman]
drivername=PROTMAN$
PRIORITY=MS$NDISHLP

[MS$NDISHLP]
drivername=ndishlp$
BINDINGS=ms$ne2clone
```

DOS Installation (continued)

A:\NET\PROTOCOL.INI (continued)

```
[ms$netbeui]
drivername=netbeui$
SESSIONS=10
NCBS=12
BINDINGS=ms$ne2clone
LANABASE=0
```

A:\NET\SYSTEM.INI

```
[network]
filesharing=no
printsharing=no
autologon=yes
computername=COMPNAME
lanroot=A:\NET
username=
password=
workgroup=NETNAME
reconnect=no
directhost=no
dospophotkey=N
lmlogon=0
logondomain=NETNAME
preferredredir=full
autostart=full
maxconnections=8

[network drivers]
netcard=smc9000.dos
transport=ndishlp.sys,*netbeui
devdir=A:\NET
LoadRMDrivers=yes

[Password Lists]
*Shares=A:\NET\Shares.PWL
```

Creating a Bootable DOS DiskOnChip

The DiskOnChip is shipped pre-formatted, non-bootable, without any files on it. The DiskOnChip will appear as Drive D in systems with an installed hard drive. If a hard drive is not installed, the DOC will appear as Drive C:

1. Boot your system under DOS or Windows (if using Windows, start a DOS session)
2. Type SYS C: (or SYS D: if appropriate)

Dimensions and Mounting

The VSBC-6 complies with all EBX standards which provide for specific mounting hole and PC/104-*Plus* stack locations as shown in the diagram below.

Caution The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

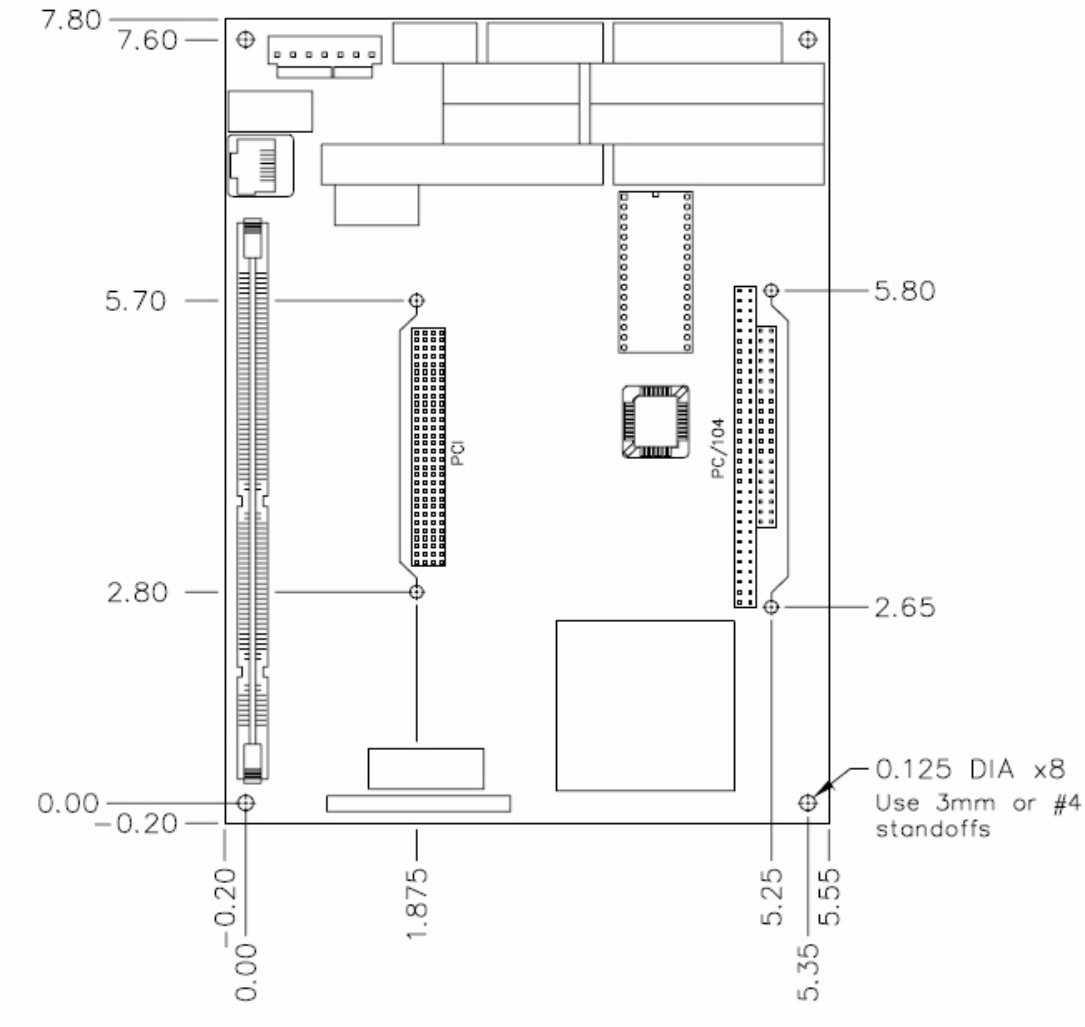


Figure 1. Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The VSBC mounts on four 4-40, 3/8" hardware standoffs using the corner mounting holes (A). These standoffs are secured to the underside of the circuit board using 1/4" 4-40 pan head screws.

Four additional 4-40, 3/8" standoffs (B) must be used under the circuit board to prevent excessive flexing when expansion modules are mated and demated. These are secured with four 4-40, 5/8" male-female standoffs (C) threaded from the topside which also serve as mounting struts for the PC/104 stack.

The entire assembly can sit on a table top or it can be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing. Refer to the drawing on page 15 for dimensional details.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack.

Note! Standoffs and screws for (A and B) are available as part number VL-HDW-104. Standoffs and screws for (C) are available as part number VL-HDW-100.

STANDOFF LOCATIONS

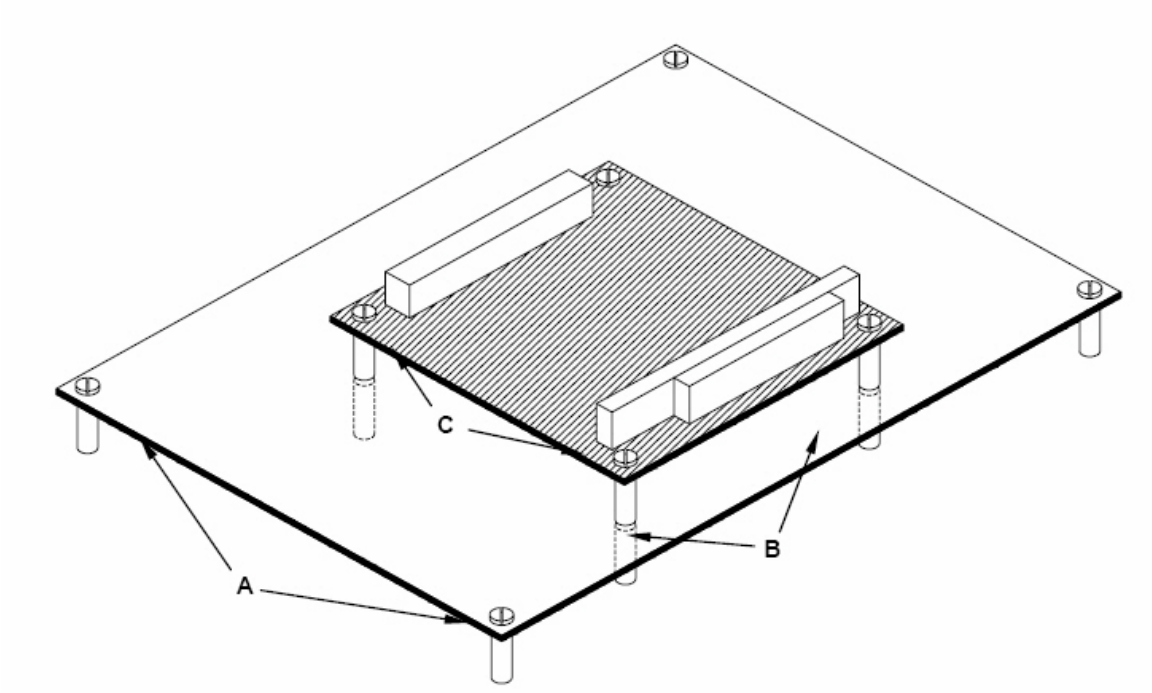


Figure 2. Standoff Locations

External Connectors

CONNECTOR LOCATION DIAGRAM

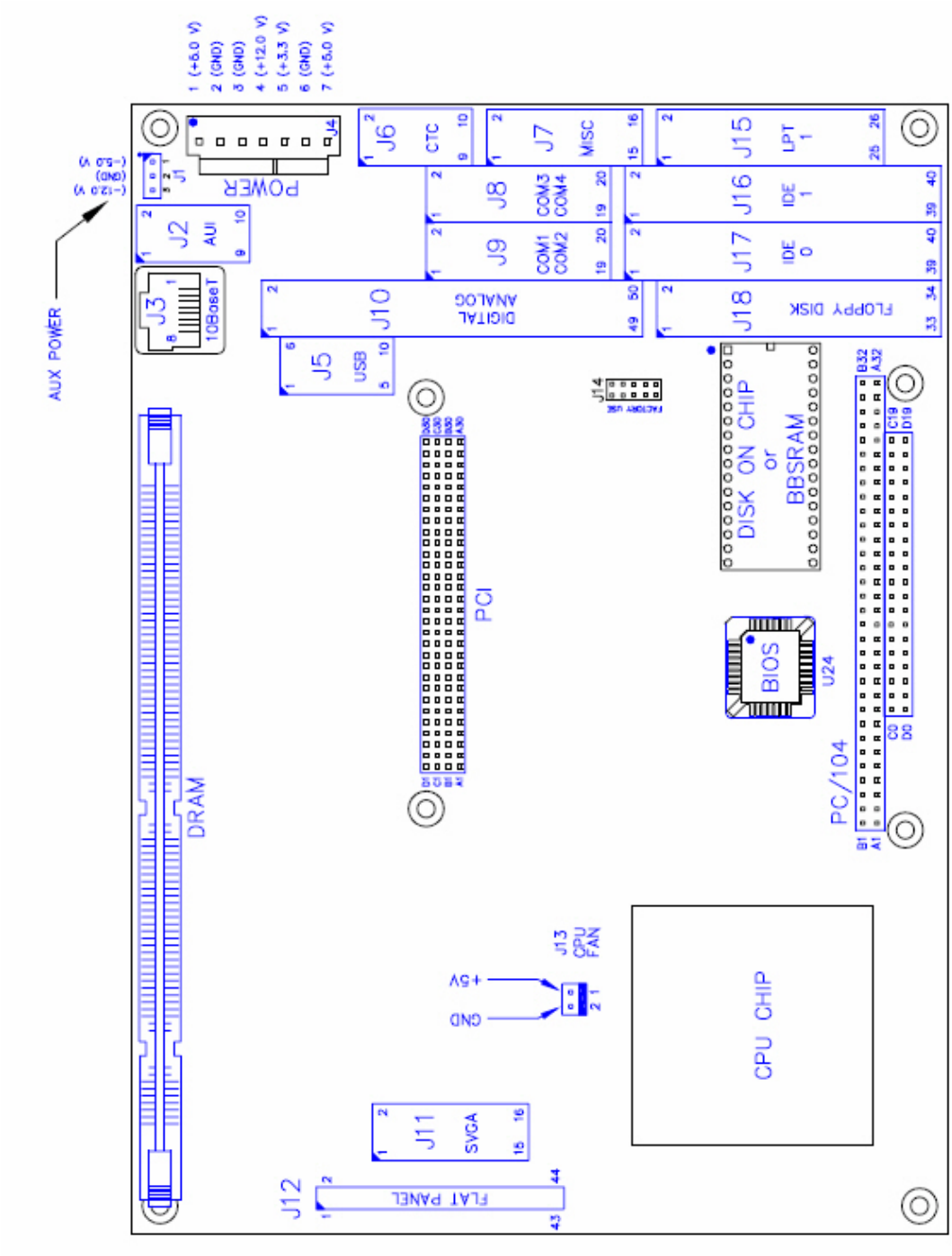


Figure 3. Connector Location Diagram

CONNECTOR FUNCTIONS AND INTERFACE CABLES

The table below notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page	‡Pin 1 Location X Coord.	‡Pin 1 Location Y Coord.
J1	PC/104-*Plus* Auxiliary Power (–5V & –12V)	Molex 22-01-2033 + Molex 08-50-0005 (3ea.)	See connector J4	See connector J4	23	–0.075	7.400
J2*	Ethernet AUI	3M 3473-7600	VersaLogic VL-CBL-1005	1 foot 10-pin socket to DB15F	39	0.025	6.890
J3	Ethernet 10BaseT	RJ-45 Crimp-on Plug	—	—	39	n/a	n/a
J4	Main Power Input (EBX Compliant)	Molex 09-50-8073 + Molex 08-52-0072 (7 ea.)	VersaLogic VL-CBL-2020	Interface from industry standard ATX power supply (to J1 and J4)	23	0.250	7.400
J5*	Dual USB 1.0 Connector	Molex 14-56-2051	VersaLogic VL-CBL-0501 (two required)	6 inch transition cable. 5 pin connector to USB 1.0 receptacle connector.	48	1.125	5.925
J6*	Counter / Timer Signals	3M 3473-7600	User supplied	—	51	1.625	7.525
J7*	Speaker, IDE LED, Programmable LED, Fused Vcc, Keyboard, Push-Button Reset	3M 3452-7600	VersaLogic VL-CBL-1602	1 foot breakout cable. 16-pin socket to two 6-PIN mini DIN panel mount, programmable LED and HD activity LED, speaker, and reset switch.	34	2.525	7.525
J8*	COM3 and COM4 Ports	3M 3421-7600	VersaLogic VL-CBL-2001	1 foot, 20-pin socket to two DB9M serial port connectors	31	2.000	7.125
J9*	COM1 and COM2 Ports	3M 3421-7600	VersaLogic VL-CBL-2001	1 foot, 20-pin socket to two DB9M serial port connectors	31	2.000	6.725
J10*	Opto-22 Interface and Analog Input (-r version)	3M 3425-7600	VersaLogic VL-CBL-5007	1.5 foot, 50-pin socket to 34-pin socket and 16-pin socket	49, 41	0.800	6.325
J11*	SVGA Video Output	3M 3452-7600	VersaLogic VL-CBL-1601	1 foot 16-pin socket to 15-pin D-sub SVGA connector	36	1.675	0.225
J12	Flat Panel Interface	Adam Tech 2FCS-44-SG + Adam Tech 2CTA §	Custom	Contact Factory	37	1.125	–0.100
J13	Fan Power Output (+5V)	Molex 22-01-3027 or Molex 22-01-2025	Provided with fan assembly	—	26	2.835	1.465
J14	PLD Reprogramming Port *(Factory use Only)*	—	—	—	—	3.300	5.800
J15*	LPT1 Port	3M 3399-7600	VersaLogic VL-CBL-2601	1 foot 26-pin socket to DB-25F connector	32	3.725	7.525
J16*	IDE Hard Drive Channel 1	3M 3417-7600	VersaLogic VL-CBL-4001	1.5 foot 40-pin dual IDE drive interface cable	33	3.400	7.125
J17*	IDE Hard Drive Channel 0	3M 3417-7600	VersaLogic VL-CBL-4001	1.5 foot 40-pin dual IDE drive interface cable	33	3.400	6.725
J18*	Floppy Drive Interface	3M 3417-7600	VersaLogic VL-CBL-3403	1.5 foot 34-pin dual floppy drive interface cable	35	3.700	6.325

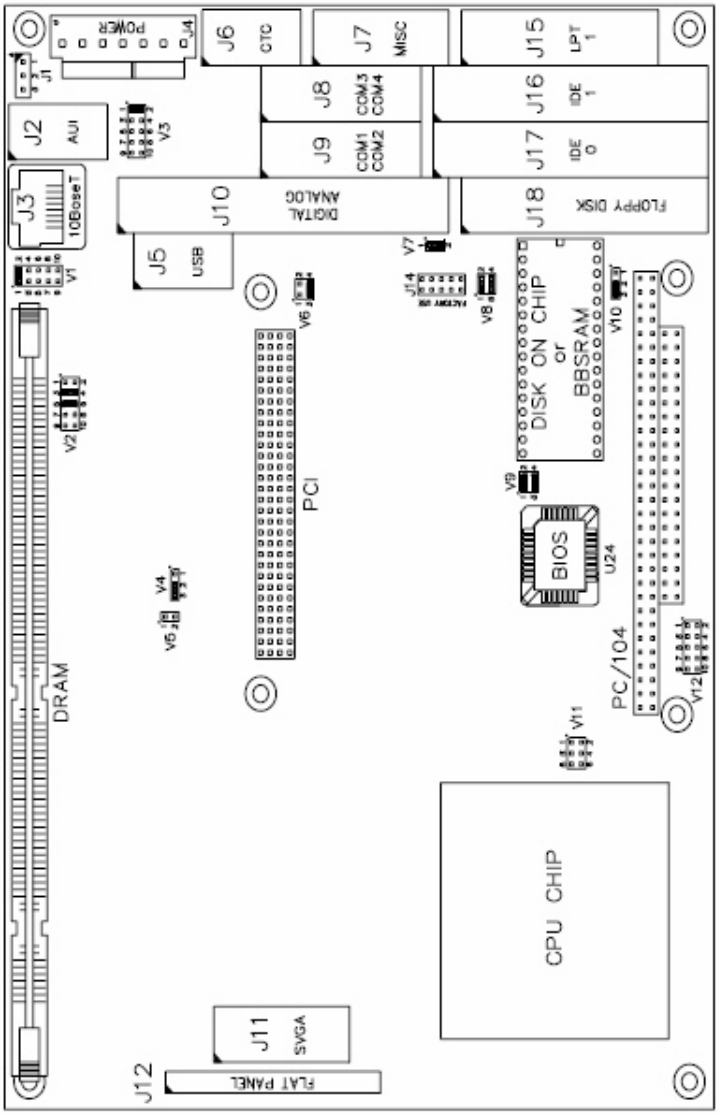
* **Note:** These standard .100" dual-row low profile headers are 3M 2500 series compatible. They are compatible with 3M snap-in latches, socket retaining clips, polarizing posts, and keys.

§ **Note:** This connector is a 2.00mm housing and crimp terminal style. Number of crimp terminals depends upon flat panel display model being used.

‡ **Note:** Measurement in inches relative to lower left hand mounting hole. See Figure 1.

Jumper Block Locations

Note! Jumpers shown in as-shipped configuration.



MODEL	V11	V12 Vcore
VSBC-6ap VSBC-6ar		2.2V
VSBC-6bp VSBC-6br		2.2V
VSBC-6cp VSBC-6cr		2.8V
VSBC-6dp VSBC-6dr DISCONTINUED		2.2V
VSBC-6ep VSBC-6er		2.2V
VSBC-6fp VSBC-6fr DISCONTINUED		2.2V
VSBC-6gp VSBC-6gr		2.2V
VSBC-6hp VSBC-6hr VSBC-6hT		1.85V
VSBC-6sp VSBC-6sr VSBC-6tp		1.85V

Rev 5 or later PCB's only

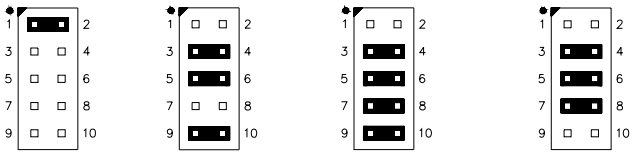
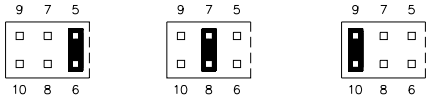
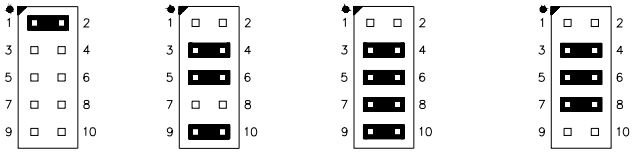
V12 (Vcore Selection)		
2.2V	2.8V	1.85V

Figure 4. Jumper Block Locations

Note: See page 25 for details on how to determine the proper V_{CORE} voltage for your CPU chip.

JUMPER SUMMARY

Table 2: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1	**COM3 Configuration** RS-232 RS-422 RS-485 Endpoint Station RS-485 Intermediate Station 	RS-232	30
V2	**Counter/Timer 4 Clock Source** External Input 6 MHz  ***Note!*** *Only ½ of jumper block V2 is shown in this picture.*	6 MHz	51
V2	**Counter/Timer 5 Clock Source** 6 MHz CTC#4 External Input  ***Note!*** *Only ½ of jumper block V2 is shown in this picture.*	6 MHz	51
V3	**COM4 Configuration** RS-232 RS-422 RS-485 Endpoint Station RS-485 Intermediate Station  ***Note!*** *Jumper V3 is shown in the vertical orientation. On the VSBC-6 circuit board, the jumper block is oriented horizontally.*	RS-232	30
V4	**CMOS RAM and Real Time Clock Erase** Erase Normal Operation  ***Note!*** *Do not operate the board with the jumper in the erase position. Leave the jumper in position V4[1-2] for at least one full minute to fully erase CMOS RAM.*	Normal	27
V5[1-2]	**CMOS Battery Test Terminals** ***Note!*** *V5 is not a jumper, it is used as a quality control test point to measure the current flowing in the battery circuit.*	Out	—

Jumper Block	Description	As Shipped	Page
V6[1-2]	**Ethernet Media Configuration** In — AUI Out — 10BaseT	Out	39
V6[3-4]	**Ethernet Address Configuration** In — Base Address defined in CMOS Setup Out — Base Address 300h	In	39,54
V7	**Opto 22 I/O Rack Power** In — I/O rack power provided by VSBC Out — I/O rack power provided externally	In	49
V8[1-2]	**System BIOS Selector** In — Primary System BIOS occupies F0000h to FFFFFh Out — Secondary System BIOS occupies F0000h to FFFFFh ***Note!*** *The secondary System BIOS is field upgradable using the BIOS upgrade utility. See www.versalogic.com/private/vsbc6support.asp for further information.*	In	—
V8[3-4]	**Video BIOS Selector** In — Primary Video BIOS occupies C0000h to C9FFFh Out — Secondary Video BIOS occupies C0000h to C9FFFh ***Note!*** *The secondary Video BIOS is field upgradable using the BIOS upgrade utility. See www.versalogic.com/private/vsbc6support.asp for further information.*	In	—
V9[1-2]	**General Purpose Input 0** In — CPU reads bit as 0 Out — CPU reads bit as 1 ***Note!*** *This jumper is reserved. Contact factory for more information.*	In	—
V9[3-4]	**General Purpose Input 1** In — CPU reads bit as 0 Out — CPU reads bit as 1 ***Note!*** *This jumper is reserved. Contact factory for more information.*	In	—
V10	**32-Pin DIP Memory Socket Device Type Selector** BBSRAM DOC  ***Note!*** *The 32-pin socket must be enabled in CMOS Setup.*	BBSRAM	28
V11	**CPU Clock Speed Multiplier** **V11[5-6] / V11[3-4] / V11[1-2] / Multiplier / Speed** Out / Out / In / 6.0 / 400 MHz Out / In / In / 2.5 [4.0] / 166 MHz [266] Out / In / Out / 3.0 / 200 MHz Out / Out / Out / 3.5 / 233 MHz In / Out / In / 4.0 / 266 MHz In / In / In / 4.5 / 300 MHz In / In / Out / 5.0 / 333 MHz In / Out / Out / 5.5 / 366 MHz ***Note!*** *Numbers in brackets are for Intel Tillamook 266 MHz CPU chips. Rev 5 or later.*	Varies	25

Jumper Block	Description	As Shipped	Page
V12	**CPU Core Voltage Selection**	Varies	25

V12[9-10]	V12[7-8]	V12[5-6]	V12[3-4]	V12[1-2]	Voltage
In	In	Out	In	Out	1.80 V
In	**In**	**Out**	**In**	**In**	**1.85 V**
In	In	In	Out	Out	1.90 V
In	In	In	Out	In	1.95 V
In	In	In	In	Out	2.00 V
In	In	In	In	In	2.05 V
Out	Out	Out	Out	Out	2.00 V
Out	Out	Out	Out	In	2.10 V
Out	**Out**	**Out**	**In**	**Out**	**2.20 V**
Out	Out	Out	In	In	2.30 V
Out	**Out**	**In**	**Out**	**Out**	**2.40 V**
Out	Out	In	Out	In	2.50 V
Out	Out	In	In	Out	2.60 V
Out	Out	In	In	In	2.70 V
Out	**In**	**Out**	**Out**	**Out**	**2.80 V**
Out	**In**	**Out**	**Out**	**In**	**2.90 V**
Out	In	Out	In	Out	3.00 V
Out	In	Out	In	In	3.10 V
Out	In	In	Out	Out	3.20 V
Out	In	In	Out	In	3.30 V
Out	In	In	In	Out	3.40 V
Out	In	In	In	In	3.50 V

Note! *Bold entries correspond to the approved CPU list on page 25. Do not confuse CPU Core Voltage with CPU I/O voltage. The VSBC-6 will only work with CPU chips with an I/O voltage of 3.3V.*

Power Supply

POWER CONNECTORS

Main power is applied to the VSBC-6 through an EBX style 7-pin polarized connector (mating connector Molex Housing 09-50-8073, Pins 08-52-0072). A 3-pin auxiliary power input connector is also provided to supply –5V and –12V to the PC/104-*Plus* stack.

See page 17 for connector pinout and location information.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors be wired correctly. Make sure to use both +5VDC pins and all three ground pins to prevent excess voltage drop.

Table 3: Main Power Connector Pinout

J4 Pin	Signal Name	Description
1	+5VDC	Power Input
2	Ground	Digital Ground
3	Ground	Digital Ground
4	+12VDC	Power Input
5	+3.3VDC	Power Input
6	Ground	Digital Ground
7	+5VDC	Power Input

Note! The +3.3VDC and +12VDC inputs on the main power connector are only required for PC/104-*Plus* expansion modules that require these voltages. The AUI interface on the Ethernet port also uses +12VDC.

Table 4: Auxiliary Power Connector Pinout

J1 Pin	Signal Name	Description
1	–5VDC	Power Input
2	Ground	Digital Ground
3	–12VDC	Power Input

Note! Auxiliary voltages are only required for PC/104-*Plus* expansion modules that require these voltage.

POWER REQUIREMENTS

The VSBC-6 requires only +5 volts (±5%) for proper operation. The voltage required for the RS-232 ports and analog input sections are generated with a DC/DC converter. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the VSBC-6 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules, and attached devices. For example, AT keyboards typically draw their power directly from the VSBC-6, and driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 3.0V, contact the factory for a replacement (part number T-HB3/5-2). Life expectancy under normal use is approximately 10 years.

Note! The VSBC-6 is designed to boot even with a dead or removed battery. See page 27 for further information.

CPU

CPU CLOCK SPEED MULTIPLIER

Jumper block V11 is used to multiply the on-board 66 MHz bus clock to match the internal clock speed of the CPU chip. For example, the 200 MHz CPU shown shown below uses a multiplier of 3.0

See page 21 for jumper configuration details.

CPU CORE VOLTAGE SELECTION

Jumper block V12 is used to program a variable output voltage regulator to match the V_{CORE} power supply requirements of the CPU chip. The V_{CORE} voltage can be determined by examining the information marked on the lid of the CPU chip.

Warning! To prevent damage to the CPU chip or the VSBC-6 circuity, you must always double check the V_{CORE} voltage indicated on the cover of the CPU chip and make sure jumper V12 is set properly.

APPROVED CPU LIST

The following list of Socket 7, 3.3V I/O voltage, 66MHz external bus compliant CPU chips are approved for use in the VSBC-6. Care must be taken to correctly configure jumper V11 to match the *CPU Clock Speed Multiplier* as shown in the table below. Jumper V12 must be configured to match the *CPU Core Voltage* as marked on the cover of the CPU chip. See pages 21 and 22 for jumper configuration details.

Table 5: CPU Configuration Table

Mfg.	Description	CPU Speed	CPU Clock Speed Multiplier
Intel	Pentium MMX	233 MHz	3.5
Intel	Tillamook	266 MHz	4.0
AMD	K6-2	266 MHz	4.0
AMD	K6-2E	266 MHz	4.0
AMD	K6-2	300 MHz	4.5
AMD	K6-2	333 MHz	5.0
AMD	K6-2	366 MHz	5.5
AMD	K6-2	400 MHz	6.0

Warning! Incorrect configuration can result in damage to the CPU chip and the VSBC-6 circuitry. Consult your CPU documentation to correctly identify clock speed, core voltage and I/O voltage prior to installation. Failure to configure and operate your CPU in accordance within the specified parameters will void your warranty.

HEAT SINK

A heat sink and cooling fan must be in place whenever power is applied to the CPU. Either a clip-on or stick-on type may be used. The fan must be a 5V type. Ball bearing models are recommended for longevity. The fan connects to header J13 for power with the positive lead (red wire) connected to pin 2 (the pin nearest to the CPU chip).

Table 6: Fan Power Connector

J13 Pin	Signal Name	Function
1	GND	Ground
2	+5V	Fan Power

L2 CACHE MEMORY

No configuration is required for the L2 Cache memory. The VSBC-6 is shipped with 512 MB of cache memory.

System RAM

COMPATIBLE MEMORY MODULES

The VSBC-6 will accept one 168-pin DIMM memory module with the following characteristics:

- Size 8 to 256 MB
- Voltage 3.3 Volt
- Error Detection Parity or Non-Parity
- Error Correction ECC or Non-ECC
- Type EDO, 60 ns (all VSBC-6 revisions)
  EDO, 60 ns or SDRAM, PC-66 or PC-100 (VSBC-6 rev 4.00 or later)

Note: Parity and ECC features are not supported in the BIOS.

CMOS RAM

CLEARING CMOS RAM

Jumper V4[2-3] is normally inserted to provide battery power to the CMOS RAM circuits. The jumper can be briefly moved to position V4[1-2] to erase the contents of the CMOS RAM should it become necessary to do so. Do not operate the board with the jumper in the erase position.

Note! The jumper should remain in position V4[1-2] for a full minute to properly erase the CMOS RAM contents.

Real Time Clock

The VSBC features a year 2000 compliant, battery-backed 146818 compatible real time clock/calendar chip. Under normal battery conditions, the clock will maintain accurate timekeeping functions during periods when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the [DEL] key during a system boot) can be used to set the time/date of the real time clock.

Disk on Chip

Socket U22 will accept an M-Systems DiskOnChip (DOC) Flash Disk for non-volatile, read/write data storage. The DOC can be configured as a boot device

ENABLE / DISABLE

The DOC can be enabled or disabled through CMOS Setup by going into the Custom screen and setting "64 K memory page at E000 "DOC" or "Disabled". When enabled, the DOC appears in the upper memory region as an 64 K page frame from E0000h to EFFFFh.

COMPATIBLE DEVICES

Any 5 Volt, M-Systems series rev 1.10 or later 2000 DOC device will work.

INSTALLING THE DOC CHIP

1. Align pin 1 on the DOC with pin 1 of socket U22.
2. Push the DOC into the socket carefully until it is fully seated.
3. Make sure jumper V10[1-2] is installed.

Warning! ***The DOC can be permanently damaged if installed incorrectly!*** When installing or removing the DOC, be sure to align the chip as shown in the picture below. To prevent electrostatic damage, first touch a grounded surface to discharge any static electricity from your body.

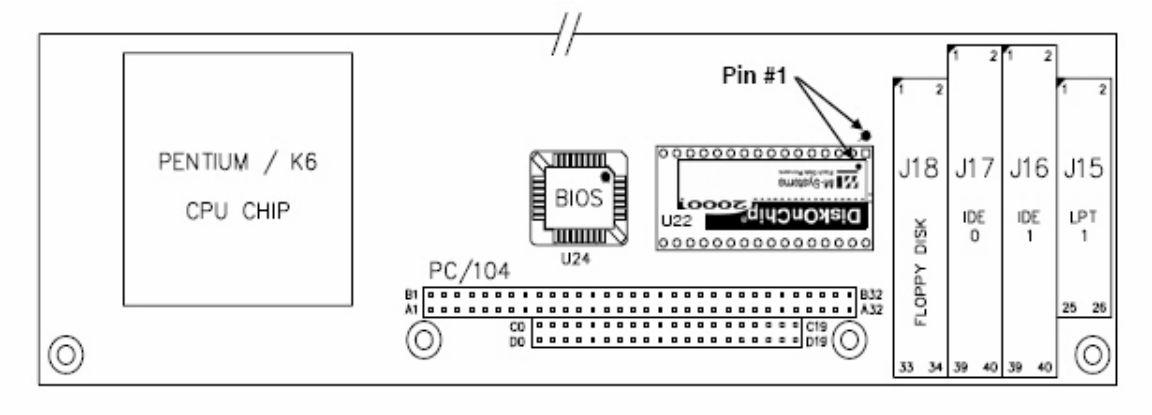


Figure 5. Disk On Chip Orientation

CMOS SETUP

To enable the DOC as drive C on a system without a hard disk, set the CMOS setup of drive C to "not installed", and reboot the computer.

Note! The DOC needs to be formatted with the System files in order for it to be a bootable drive. Refer to the M-Sy[U22] ns web site (www.m-sys.com) for documentation on the DOC and details on making it a bootable device.

Serial Ports

The VSBC-6 features four on-board 16550 based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2K baud) serial ports with interrupts fixed at IRQ4 and IRQ3 respectively. IRQ use can be enabled/disabled in CMOS Setup.

COM3 and COM4 can be operated in RS-232, RS-422, or RS-485 modes. Two additional non-standard baud rates are also available (programmable in the normal baud registers) of 230K and 460K baud. IRQ lines are chosen in CMOS Setup, and can be mapped to any IRQ line.

Each COM port can be independently enabled or disabled in the CMOS Setup screen.

COM Port Configuration

There are no configuration jumpers for COM1 and COM2 since they only operate in RS-232 mode.

Jumper V1 is used to configure COM3 for RS-232/422/485 operation. Jumper V3 is used to configure COM4. See page 20 for jumper configuration details.

COM3 / COM4 RS-485 Mode Line Driver Control

The TxD+/TxD– differential line driver can be turned on and off by manipulating the DTR handshaking line.

The following code example shows how to turn the line driver for COM3 or COM4 on and off:

```
mov   dx,03ECh   ; Point to COM3 Modem Control register
mov   dx,02ECh   ; or COM4 if desired
in    al,dx      ; Fetch existing value
or    al,01h     ; Set bit D0
out   dx,al      ; Turn DTR on (enables line driver)

in    al,dx      ; Fetch existing value
and   al,0FEh    ; Clear bit D0
out   dx,al      ; Turn DTR off (disables line driver)
```

SERIAL PORT CONNECTORS

See the *Connector Location Diagram* on pages 17 and 18 for connector and cable information. The pinout of the DB9 connector applies to use of the VersaLogic transition cable #VL-CBL-2001.

Table 7: Connectors J8/J9 — Serial Port Pinout

COM1 J9 Pin	COM2 J9 Pin	COM3 J8 Pin	COM4 J8 Pin	RS-232	RS-422	RS-485	DB9 Pin
1	11	1	11	DCD	—	—	1
2	12	2	12	DSR	—	—	6
3	13	3	13	RXD*	TxD+	TxD+	2
4	14	4	14	RTS	TxD–	TxD–	7
5	15	5	15	TXD*	—	—	3
6	16	6	16	CTS	Ground	Ground	8
7	17	7	17	DTR	RxD–	TxD/RxD–	4
8	18	8	18	RI	RxD+	TxD/RxD+	9
9	19	9	19	Ground	Ground	Ground	5
10	20	10	20	N/C	—	—	—

Parallel Port

The VSBC-6 includes a standard bi-directional/EPP/ECP compatible LPT port which resides at the PC standard address of 378h. The port can be enabled/disabled and interrupt assignments can be made via the CMOS Setup screen. The pinout of the DB25 connector applies to use of the VersaLogic transition cable #VL-CBL-2601.

Table 8: LPT1 Parallel Port Pinout

J15 Pin	Centronics Signal	Signal Direction	DB25 Pin
1	Strobe	Out	1
2	Auto feed	Out	14
3	Data bit 1	In/Out	2
4	Printer error	In	15
5	Data bit 2	In/Out	3
6	Reset	Out	16
7	Data bit 3	In/Out	4
8	Select input	Out	17
9	Data bit 4	In/Out	5
10	Ground	—	18
11	Data bit 5	In/Out	6
12	Ground	—	19
13	Data bit 6	In/Out	7
14	Ground	—	20
15	Data bit 7	In/Out	8
16	Ground	—	21
17	Data bit 8	In/Out	9
18	Ground	—	22
19	Acknowledge	In	10
20	Ground	—	23
21	Port Busy	In	11
22	Ground	—	24
23	Paper End	In	12
24	Ground	—	25
25	Select	In	13
26	No Connect	—	—

EIDE Hard Drive / CD-ROM Interfaces

Two EIDE interfaces are available to connect up to four hard disk or CD-ROM drives. Connector J17 is the primary IDE controller and connector J16 is the secondary IDE controller. Use CMOS Setup to specify the drive parameters of the attached drives.

Some older IDE drivers, such as those that are PIO Mode 0-1, do not operate reliably with this product. VersaLogic recommends the use of only PIO Mode 2-3 and Ultra DMA type drives with this product.

Warning! Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 9: EIDE Hard Drive Connector Pinout

J16, J17 Pin	Signal Name	EIDE Signal Name	Function
1	HRST*	Host Reset	Reset signal from CPU
2	Ground	Ground	Ground
3	IDE7	DATA 7	Data bit 7
4	HD8	DATA 8	Data bit 8
5	HD6	DATA 6	Data bit 6
6	HD9	DATA 9	Data bit 9
7	HD5	DATA 5	Data bit 5
8	HD10	DATA 10	Data bit 10
9	HD4	DATA 4	Data bit 4
10	HD11	DATA 11	Data bit 11
11	HD3	DATA 3	Data bit 3
12	HD12	DATA 12	Data bit 12
13	HD2	DATA 2	Data bit 2
14	HD13	DATA 13	Data bit 13
15	HD1	DATA 1	Data bit 1
16	HD14	DATA 14	Data bit 14
17	HD0	DATA 0	Data bit 0
18	HD15	DATA 15	Data bit 15
19	Ground	Ground	Ground
20	NC	NC	No connection
21	NC	NC	No connection
22	Ground	Ground	Ground
23	HWR*	HOST IOW*	I/O write
24	Ground	Ground	Ground
25	HRD*	HOST IOR*	I/O read
26	Ground	Ground	Ground
27	NC	NC	No connection
28	HAEN	ALE	Address latch enable
29	NC	NC	No connection
30	Ground	Ground	Ground
31	HINT	HOST IRQ14	IRQ14
32	XI16*	HOST IOCS16*	Drive register enabled
33	HA1	HOST ADDR1	Address bit 1
34	NC	NC	No connection
35	HA0	HOST ADDR0	Address bit 0
36	HA2	HOST ADDR2	Address bit 2
37	HCS0*	HOST CS0*	Reg. access chip select 0
38	HCS1*	HOST CS1*	Reg. access chip select 1
39	NC	NC	No connection
40	Ground	Ground	Ground

Utility Connector

KEYBOARD/MOUSE INTERFACE

A standard PS/2 keyboard and mouse interface is accessible through connector J7. In addition, connector J7 supports a programmable LED output, hard drive activity LED, and a speaker output as shown in the table below. The pinout of the PS/2 connectors applies to use of the VersaLogic transition cable #VL-CBL-1602.

Table 10: Utility Connector

J7 Pin	Signal Name	Description	PS/2 Pin	
1	PBRST*	Push-button reset		
2	GND	Ground		
3	PLED*	Programmable LED		
4	MKPWR	Protected +5V		
5	SPKO*	Speaker Output		
6	MKPWR	Protected +5V		
7	IDE_LED*	IDE Drive Indicator LED		
8	MKPWR	Protected +5V		
9	MKPWR	Protected +5V	4	
10	XMSDATA	Mouse Data	1	← Mouse Connector
11	GND	Ground	3	
12	MSCLK	Mouse Clock	5	
13	MKPWR	Protected +5V	4	
14	KBDATA	Keyboard Data	1	← Keyboard Connector
15	GND	Ground	3	
16	KBCLK	Keyboard Clock	5	

PROGRAMMABLE LED

The Utility Connector J7 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J7 pin 3, connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on.

To turn the LED on and off, set or clear bit D7 in I/O port 0E0h (or 1E0h if selected in CMOS Setup). When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn on and off the LED. Refer to page 56 for further information:

LED On

```
in    al,E0h
or    al,80h
out   E0h,al
```

LED Off

```
in    al,E0h
and   al,7Fh
out   E0,al
```

Note! The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

EXTERNAL SPEAKER

A miniature 8 ohm speaker can be connected between J7 pin 5 (SPKO*) and J7 pin 6 (MKPWR).

PUSH-BUTTON RESET

The Utility Connector J7 (see page 34) includes an input for a push-button reset switch. Shorting J7 pin 1 to ground will cause the VSBC-6 to reboot.

Floppy Drive Interface

The VSBC-6 supports a standard 34-pin PC/AT style floppy disk interface at connector J18. Up to two floppy drives can be attached to this port. CMOS Setup can be used to enable or disable the floppy disk interface.

Warning! Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 11: Floppy Disk Interface Connector Pinout

J18 Pin	Signal Name	Function
1	Ground	Ground
2	R/LC	Load Head
3	Ground	Ground
4	NC	No Connection
5	Ground	Ground
6	NC	No Connection
7	Ground	Ground
8	INDX*	Beginning Of Track
9	Ground	Ground
10	MTR1*	Motor Enable 1
11	Ground	Ground
12	DRV0*	Drive Select 0
13	Ground	Ground
14	DRE1*	Drive Select 1
15	Ground	Ground
16	MTR0*	Motor Enable 0
17	Ground	Ground
18	DIR	Direction Select
19	Ground	Ground
20	STEP*	Motor Step
21	Ground	Ground
22	WDAT*	Write Data Strobe
23	Ground	Ground
24	WGAT*	Write Enable
25	Ground	Ground
26	TRK0*	Track 0 Indicator
27	Ground	Ground
28	WPRT*	Write Protect
29	Ground	Ground
30	RDAT*	Read Data
31	Ground	Ground
32	HDSL	Head Select
33	Ground	Ground
34	DCHG	Drive Door Open

Video Interface

An on-board Chips and Technologies 65550 video controller with 2MB video RAM provides full SVGA video output capabilities for the VSBC-6.

Windows 95/98/NT automatically detects the 65550 and installs native driver support for all resolutions and color depths. The 65550 is also supported by QNX and VXWorks operating systems.

A 40KB video BIOS located at C0000h can be shadowed via CMOS Setup.

VIDEO RESOLUTIONS

Several standard VESA SVGA modes and color depths are available depending upon the amount of installed video RAM.

Table 12: Video Resolutions

2 MB Video RAM *(standard)*	**1 MB Video RAM** *(optional)*
640 x 480, 16M colors	640 x 480, 16M colors
800 x 600, 16M colors	800 x 600, 64K colors
1024 x 768, 64K colors	1024 x 768, 256 colors
1280 x 1024, 256 colors	1280 x 1024, 16 colors

VIDEO OUTPUT CONNECTOR

See the *Connector Location Diagram* on page 17 for pin and connector location information. An adapter cable, part number VL-CBL-1601, is available to translate J11 into a standard 15-pin D-Sub SVGA connector.

Table 13: Video Output Pinout

J11 Pin	Signal Name	Function	Mini DB15 Pin
1	CRED	Red video	1
2	NC	No connect	9
3	CGRN	Green video	2
4	SGND	Sync return (digital ground)	10
5	CBLU	Blue video	3
6	N/C	No connect	11
7	N/C	No Connect	4
8	N/C	No Connect	12
9	GND	Digital ground	5
10	CHSYNC	Horizontal sync	13
11	GND	Red ground	6
12	CVSYNC	Vertical sync	14
13	GND	Green ground	7
14	N/C	No Connect	15
15	GND	Blue ground	8
16	NC	No connect	N/C

FLAT PANEL DISPLAY CONNECTOR

See the *Connector Location Diagram* on page 17 for pin and connector location information.

Table 14: Flat Panel Display Pinout

J12 Pin	Signal Name	Function	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 9/12/ 16-bit	Color TFT 18/24 bit	Color TFT HR 18/24 bit	Color STN STN SS 8-bit (X4bP)	Color STN SS 16-bit (4bP)	Color STN DD 8-bit (4bP)	Color STN DD 16-bit (4bP)	Color STN DD 24-bit
1	+12V	Power Supply											
2	+12V	Power Supply											
3	GND	Ground											
4	GND	Ground											
5	+5V	Power Supply											
6	+5V	Power Supply											
7	ENAVEE	Power sequencing control for LCD bias voltage											
8	GND	Ground											
9	P0	Data Output		UD3	UD7	B0	B0	B00	R1	R1	UR1	UR0	UR0
10	P1	" "		UD2	UD6	B1	B1	B01	B1	G1	UG1	UG0	UG0
11	P2	" "		UD1	UD5	B2	B2	B02	G2	B1	UB1	UB0	UB0
12	P3	" "		UD0	UD4	B3	B3	B03	R3	R2	UR2	UR1	LR0
13	P4	" "		LD3	UD3	B4	B4	B10	B3	G2	LR1	LR0	LG0
14	P5	" "		LD2	UD2	G0	B5	B11	G4	B2	LG1	LG0	LB0
15	P6	" "		LD1	UD1	G1	B6	B12	R5	R3	LB1	LB0	UR1
16	P7	" "		LD0	UD0	G2	B7	B13	B5	G3	LR2	LR1	UG1
17	P8	" "	P0		LD7	G3	G0	G00	SHF CLKU	B3		UG1	UB1
18	P9	" "	P1		LD6	G4	G1	G01		R4		UB1	LR1
19	P10	" "	P2		LD5	G5	G2	G02		G4		UR2	LG1
20	P11	" "	P3		LD4	R0	G3	G03		B4		UG2	LB1
21	P12	" "	P4		LD3	R1	G4	G10		R5		LG1	UR2
22	P13	" "	P5		LD2	R2	G5	G11		G5		LB1	UG2
23	P14	" "	P6		LD1	R3	G6	G12		B5		LR2	UB2
24	P15	" "	P7		LD0	R4	G7	G13		R6		LG2	LR2
25	P16	" "					R0	R00					LG2
26	P17	" "					R1	R01					LB2
27	P18	" "					R2	R02					UR3
28	P19	" "					R3	R03					UG3
29	P20	" "					R4	R10					UB3
30	P21	" "					R5	R11					LR3
31	P22	" "					R6	R12					LG3
32	P23	" "					R7	R13					LB3
33	GND	Ground											
34	GND	Ground											
35	SHFCLK	Shift Clock. Pixel clock for flat panel data.	SHF CLK	SHF CLK	SHF CLK	SHF CLK	SHF CLK	SHF CLK	SHF CLK	SHF CLK	SHF CLK	SHF CLK	SHF CLK
36	FLM	First Line Marker. Flat panel equivalent of VSYNC.											
37	DE	Display Enable or M signal (ADCCLK) or BLANK#											
38	LP	Latch Pulse. Flat panel equivalent of HSYNC.											
39	GND	Ground											
40	ENABKL	Enable Backlight. Can be programmed for other functions.											
41	N/C	No Connection											
42	N/C	" "											
43	N/C	" "											
44	N/C	" "											

COMPATIBLE FLAT PANEL DISPLAYS

The following list of flat panel displays are reported to work properly with the Chips and Technologies 65550B video controller chip used on the VSBC-6:

- Fujitsu FLC31SVC6S
- Hitachi D01VC1CAA
- Hitachi LMG9970ZWCC
- Hitachi LMG9972ZWCC
- Hitachi TX34D61VC1CAD
- NEC NL8060BC31-01
- Optrex DMF-50714NCU-FW (1024x768 DSTN)
- Samsung LT121-103
- Samsung LT133X1-104
- Samsung LT133X1-124
- Sanyo LM-GK53-22NTX (DSTN)
- Sanyo LM-GD53-22NAZ
- Sharp LM15X80 (XGA DSTN)
- Sharp LQ14X01
- Sharp LQ9D03B (640x480 TFT)
- Toshiba LTM12C016
- Toshiba LTM10C209

Ethernet Interface

The VSBC-6 features an industry-standard Ethernet interface based on the SMC LAN LAN91C96 Interface Chip. While this interface is not NE2000 compatible, the SMC 9000 series is widely supported. Drivers are readily available to support a variety of operating systems such as QNX, VxWorks and other RTOS vendors. Win95/98/NT ship with built-in support for this Ethernet interface. The drivers load automatically when the operating system is installed.

HARDWARE CONFIGURATION

Jumper V6[3-4] is used to select the base I/O address for the Ethernet interface, and jumper V6[1-2] is used to select the Ethernet media you will be using. Select the twisted pair interface if you want to connect a twisted pair cable to the RJ45 connector. Select the AUI interface if you want to attach an external transceiver or Media Attachment Unit (MAU). This allows use of thick or thin coax cable, or fiber optic media to be used.

See page 21 for jumper configuration details.

Note! Use of the AUI interface requires connection of +12V power to the VSBC-6.

SOFTWARE CONFIGURATION

The CMOS Setup screen is used to define the base address and the IRQ line used by the Ethernet interface, or to enable/disable the device. When disabled, the ethernet interface is "parked" at I/O addresses 180h – 18Fh and it does not use any interrupts.

ETHERNET CONNECTORS

Table 15: RJ45 Ethernet Connector

J3 Pin	Signal Name	Function
1	T+	Transmit Data +
2	T–	Transmit Data –
3	R+	Receive Data +
4	NC	No Connection
5	NC	No Connection
6	R–	Receive Data –

Table 16: AUI Ethernet Connector

J2 Pin	Signal Name	Function
1	CD–	Collision Detect –
2	CD+	Collision Detect +
3	TX–	Transmit Data –
4	TX+	Transmit Data +
5	GND	Ground
6	GND	Ground
7	RX–	Receive Data –
8	RX+	Receive Data +
9	+12V	+12V Power
10	GND	Ground

Watchdog Timer

A watchdog timer circuit is included on the VSBC-6 to reset the CPU if proper software execution fails or a hardware malfunction occurs.

ENABLING THE WATCHDOG

To enable or disable the watchdog, set or clear bit D0 in I/O port 0E0h (or 1E0h if selected in CMOS Setup). When changing the contents of the register, make sure not to alter the value of the other bits.

The following code example enables the watchdog:

```
in    al,E0h
or    al,01h
out   E0h,al
```

Note! The watchdog timer powers up in a disabled state.

REFRESHING THE WATCHDOG

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (250 ms). Outputting a 5Ah to the *Watchdog Timer Hold-Off Register* at 0E1h (or 1E1h if selected in CMOS Setup) resets the watchdog time-out period, preventing the CPU from being reset for the next 250 ms. See page 57 for additional information.

There is no provision for selecting a different timeout period using software.

The following code example refreshes the watchdog:

```
mov   al,5Ah
out   E1h,al
```

Analog Input

The VSBC-6 "–r" models employ a multi-range, 12-bit A/D converter which will accept up to eight single-ended input signals. The converter features fast 6 microsecond conversion time, with channel independent input ranges of 0 to +5V, ±5V, 0 to +10V, and ±10V.

HARDWARE CONFIGURATION

There are no jumpers associated with the analog input circuitry.

EXTERNAL CONNECTIONS

Single-ended analog voltages are applied to connector J10 as shown in the table below.

Table 17: Analog Input Connector

J10 Pin	Signal Name	Function
1	ADCH0	Channel 0 Analog Input
2	ADCH1	Channel 1 Analog Input
3	ADGND	Analog Ground
4	ADCH2	Channel 2 Analog Input
5	ADCH3	Channel 3 Analog Input
6	ADGND	Analog Ground
7	ADCH4	Channel 4 Analog Input
8	ADCH5	Channel 5 Analog Input
9	ADGND	Analog Ground
10	ADCH6	Channel 6 Analog Input
11	ADCH7	Channel 7 Analog Input
12	ADGND	Analog Ground

Note! Connector J10 also includes signals for the Opto 22 interface.

Warning! All analog inputs are fault protected to ±16V (board power on or off). Exceeding these maximums can cause permanent damage to the A/D converter circuitry. Such damage is not covered under warranty.

CALIBRATION

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

ANALOG CONTROL REGISTER

ACR (WRITE) 00E4h (or 01E4h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0

Table 18: Analog Control Register Bit Assignments

Bit	Mnemonic	Description
D7, D6	PD1, PD0	**Clock and Power-Down Selection** — These bits select the power savings mode and clock source for the A/D circuit. **PD1 PD0 Mode** 0 0 Normal Operation / External Clock Mode 0 1 Normal Operation / Internal Clock Mode 1 0 Standby Power-Down (STBYPD) 1 1 Full Power-Down (FULLPD) ***Note!*** *STBYPD and FULLPD selections do not affect the clock mode.*
D5	ACQMOD	**Acquisition Mode** — This bit selects the type of acquisition mode. ACQMOD = 0 Internal Acquisition. A write to the ACR register will initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3.26µs) ends. ACQMOD = 1 External Acquisition. Use this mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The acquisition and start-of-conversion is controlled with two separate writes to the ACR register. The first write, written with ACQMOD = 1, starts and acquisition interval of indeterminate length. The second write, written with ACQMOD = 0, terminates acquisition and starts conversion. However, if the second write contains ACQMOD = 1, an indefinite acquisition interval is restarted. ***Note!*** *The address bits for the input mux (A0–A2) must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write.*
D4, D3	RNG, BIP	**Range and Polarity Selection** — These bits select the input range and polarity on a channel-by-channel basis. **RNG BIP Input Range** 0 0 0 to +5V 1 0 0 to +10V 0 1 ±5V 1 1 ±10V ***Warning!*** *The board can be damaged if voltages in excess of ±16V are applied.*
D2-D0	A2, A1, A0	**Input Channel Address** — These bits select which input channel you wish to convert. **A2 A1 A0 Channel** 0 0 0 Channel 0 0 0 1 Channel 1 0 1 0 Channel 2 0 1 1 Channel 3 1 0 0 Channel 4 1 0 1 Channel 5 1 1 0 Channel 6 1 1 1 Channel 7

DIGITAL CONTROL / ANALOG STATUS REGISTER

DCAS (READ/WRITE) 00E2h (or 01E2h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	—	DONE	DIRHI	DIRLO

Table 19: Digital Control / Analog Status Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	—	**Reserved** — These bits have no function.
D2	DONE	**Analog Input Conversion Complete** — This status bit is used to determine when it is OK to read data from the A/D converter. DONE = 0 Conversion underway, data not yet available. DONE = 1 Analog input conversion has completed. Valid data is available to be read from the ADCLO and ADCHI registers. Done is reset to "0" when a new conversion is started. ***Note!*** *This bit is not valid until an A/D conversion cycle has been triggered.*
D1	DIRHI	**Direction Control for Opto 22 Digital I/O Hi Port** — This bit controls the input/output direction of the digital I/O signals DIO8–DIO15. DIRHI = 0 Input DIRHI = 1 Output ***Note!*** *See page 49 for further information.*
D0	DIRLO	**Direction Control for Opto 22 Digital I/O Lo Port** — This bit controls the input/output direction of the digital I/O signals DIO0–DIO7. DIRLO = 0 Input DIRLO = 1 Output ***Note!*** *See page 49 for further information.*

ADC DATA HIGH REGISTER

ADCHI (READ) 00E5h (or 01E5h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
D11 / 0	D11 / 0	D11 / 0	D11 / 0	D11	D10	D9	D8

The ADCHI register is a read register containing the upper 4 bits of data from the A/D conversion results. It is used in conjunction with the ADCLO register to read the complete 12-bit data word.

When reading data, it is normal convention to read the ADCLO register first, followed by the ADCHI register.

Table 20: ADCHI Bit Assignments

Bit	Mnemonic	Description
D7-D4	D11 / 0	**Sign Extension** — These four bits read as "0" in unipolar input mode (BIP = 0), in bipolar input mode, D11 is duplicated (sign extended) into these four bits.
D3-D0	ADCDATA	**A/D Input Data (Most Significant Nibble)** — These bits contain data bits D11 through D8 of the conversion results.

ADC DATA LOW REGISTER

ADCLO (READ) 00E4h (or 01E4h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

The ADCLO register is a read register containing the lower 8 bits of data from the A/D conversion results. It is used in conjunction with the ADCHI register to read the complete 12-bit data word.

After a conversion is complete (as reported by the DONE bit in the ADCSTAT register) the ADCLO register should be read first, followed by the ADCHI register. A word-wide input instruction from the ADCLO register (in ax,dx) will fetch data from both registers in the proper sequence.

The data registers are located on an even address boundary to facilitate efficient single-cycle reading of the A/D data.

Table 21: ADCLO Bit Assignments

Bit	Mnemonic	Description
D7-D0	ADCDATA	**A/D Input Data (Least Significant Byte)** — These bits contain data bits D7 through D0 of the conversion results.

TWO'S COMPLEMENT DATA FORMAT (±5V AND ±10V ONLY)

The A/D converter translates applied analog voltages into 12-bit, two's complement digital words. The full analog input range is divided into 4096 steps. The output code (0000h) is associated with a mid-range analog value of 0 Volts (ground).

The formulas for calculating analog or digital values are given by:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.004882813 Volts (±10V)
0.002441406 Volts (±5V)

Sample values are shown in the table below:

Table 22: Two's Complement Data Format

±5V Input Voltage	±10V Input Voltage	Hex	Decimal	Comment
+5.000000	+10.000000	—	—	Out of range
+4.997559	+9.995117	07FFh	2047	Maximum positive voltage
+2.500000	+5.000000	0400h	1024	Positive half scale
+1.250000	+2.500000	0200h	512	Positive quarter scale
+0.002441	+0.004883	0001h	1	Positive 1 LSB
0.000000	0.000000	0000h	0	Zero (ground input)
–0.002441	–0.004883	FFFFh	–1	Negative 1 LSB
–1.250000	–2.500000	FE00h	–512	Negative quarter scale
–2.500000	–5.000000	FC00h	–1024	Negative half scale
–5.000000	–10.000000	F800h	–2048	Maximum negative voltage

BINARY FORMAT (0 TO +5V AND 0 TO +10V ONLY)

The full analog input range is divided into 4096 steps. The output code (0000h) is associated with an analog input voltage of 0 Volts (ground). All codes are considered positive.

The formulas for calculating analog or digital values are given by:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.002441406 Volts (0 to +10V Range)
0.001220703 Volts (0 to +5V Range)

Sample values are shown in the table below:

Table 23: Binary Data Format

0 to +5V Input Voltage	0 to +10V Input Voltage	Hex	Decimal	Comment
+5.000000	+10.000000	—	—	Out of range
+4.998779	+9.997559	0FFFh	4095	Maximum voltage
+2.500000	+5.000000	0800h	2048	Half scale
+1.250000	+2.500000	0400h	1024	Quarter scale
+0.001220	+0.002441	0001h	1	1 LSB
0.000000	0.000000	0000h	0	Zero (ground input)

ANALOG INPUT CODE EXAMPLE

The following code example illustrates the procedure for reading a ±10V analog voltage from channel 0:

```
       OUT   0E4h,18h    ;Select channel 0 and begin conversion
BUSY:  IN    AL,0E2h     ;Get A/D status
       AND   AL,04h      ;Isolate the DONE bit
       JZ    BUSY        ;Loop back if conversion isn't complete
DONE:  MOV   DX,00E4h    ;Point to ADCLO register
       IN    AX,DX       ;16-bit input reads ADCLO and ADCHI into AX
```

USB 1.0 Interface

A USB 1.0 (Universal Serial Bus) connector provides a common interface to connect a wide variety of keyboards, modems, mice, and telephony devices to the VSBC-6. With USB 1.0, there is no need to have separate connectors for many common PC peripherals.

The USB 1.0 interface on the VSBC-6 is OHCI (Open Host Controller Interface) compatible, which provides a common industry software/hardware interface.

Note The USB 1.0 interface must be enabled in CMOS Setup.

Table 24: USB 1.0 Interface Connector

J5 Pin	Signal Name	Function
1	USBPWR1	+5V (Protected)
2	USBP00	Channel 0 Data –
3	USBP01	Channel 0 Data +
4	GND1	Digital Ground
5	GND	Cable Shield
6	GND	Cable Shield
7	GND1	Digital Ground
8	USBP11	Channel 1 Data +
9	USBP10	Channel 1 Data –
10	USBPWR1	+5V (Protected)

Warning! Connector J5 is not numbered in the conventional manner as most dual-row headers. Care must be taken to attach the USB 1.0 adapter cables as shown below to prevent voltage reversal.

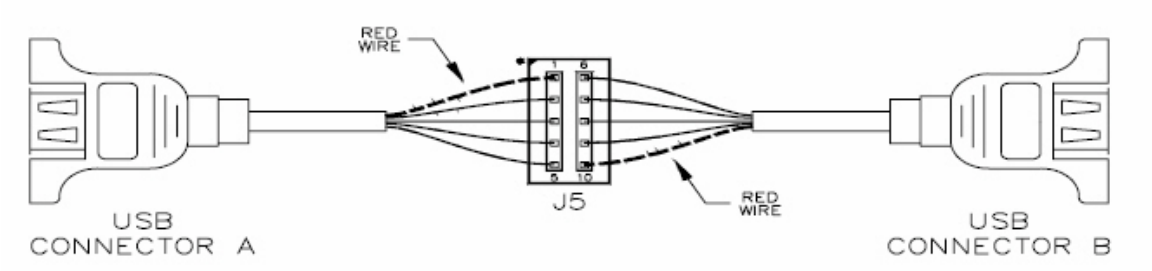


Figure 6. USB 1.0 Connector Orientation Diagram

Opto 22 (Digital I/O) Interface

The VSBC-6 includes a 16-channel digital I/O interface. The digital lines are grouped as two 8-bit bi-directional ports. The direction of each port is controlled by software, and each signal is pulled-up to +5V with a 10K ohm resistor.

The 24 mA source/sink drive and short protected outputs are an excellent choice for industrial TTL interfacing, or they can be used to interface directly (plug compatible) with standard opto-isolated modular I/O racks.

EXTERNAL CONNECTIONS

Table 25: Digital I/O Connector

J10 Pin	Signal Name	Function
13	NC	No Connection
14	GND	Digital Ground
15	NC	No Connection
16	GND	Digital Ground
17	DIO0	OPTO 22 Module 15
18	GND	Digital Ground
19	DIO1	OPTO 22 Module 14
20	GND	Digital Ground
21	DIO2	OPTO 22 Module 13
22	GND	Digital Ground
23	DIO3	OPTO 22 Module 12
24	GND	Digital Ground
25	DIO4	OPTO 22 Module 11
26	GND	Digital Ground
27	DIO5	OPTO 22 Module 10
28	GND	Digital Ground
29	DIO6	OPTO 22 Module 9
30	GND	Digital Ground
31	DIO7	OPTO 22 Module 8
32	GND	Digital Ground
33	DIO8	OPTO 22 Module 7
34	GND	Digital Ground
35	DIO9	OPTO 22 Module 6
36	GND	Digital Ground
37	DIO10	OPTO 22 Module 5
38	GND	Digital Ground
39	DIO11	OPTO 22 Module 4
40	GND	Digital Ground
41	DIO12	OPTO 22 Module 3
42	GND	Digital Ground
43	DIO13	OPTO 22 Module 2
44	GND	Digital Ground
45	DIO14	OPTO 22 Module 1
46	GND	Digital Ground
47	DIO15	OPTO 22 Module 0
48	GND	Digital Ground
49	PWR	+5V Rack Power*
50	GND	Digital Ground

* Optional. Refer to jumper V7 on page 21.

Note! The digital signals on connector J10 are shared with the analog input interface.

RACK POWER

When jumper V7 is installed, up to 250 mA can be drawn from J10 pin 49 to power the Opto 22 interface rack or other external equipment. The power output is protected by a self resetting circuit breaker.

Warning! If the I/O rack is powered by a separate external supply, the power jumper on the I/O rack or jumper V7 must be removed.

SIGNAL DIRECTION

The 16 I/O signals are divided into two 8-bit I/O ports. The direction of each port is controlled by the DIRHI and DIRLO bits in the DCAS register (see page 43).

DIGITAL I/O DATA PORTS

DIOHI (READ/WRITE) 00E7h (or 01E7h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8

DIOLO (READ/WRITE) 00E6h (or 01E6h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

Table 26: Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	DIO15–DIO8 DIO7–DIO0	**Digital I/O Data** — Data written to these register is driven onto the Opto 22 Digital I/O port signals when the port direction is set to output mode. When the port is in input mode, these bits reflect the input state of the signal lines. DIO = 0 Signal low (GND) DIO = 1 Signal high (+5V) ***Note!*** *Opto 22 modules use inverted logic. An "on" module is a "0" logic level.*

Auxiliary Timer/Counter Channels

The VSBC-6 includes three uncommitted 8254 type counter/timer channels for general application program use. Control signals for the three channels are available on connector J6.

JUMPER CONFIGURATION

Jumper V2 selects the clock source for channels 4 and 5. Options include:

- Internal 6 MHz timebase
- External clock from connector J6
- Cascading channels 4 and 5 together for 32-bit counter/timer operations

See page 20 for jumper configuration details.

EXTERNAL CONNECTIONS

Table 27: Counter/Timer I/O Connector

J6 Pin	Signal Name	Function
1	OCTC3	CTC Channel 3 Output
2	GND	Digital Ground
3	ICTC4	CTC Channel 4 Input
4	GND	Digital Ground
5	OCTC4	CTC Channel 4 Output
6	GND	Digital Ground
7	ICTC5	CTC Channel 5 Input
8	GND	Digital Ground
9	OCTC5	CTC Channel 5 Output
10	GND	Digital Ground

COUNTER / TIMER REGISTERS

Table 28: Counter / Timer Registers

Mnemonic	R/W	Address	Name
T3CNT	R/W	0044h	Timer 3 Count Load/Read
T4CNT	R/W	0045h	Timer 4 Count Load/Read
T5CNT	R/W	0046h	Timer 5 Count Load/Read
TCW	W	0047h	Timer Control Word

OPERATION

Operational details for this industry standard 8254 type counter/timer chip are beyond the scope of this manual. Register details, operational modes, and programming information can be obtained from the VersaLogic website by downloading the 8254.PDF data sheet.

PC/104 Expansion Bus

The VSBC-6 will accept up to four PC/104 and/or three PC/104-*Plus* expansion modules. Both 3.3V and 5.0V modules are supported.

ARRANGING THE STACK

If PC/104-*Plus* modules will be used, they go on the stack first (closest to the VSBC-6 circuit board). The first module is called "slot 0", the next module is "slot 1", and the third module is "slot 2". Make sure to correctly configure the "slot position" jumpers on each PC/104-*Plus* module to match it's physical position in the stack.

The BIOS automatically configures the I/O ports and Memory map allocation, including allocation of interrupts.

PC/104 modules are stacked on top of the PC/104-*Plus* modules; 16-bit modules first followed by 8-bit PC/104 modules. Lastly, non-standard modules which lack feedthrough connectors should be assembled on top of the stack.

Note Some modules may require –12V and/or –5V for correct operation. Check that the proper connections to the 3-pin auxiliary power input connector (J1) are made if your expansion module(s) use these voltages. See pages 17 and 23 for details.

I/O CONFIGURATION

PC/104 Modules

PC/104 I/O modules should be addressed in the 100h – 3FFh address range. Care must be taken to avoid the I/O addresses shown in the *On-Board I/O Devices* table on page 54. These ports are used by on-board peripherals and video devices.

PC/104-Plus *Modules*

PC/104-*Plus* modules do not use CPU I/O addressing. No configuration is necessary except to jumper the expansion module for the correct stack position.

Memory and I/O Map

MEMORY MAP

The lower 1 MB memory map of the VSBC-6 is arranged as shown in the following table. CMOS setup is used to choose between DRAM and PC/104 for three sections of memory from 0C0000h to 0EFFFFh.

Various blocks of memory space between A0000h and FFFFFh can be shadowed. CMOS setup is used to enable or disable this feature.

Table 29: Memory Map

Start Address	End Address	Comment
F0000h	FFFFFh	System BIOS
E0000h	EFFFFh	Flash Page, System BIOS, DOC, BBSRAM, BIOS Ext.
CC000h	DFFFFh	PC/104
C0000h	CBFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	DRAM

I/O MAP

The following table lists the common I/O devices in the VSBC-6 I/O map. User I/O devices should be added in the 100h – 3FFh range, using care to avoid the devices already in the map as shown below.

Table 30: On-Board I/O Devices

I/O Device	Standard I/O Addresses	Alternate * I/O Addresses
Auxillary Counter/Timer Channels	44h – 47h	
Special Control Register	0E0h	1E0h
Watchdog Hold-Off Register/Revision Register	0E1h	1E1h
Digital Control / Analog Status Register	0E2h	1E2h
Map and Paging Control Register	0E3h	1E3h
Analog Control / ADC Low Register	0E4h	1E4h
ADC High Data Register	0E5h	1E5h
Digital I/O Low Data Register	0E6h	1E6h
Digital I/O High Data Register	0E7h	1E7h
Primary Hard Drive Controller	1F0h – 1F7h	
Secondary Hard Drive Controller	170h – 177h	
Ethernet **Note:** Address range 180h – 18Fh is used to "park" the Ethernet interface chip when the Ethernet port is disabled in CMOS Setup.	340h – 34Fh	180h – 18Fh 280h – 28Fh 300h – 30Fh 320h – 32Fh 360h – 36Fh 380h – 38Fh 3A0h – 3Afh
COM2 Serial Port	2F8h – 2FFh	
COM4 Serial Port	2E8h – 2EFh	
LPT1 Parallel Port	378h – 37Fh	
SVGA Video	3B0h – 3DFh	
COM3 Serial Port	3E8h – 3EFh	
Floppy Disk Controller	3F0h – 3F7h	
COM1 Serial Port	3F8h – 3FFh	

* User selectable via CMOS Setup.

Note Except for the Ethernet interface, the I/O ports occupied by on-board devices are freed up when the device is disabled in CMOS Setup.

Interrupt Configuration

The VSBC-6 has the standard complement of PC type interrupts. Ten non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines are automatically allocated as needed to PCI devices.

There are no interrupt configuration jumpers. All configuration is handled through CMOS setup. The switches in the diagram below indicate the various CMOS Setup options. Closed switches show factory default settings.

Note If your design needs to use interrupt lines on the PC/104 bus, we recommend using IRQ5, IRQ9, and/or IRQ10. Make sure to configure CMOS Setup with the chosen PC/104 interrupts. This prevents their allocation to PCI devices.

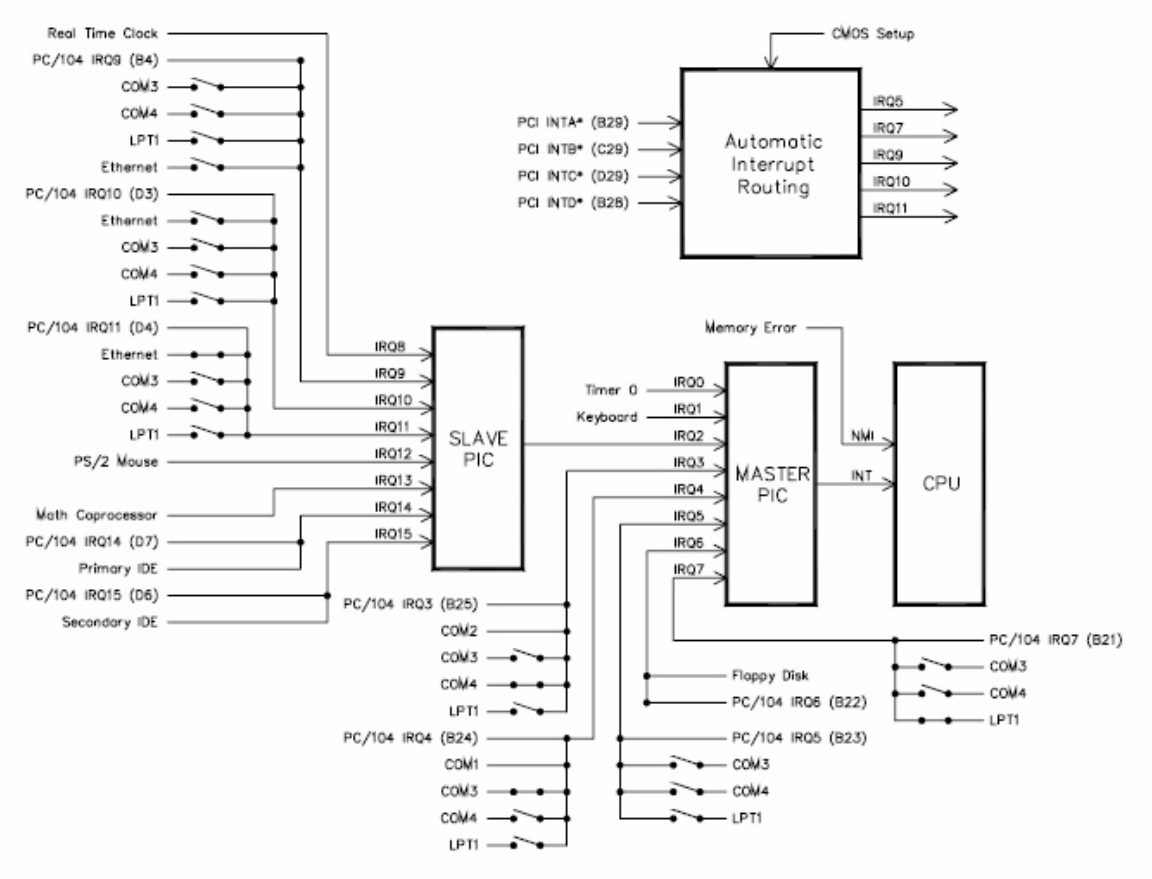


Figure 7. Interrupt Circuit Diagram

Special Control Register

SCR (READ/WRITE) 00E0h (or 01E0h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
LED	Reserved	REV	Reserved	COM1DIS	COM2DIS	ETHDIS	WDOGEN

Table 31: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	LED	**Light Emitting Diode** — Controls the programmable LED connector J7 LED = 0 Turns LED off. LED = 1 Turns LED on.
D6	—	**Reserved** — This bit has no function. Always reads as 1.
D5	REV	**Rev Indicator** — Indicates the board revision level. The system BIOS reads this bit to determine SDRAM support. REV = 0 Board revision 3.02 and earlier. REV = 1 Board revision 4.00 and above. ***Note!*** *This bit is a read-only bit.*
D4	—	**Reserved** — This bit has no function. Always reads as 1.
D3	COM1DIS	**COM1 Disable** — Enables and disables COM1. COM1DIS = 0 Enables COM1. COM1DIS = 1 Disables COM1.
D2	COM2DIS	**COM2 Disable** — Enables and disables COM2. COM2DIS = 0 Enables COM2. COM2DIS = 1 Disables COM2.
D1	ETHDIS	**Ethernet Disable** — Enables and disables the Ethernet port. ETHDIS = 0 Enables Ethernet port. ETHDIS = 1 Disables Ethernet port.
D0	WDOGEN	**Watchdog Enable** — Enables and disables the watchdog timer reset circuit. WDOGEN = 0 Disables the watchdog timer. WDOGEN = 1 Enables the watchdog timer.

Revision Indicator Register

REVIND (READ ONLY) 00E1h (or 01E1h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
PC6	PC5	PC4	PC3	PC2	PC1	PC0	REV0

This register is used to indicate the revision level of the VSBC-6 product.

Bit	Mnemonic	Description
D7-D1	PC6-PC0	**Product Code** — These bits are hard coded to represent the product type. The VSBC-6 will always read as 1111111. Other codes are reserved for future products. **PC6 PC5 PC4 PC3 PC2 PC1 PC0 Product Code** 1 1 1 1 1 1 1 VSBC-6 ***Note!*** *This bits are read-only.*
D0	REV0	**Revision Level** — These bits are represent the VSBC-6 circuit revision level. **REV0 Revision Level** 0 Rev 5 1 Rev 4 see REV bit in SCR. ***Note!*** *This bits are read-only.*

Watchdog Timer Hold-Off Register

WDHOLD (WRITE ONLY) 00E1h (or 01E1h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

A watchdog timer circuit is included on the VSBC-6 board to reset the CPU if proper software execution fails or a hardware malfunction occurs. The watchdog timer is enabled/disabled by writing to bit D0 of SCR

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (250 ms minimum). Writing a 5Ah to WDHOLD resets the watchdog timeout period, preventing the CPU from being reset for the next 250 ms.

Map and Paging Control Register

MPCR (READ/WRITE) 00E3H (or 01E3h via CMOS Setup)

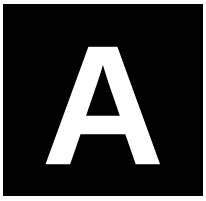
D7	D6	D5	D4	D3	D2	D1	D0
FPGEN	Reserved	SPGEN	Reserved	DPGEN	PG2	PG1	PG0

Table 32: Map and Paging Control Register Bit Assignments

Bit	Mnemonic	Description
D7	FPGEN	**FLASH Paging Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to the on-board FLASH memory. FPGEN = 0 FLASH page frame disabled. FPGEN = 1 FLASH page frame enabled. ***Note!*** *This bit is for factory use only. It is used to write user default CMOS setup values to FLASH and to upgrade the system BIOS. When FPGEN = 1, the Page Select bits are used to access various blocks within the FLASH.*
D6	—	**Reserved** — This bit has no function.
D5	SPGEN	**Battery Backed Static RAM Paging Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to an optional Dallas Semiconductor Battery-Backed Static RAM chip plugged into socket U22 (512KB max.) SPGEN = 0 BBSRAM page frame disabled. SPGEN = 1 BBSRAM page frame enabled. ***Note!*** *When SPGEN = 1, the Page Select bits are used to access various 64K blocks within the BBSRAM chip.*
D4	—	**Reserved** — This bit has no function.
D3	DPGEN	**DiskOnChip Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to the Disk on Chip DPGEN = 0 DOC page frame disabled. DPGEN = 1 DOC page frame enabled. ***Note!*** *The Page Select bits are not used when accessing the DOC.*
D2-D0	PG2-PG0	**Page Select** — Selects which 64K block of FLASH or BBSRAM will be mapped into the page frame at E0000h to EFFFFh **PG2 PG1 PG0 — Memory Range within FLASH or BBSRAM** 0 0 0 — 000000h to 00FFFFh 0 0 1 — 010000h to 01FFFFh 0 1 0 — 020000h to 02FFFFh 0 1 1 — 030000h to 03FFFFh 1 0 0 — 040000h to 04FFFFh 1 0 1 — 050000h to 05FFFFh 1 1 0 — 060000h to 06FFFFh 1 1 1 — 070000h to 07FFFFh

Note For proper operation, only one page enable bit (FPGEN, SPGEN, or DPGEN) should be set at a time.

Appendix A — Other References



PC Chipset *ALi Aladdin IV+ Chipset*	Acer Laboratories Inc., (www.acerlabs.com)
Ethernet Controller *LAN91C96 (formerly called SMC91C96)*	Standard Microsystems Corp., (www.smsc.com)
Video Controller *65550*	Asiliant Technologies Inc., (www.Asiliant.com)
A/D Converter *Maxim 197*	Maxim Integrated Products, (www.maxim-ic.com)
Disk On Chip *DOC2000*	M-Systems Inc., (www.m-sys.com)
PC/104 Specification *PC/104 Resource Guide*	PC/104 Consortium, (www.controlled.com/pc104)
CPU Chips	
K6 & K6-2	Advanced Micro Devices, (www.amd.com)
Pentium	Intel Corporation, (www.intel.com)
PC/104-*Plus* Specification *PC/104 Resource Guide*	VersaLogic Corp., (www.versalogic.com)
General PC Documentation *The Programmer's PC Sourcebook*	Microsoft Press, mspress.microsoft.com
General PC Documentation *The Undocumented PC*	www.amazon.com