Reference Manual

REV. 7/3/2017

SPX-3

CANbus Controller
Serial Peripheral Expansion
(SPX™) Board

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MSPX3

Product Release Notes

Rev. 1.1

- Updated Web links

Rev. 1

- Production release.

Support Page

The SPX support page, at **https://versalogic.com/products/DS.asp?ProductID=208**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Data sheets and manufacturers' links for chips used in this product
- Utility routines and benchmark software

This is a private page for SPX users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

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Introduction 1

Description

The VersaLogic SPX-3 is a CANbus expansion module designed to be used with any SPX™ enabled base board. Its features include:

- Microchip MCP2515 CAN controller, 2.0B (PeliCAN compatible) at 1 Mbit/s
- Microchip MCP2551 CAN transceiver, meets or exceeds all ISO11898-2 standards
- 0-8 byte length in the data field
- Standard 11-bit ID and 29-bit ID extended data frames
- Two receive buffers with prioritized message storage
- Six 29-bit filters
- Two 29-bit masks
- Three transmit buffers with prioritization
- Software configurable hardware interrupt

VersaLogic SPX boards are a line of I/O expansion boards using the industry standard Serial Peripheral Interface (SPI) bus. These are small 1.2" x 3.775" boards that can be mounted on the PC/104 and PC/104-*Plus* stack using normal standoffs. They can also mount up to two feet away from the base board using custom cabling.

SPX boards are electrically connected to a base board via a 14-pin 2 mm cable. Up to four boards can be daisy-chained together. The SPI bus requires each chip to have a discrete chip-select signal, and the 14-pin interface supplies four chip-select signals. The maximum clock rate is 8 MHz.

Power for SPX boards is supplied through the interface cable. I/O connections on SPX boards are provided through screw terminal/wire connections.

All SPX boards are RoHS compliant and industrial temperature rated.

About SPI

The SPI bus specifies four logic signals: SCLK – Serial clock (output from master); MOSI – Master output, slave input (output from master); MISO – Master input, slave output (output from slave); and SS – Slave select (output from master).

The SPI implementation on VersaLogic CPU boards adds additional features, such as hardware interrupt input to the master. The master initiates all SPI transactions. A slave device responds when its slave select is asserted and it receives clock pulses from the master.

Slave selects are controlled in one of two modes: manual or automatic. In automatic mode, the slave select is asserted by the SPI controller when the most significant data byte is written. This initiates a transaction to the specified slave device. In manual mode, the slave select is controlled by the user and any number of data frames can be sent. The user must command the slave select high to complete the transaction.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. All four common SPI modes are supported through the use of clock polarity and phase controls.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 1.2" x 3.775"; SPX compliant
Storage Temperature: -40° C to 85° C
Free Air Operating Temperature:
-40° C to +85° C
Power Requirements:
+5.0V ± 5% @ 25.04 mA (125.2 mW), (CANbus idle) typ., 100.04 mA (500.2 mW) max.
(Interface cable provides 500 mA total, to be shared by all SPX modules)
CANbus:
CAN V2.0B at 1 Mbit/s
Standard 11-bit ID and 29-bit ID extended data frames
Two receive buffers with prioritized message storage
Six 29-bit filters
Two 29-bit masks
Three prioritized transmit buffers
112 max number of nodes
Minimum bit rate: 15 kbps
Maximum bit rate: 1.0 Mbps*
CANH, CANL Vmax: +40V, -40V
Fundamental Oscillator: 24 MHz
Compatibility:
SPX – Full compliance
(Any 3.3V signaling SPI interface, 8 MHz maximum clock)
Weight:
0.0xx lbs (0.0xx kg)
Compliance:
RoHS – Full compliance
CANopen – minimum bit rate: 15 kbps
SAE J1939

Specifications are subject to change without notice.

RoHS-Compliance

The SPX-3 is RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

Electrostatic Discharge

Electrostatic discharge (ESD) can damage boards, disk drives, and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Technical Support

If you are unable to solve a problem with this manual please visit the SPX Product Support web page listed below. If you have further questions, contact VersaLogic technical support at (503) 747-2261. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

SPX Support Website

https://versalogic.com/products/DS.asp?ProductID=208

Repair Service

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261. VersaLogic's standard turn-around time for repairs is five working days after the product is received.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contact if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

SPX-3 Board Layout

The figure below shows the dimensions of the SPX-3 board, as well as the location of connectors, jumpers, and mounting holes.

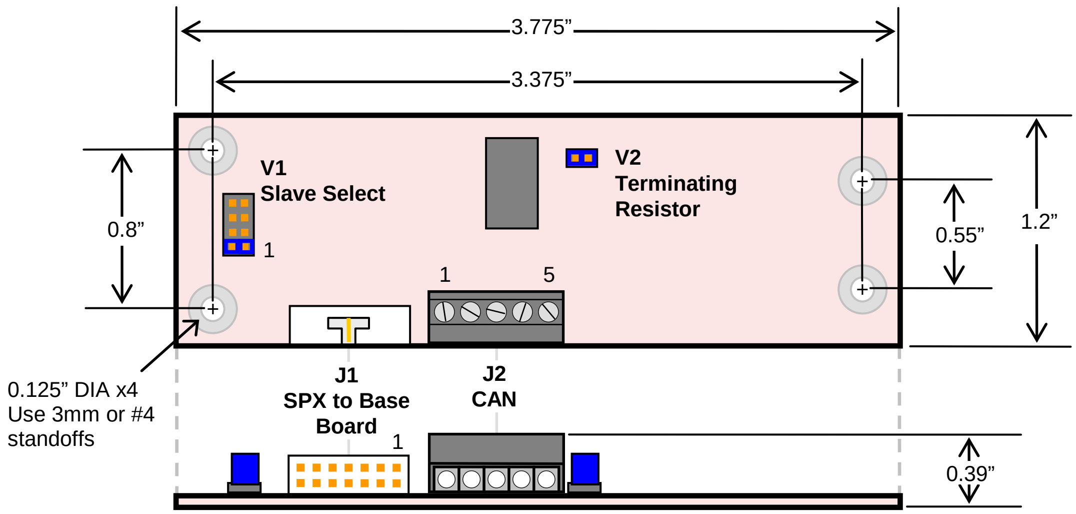

Figure 1. SPX-3 Board Layout
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The SPX-3 mounts on two hardware standoffs using the corner mounting holes. These standoffs are secured to the board, typically across the PC/104 and PC/104-*Plus* stack locations, using pan head screws, shown in Figure 2.

Standoffs and screws are available as part number VL-HDW-101.

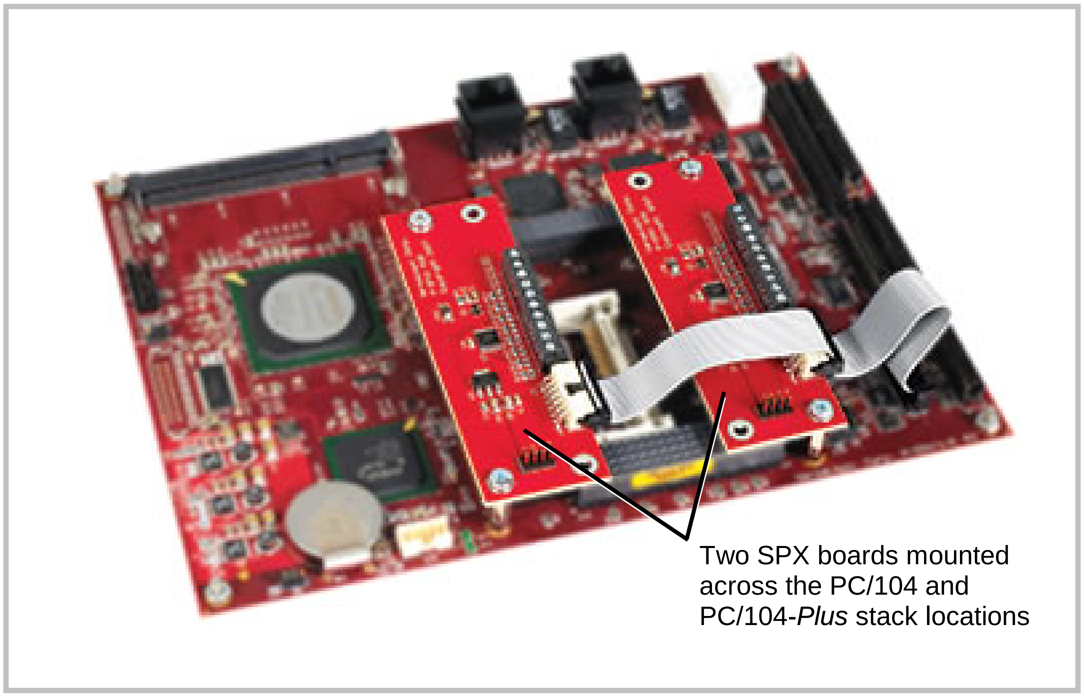

Figure 2. SPX Board Mounting

Connector Functions and Interface Cables

The following table shows the function of each connector, as well as mating connectors and cables.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description
J1	SPX to Base Board	FCI 89361-714LF or equivalent	CBR-1401 CBR-1402	2 SPX Module Cable 4 SPX Module Cable
J2	CANbus	Bare wires to 5-pin screw terminal	–	16-28 AWG wire

Jumper Summary

Table 2: Jumper Summary

Jumper Block	Description	As Shipped
V1[1-2]	Slave Select 0	In
V1[3-4]	Slave Select 1	Out
V1[5-6]	Slave Select 2	Out
V1[7-8]	Slave Select 3	Out
V2	Termination	In

J1 Connector Pinout

Table 3: J1 Connector Pinout

Pin	Signal Name	Description
1	V5_0	+5.0V
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Master In Slave Out
5	GND	Ground
6	MOSI	Master Out Slave In
7	GND	Ground
8	SS0#	Slave Select 0
9	SS1#	Slave Select 1
10	SS2#	Slave Select 2
11	SS3#	Slave Select 3
12	GND	Ground
13	SINT#	SPI Interrupt
14	V5_0	+5.0V

CANbus 3

Description

The CAN system is constructed according to the OSI layered communications model. The SPX-3 provides the data-link and physical layers for a CAN V2.0B interface that operates at speeds of up to 1 Mbit/s. In this manual, usage of the SPX-3 will be described in consolidation of these two layers.

The SPX-3 CANbus interface is implemented using the Microchip MCP2515 CAN controller and MCP2551 high-speed CAN transceiver. For detailed information on these chips, refer to their respective data sheets.

CAN is a multi-node half-duplex bus system that utilizes Station ID numbers to represent each node. To transmit data, the transmitting node assembles a data frame, which begins with the recipient's Station ID and is followed by up to eight bytes of data payload, and then an acknowledge period during which the receiving node transmits an acknowledge bit when the frame is transmitted onto the bus. There are also utility bits within the frame, not mentioned here, that are used by the nodes to process the frame. See the MCP2515 datasheet for more detailed information about CAN frames. When a frame is received, the node compares the Station ID to sets of masks and filters to determine if it should accept the frame payload, or discard it. Filters and masks can be set up to accept ID-specific frames, all frames (broadcast), or subnet (similar to Ethernet). The figure below shows a typical CAN network.

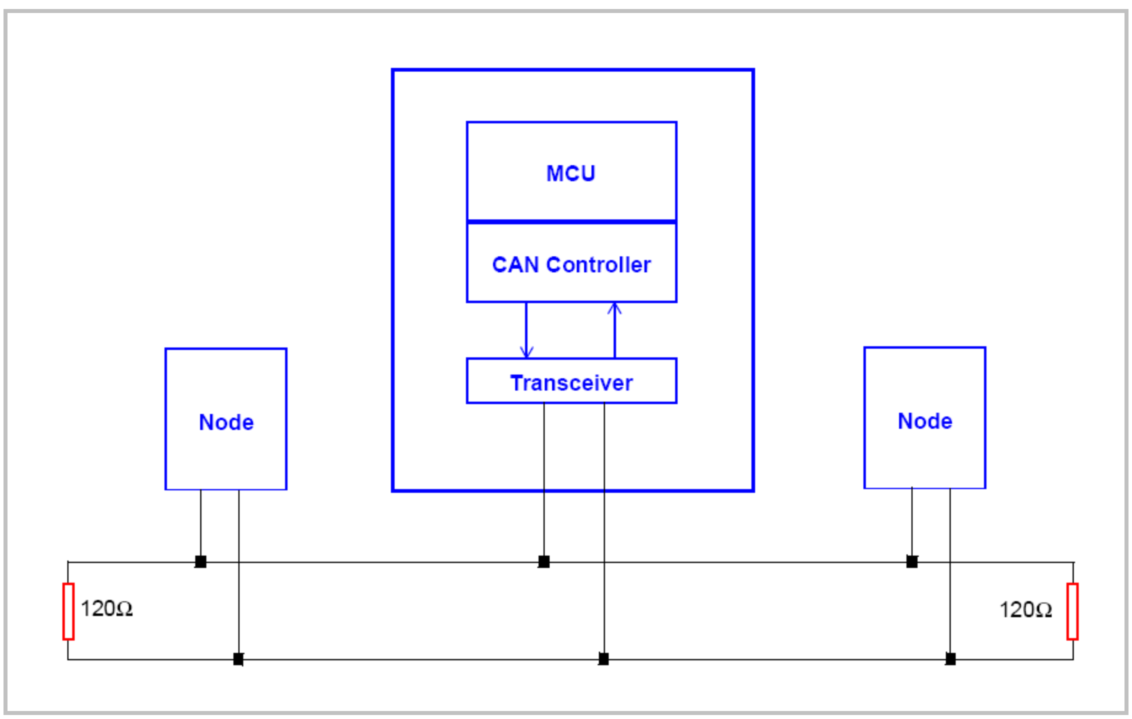

Figure 3. Typical CAN Network

CAN NETWORK CONFIGURATION

When setting up a CAN network, the bit timing is critical. Each node may operate with its own oscillator base frequency that can differ in value from other nodes on the bus. The CAN controller has configuration settings to “normalize” the oscillator frequency to produce a Nominal Bit Time that must be common to all nodes on the bus. Microchip’s application note, AN754, describes in detail the aspects of CAN bit timing as does the MCP2515 datasheet. The normalized oscillator period is abstracted to discrete Time Quanta (TQ). TQs are then used as the base time unit for constructing the Nominal Bit Time in several distinct segments. These segments are used for bus synchronization and cover for the differences in node oscillator base frequencies and bus length. The figure below shows a CANbus bit as constructed from its base oscillator.

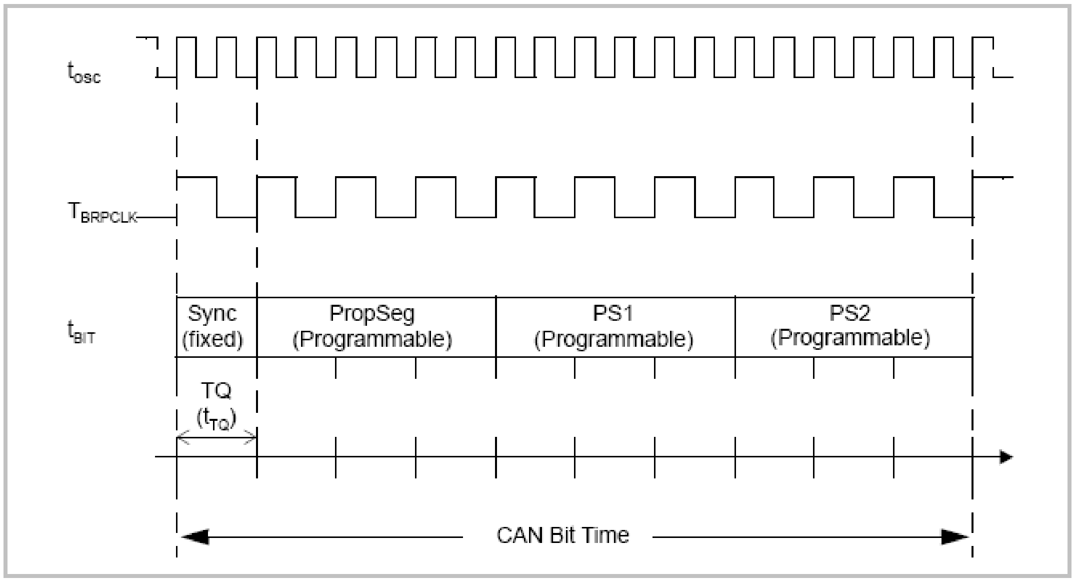

Figure 4. CANbus Bit

The next aspects to consider for setting up the CAN network are Station IDs, masks and filters. The MCP2515 allows the use of Extended IDs, increasing the ID size to 29 bits. This gives the network designer greater flexibility for setting up subnets and organizing data flow. The masks and filters are set up similarly to the receive buffer register layout and work on either an 11-bit ID or the 29-bit ID regardless of the type of data frame received. Systems can use any combination of Standard IDs and Extended IDs for nodes in the same network. The masks and filters work as shown in Table 4.

Table 4: CAN Masks and Filters

ID Mask Bit	ID Filter Bit	Station ID Bit	Accept/Reject
0	X*	X	Accept
1	0	0	Accept
1	0	1	Reject
1	1	0	Reject
1	1	1	Accept

* X = Don't care.

EXTERNAL CONNECTIONS

CANbus is transmitted through connector J2 of the SPX-3 as shown in the following table.

Table 5: CAN Connectors

J2 Pin	Signal Name	Description
1	NC	No connection
2	CANH	CAN high-level bus signal
3	CANL	CAN low-level bus signal
4	NC	No connection
5	Ground	Ground

USING CANBUS

Communicating on the CAN bus with the SPX-3 is handled through sets of transmit and receive buffers within the MCP2515 CAN controller. To transmit a message, one of the three transmit buffers is selected (the lowest numerical buffer, TXB0, has the highest priority) and the recipient Station ID is loaded first, followed by up to eight bytes of data. To initiate a transfer, a Request-To-Send command is sent to the SPX-3, and if the bus is idle, an appropriate CAN data frame will be transmitted on the bus. If an error is encountered, an error frame may be transmitted by the remote node indicating so. Reads to the MCP2515 Status and Error Flag Registers can help pinpoint the problem. Note: If not operating in One-Shot Mode, a frame will be retransmitted continuously until a valid acknowledge is received by any node on the bus. A good indication of a mismatch in Bit Time between nodes is the presence of acknowledge errors.

Message reception is done by reading the appropriate receive buffer when it contains a valid message. The receive buffer, RXB0, has the higher priority. A valid message is one that has successfully passed through the bit masks and filters of the receiver. Any other CAN frames are discarded. Notice of a valid message in a receive buffer can be found by polling the Main or Receive Status Registers or configuring the MCP2515 to generate an interrupt according to desired conditions.

The MCP2551 CAN transceiver has a "slope control" capability to adjust the slew rate of the CANbus signaling for operation in extremely noisy environments. This setting is controlled by the use of a resistor, R1, on the SPX-3 (Rs in the MCP2551 datasheet). The default setting is "High-Speed": R1 is a 0805 zero-ohm resistor connected to ground. R1 can be replaced with another 0805 resistor of a desired value to utilize the Slope Control feature. See the MCP2551 datasheet for more information.

INTERRUPT SELECTION

The SPX-3 has a hardware interrupt capability that involves configuring the MCP2515 to choose among eight sources from which to generate an interrupt. More than one interrupt source is possible. After this is set, an IRQ can be assigned and enabled in the SPISTATUS register (I/O address 0x1D9 of EBX-11 Rev. 6.xx or later). Note that all SPI device hardware interrupt signals are wire-OR'd on the base board, including on-board devices and SPX expansion modules. The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ. Care must be given to ensure the interrupt is handled as intended.

PROGRAMMING NOTES

The Microchip MCP2515 CAN controller SPI interface has a range of different commands designed to take full advantage of its abilities. The VersaLogic SPX controller in its current revision (EBX-11 Rev 6.xx) fully supports all of these commands. In EBX-11 Rev 5.xx and below the Bit Modify command, the Load TX Buffer instruction, and Read RX Buffer instructions were not supported, but all other commands were. These operations can be performed using normal register read and write instructions. The effects of missing these commands are primarily an inconvenience to the programmer, but may affect throughput of very large data payloads due to the extra overhead required for single register SPI read/writes. The EBX-11 Rev. 6.xx compatible SPX interface incorporates features that allow the use of the full command set of the MCP2515, and is recommended. Driver support is also planned for future release.

The SPX-3 incorporates the MCP2515 using an SPI-only configuration. The MCP2515 pins CLKOUT, TX0RTS, TX1RTS, TX2RTS, RX0BF, and RX1BF pins are not connected.

SPI INTERFACE

All CANbus instructions are sent and received by the base board using the base board's SPX interface. The VersaLogic SPI implementation (SPX interface), employs four 8-bit data registers, SPIDATA3-0. Writing the MSB to the SPIDATA3 register triggers the SPI transaction. See Appendix A for more information about base board registers.

The MCP2515 operates in SPI Mode 0,0 (SCLK idle low, valid data on rising edge) or mode 1,1 (EBX-11 Rev. 6.xx SPX mode 1,0). Frame lengths vary from 8 bits to 32 bits according to the instruction. MCP2515 instructions are shown in Table 6 along with their respective frame lengths.

Table 6: CAN Controller Instructions

MCP2515 SPI Instruction	SPI Frame Length	MSB Format	Middle Byte	Middle Byte	LSB
Reset	8-bit	0xC0	N/A	N/A	N/A
Read	24-bit	0x03	Register Address	Data Out	N/A
Read Rx Buffer	8-bit manual	1001 0nm0**	N/A	N/A	N/A
Write	24-bit	0x02	Register Address	Data to Write	N/A
Load Tx Buffer	8-bit manual	1001 0abc**	N/A	N/A	N/A
RTS	8-bit	1000 0nnn*	N/A	N/A	N/A
Read Status	16-bit	0xA0	Data Out	Repeat Data Out	N/A
RX Status	16-bit	0xB0	Data Out	Repeat Data Out	N/A
Bit Modify	32-bit	0x05	Register Address	Mask Value	Data Value

* The digit selected determines which transmit buffer to send. 0, 2, or 4 send TXB0, TXB1, or TXB2 respectively. Only one digit may be used.

** Buffer address is selected according to bits n, and m in the case of Rx buffers and a,b, and c in the case of Tx buffers. Only one buffer is used at a time.

For detailed information regarding the MCP2515 setup and usage, refer to the MCP2515 datasheet and higher OSI layer CAN protocol specification (if used).

Base Board SPI Registers

A

The following tables describe the SPI control and data registers of the EBX-11 Rev. 6.00 and later. This is the standard set of SPI registers for VersaLogic CPU boards with an SPX interface. See the reference manual for details and updates.

SPICONTROL (READ/WRITE) 1D8h

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 7: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge
D5-D4	SPILEN	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes. **SPILEN1 SPILEN0 Frame Length** 0 0 8-bit 0 1 16-bit 1 0 24-bit 1 1 32-bit
D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (1DDh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual
D2-D0	SS	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the base board will be directly controlled by these bits when MAN_SS = 1. **SS2 SS1 SS0 Slave Select** 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, J17 pin-8 0 1 0 SPX Slave Select 1, J17 pin-9 0 1 1 SPX Slave Select 2, J17 pin-10 1 0 0 SPX Slave Select 3, J17 pin-11 1 0 1 On-Board A/D Converter Slave Select 1 1 0 On-Board Digital I/O Ch 0-Ch 15 Slave Select 1 1 1 On-Board Digital I/O Ch 16-Ch 31 Slave Select

SPISTATUS (READ/WRITE) 1D9h

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 8: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10 **Note:** The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts (see **Error! Reference source not found.**).
D5-D4	SPICLK	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPI Data Registers

SPIDATA0 (READ/WRITE) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) 1DBh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) 1DCh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) 1DDh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit use the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.