VL-486-3

Single Board Industrial CPU
Card for the STD 32 Bus

M486-3

VL-486-3

486SXLC Single Board Industrial Computer
for the STD 32 Bus

REFERENCE MANUAL

Doc. Rev. 07/96

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Table of Contents

Other References

Chips and Technologies, Inc., (408)434-0600,
82C836 Chipset Data Book

Chips and Technologies, Inc., (408)434-0600,
82C721 Universal Peripheral Controller II Data Book

STD Manufacturers Group, (408)723-5083,
STD 32 Bus Specification and Designer's Guide

Texas Instruments (214)917-1264,
TI486SXLC2 *Data Book*

Microsoft Press, (800)677-7377,
The Programmer's PC Sourcebook

Addison-Wesley, (617)944-3700,
The Undocumented PC

Overview 1

This chapter introduces the VL-486-3 CPU card, lists its features and specifications, and provides a brief overview of the installation and configuration process.

Using This Manual

Each chapter in this manual corresponds to a step in the installation process:

- Chapter 1, “Overview,” lists basic information about the CPU card, specifications, and system requirements. Use this chapter to familiarize yourself with the card and it’s capabilities.
- Chapter 2, “DOS Based Quick Start,” describes how to quickly get your DOS based system set up and running using a VL-486-3 CPU card.
- Chapter 3, “Configuration” describes how to jumper and initialize the CPU card.
- Chapter 4, “Installation,” describes how to install the VL-486-3. It also provides details on the external connections.
- Chapter 5, “Register Descriptions,” lists all the user-programmable registers on the CPU card.
- Appendix A, “Schematics” shows the circuit diagrams on the CPU card.

Introduction

The VL-486-3 CPU card features a 32-bit, 50 MHz, clock doubled 486SXLC microprocessor, up to 8MB RAM, up to 1MB Flash EEPROM or EPROM, two COM ports, one LPT port, IDE hard disk interface, floppy disk interface, and real time clock. The card can be used as a DOS or non-DOS computer in either STD 80 or STD 32 Bus systems.

PC/AT Compatibility

Standard I/O and peripheral interfaces and optional onboard firmware, containing BIOS, self tests, and a setup utility, bring a full-function PC/AT compatible computer to the STD Bus form factor.

STD Bus Compatibility

The VL-486-3 CPU card complies with certain subsets of the STD 32 Bus specification that allow it to communicate with STD 80 compatible 8-bit and STD 32 compatible 16-bit I/O and memory cards. In addition, the card fully complies with the STD 80 Bus specification using a bus speed of 8.33 MHz. The CPU card is compatible with all I/O and memory cards that adhere to STD 80 specifications.

ON-BOARD MEMORY

RAM Four 42-pin SOJ JEDEC compatible sockets accept up to four 1M x 16 dynamic RAM chips to provide a total of 2M, 4M, 6M or 8M of 16-bit system memory. The use of 1M x 18 RAM chips will provide parity error detection if desired.

ROM Two 32-pin PLCC JEDEC compatible sockets accept one or two high density memory components including 128K x 8, 256K x 8, and 512K x 8 EPROMs and Flash EPROMs. You can start out with one device, and add a second one when your storage requirements grow. A Flash File System is available to make the Flash device(s) appear as a bootable disk drive.

HARD DISK DRIVE AND FLOPPY DISK DRIVE INTERFACES

A 40-pin IDE hard disk drive interface and a 34-pin floppy disk drive interface are included on the VL-486-3 card for connection to industry standard IDE hard drive(s) and PC/AT style floppy drive(s) (5¼” or 3½”). Each interface supports two drives.

COM PORTS

The two on-board COM ports are hardware and software compatible with the PC/AT architecture. Baud rates are programmable from 50 baud to 115K baud. COM1 is a standard RS-232 interface, COM2 can be jumpered as an RS-232 or RS-485 port.

PARALLEL PORT

The bidirectional parallel port can be used as a standard PS2 compatible LPT port or as 17 general purpose TTL I/O signals. Each output line has a 24 ma current sink rating. Eight of the signals are programmable as a group for input or output, three are dedicated output, and five are dedicated inputs. A strobe signal, which produces a 50 µs pulse under program control, is also available as an output.

COUNTERS/TIMERS

The VL-486-3 card includes three 8254 type 16-bit counter/timers. One channel provides timing for dynamic RAM refresh, one channel generates an 18.2 ms DOS interrupt, and another channel is used to drive the speaker. All channels are available for general purpose timing and periodic interrupt sources if they are not being used by an operating system.

The counter/timers are provided by the 82C836 Integrated Peripherals Controller chip.

REAL TIME CLOCK WITH CMOS RAM

A battery-backed 146818 compatible real time clock (RTC) provides accurate date and time functions. This PC/AT compatible RTC also contains 128 bytes of battery-backed CMOS RAM with 114 bytes available as a system resource to store standard DOS setup parameters. Normally, DOS requires 51 bytes, leaving 63 bytes for general purpose use.

INTERRUPT CONTROLLERS

Two PC AT compatible 8259 type programmable interrupt controllers (PICs) are provided for full MS-DOS functionality. Interrupt sources and destinations can be configured with jumper blocks. Interrupt lines connect to on-card sources, STD Bus sources, and to a user connector.

DMA CONTROLLERS

The VL-486-3 has two DMA controllers which provide eight DMA channels. One channel is used for floppy disk data transfers, and a second (8- or 16-bit) channel is available for general purpose use through a front-plane user connector. The remaining six channels are accessible only by software.

WATCHDOG TIMER

A 1232 type watchdog timer provides a degree of protection against hardware and software failures. When the watchdog timer is enabled, it must be periodically updated by software at least every 250 ms. A system failure which prevents updating will reset the CPU.

Technical Specifications

Size:

Meets all STD 80 and STD 32 Bus mechanical specifications

Storage Temperature:

-40 °C to 85 °C

Free Air Operating Temperature:

0 °C to 65 °C

Power Requirements: *(with 8 MB RAM and 1 MB Flash installed)*

5V ±5% @ 800 ma

System Reset:

V_{CC} sensing, resets below 4.7V

Watchdog reset (jumper option)

LPT1/Parallel Interface:

IBM AT and PS/2 Compatible (Bidirectional)

Data Lines:

Output low voltage: 0.5V @ 24 ma
Output high voltage: 2.4V @ -12 ma

Control Lines:

Output low voltage: 0.5V @ 24 ma
Output high voltage: 2.4V @ -150 µA

COM1 & COM2 Interfaces:

IBM AT and PS/2 Compatible

Floppy Disk Drive Interface:

IBM AT and PS/2 Compatible

Hard Disk Drive Interface:

IBM AT and PS/2 Compatible (IDE)

Memory Sockets:

RAM:

Four sockets (sequentially addressed):
42-pin SOJ JEDEC; 1Mx16, or 1Mx18 Dynamic RAM

ROM:

Two sockets (64K paged):
32-pin PLCC JEDEC; 128x8, 256x8, 512x8 KB EPROMs or Flash EEPROMs

Memory Speed: (on-board):

RAM: 70 ns
EPROM and Flash EEPROM: 200 ns or faster

Bus Compatibility:

STD 80: Full compliance, 8.33 MHz bus speed
STD 32: Permanent Master; SA16, SA8-I, MB, MX
STD 32: Temporary Master; SA16, SA8-I, MB, {MX}

Specifications are subject to change without notice.

Technical Support

If you have problems that this manual can't help you solve, contact VersaLogic for technical support at **1-800-824-3163**.

DOS Based Quick Start 2

This chapter describes how to quickly get your DOS-based system set up and running using the VL-486-3 CPU card.

Introduction

A minimum DOS based run time system requires the CPU card, a BIOS, and a boot device (flash file system, floppy drive, or hard drive) containing an operating system and an application program. In many cases a video card, keyboard and monitor are added to this list, however, the VL-486-3 does not demand their presence in order to boot.

When a hard drive or 5¼” floppy disk is used, it is necessary to configure the startup information stored in CMOS RAM. The most convenient method of setting up this information is by using a keyboard and monitor (requires addition of a video card), however, a method is available to use COM2 to interact with the setup program.

Typical components of a DOS based system include:

- VL-486-3 CPU Card
- STD or STD 32 Card Cage
- One or two Floppy Disk Drives (3½” or 5¼”)
- One or two IDE Hard Disk Drives
- Standard PC/AT keyboard
- Video/Keyboard Card
- Video Monitor
- Power Supply

Installation

Before installing the VL-486-3 CPU card in a card cage, you must confirm that the on-card battery is activated.

Caution Electrostatic discharge (ESD) can damage cards, disk drives, and other components. Do the installation procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part on the card cage.

Cards can be extremely sensitive to ESD and always require careful handling. After removing the card from its protective wrapper or from the card cage, place the card on a grounded, static-free surface, component side up. Use an anti-static foam pad if available, but not the card wrapper. Do not slide the card over any surface.

The card should also protected during shipment or storage with anti-static foam or bubble wrap. To prevent damage to the lithium battery, do not use black conductive foam or metal foil.

Warning! The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Activating the Battery

The VL-486-3 CPU card is shipped with the battery disconnected. Since the battery provides backup power to the CMOS RAM and the real time clock circuits when the card is powered down, the battery must be activated before putting the card in service.

To activate the battery, move jumper V4 to position [2-3] (bottom position) as shown on page 21.

Jumper Locations

Note Jumpers and resistor packs shown in as-shipped configuration.

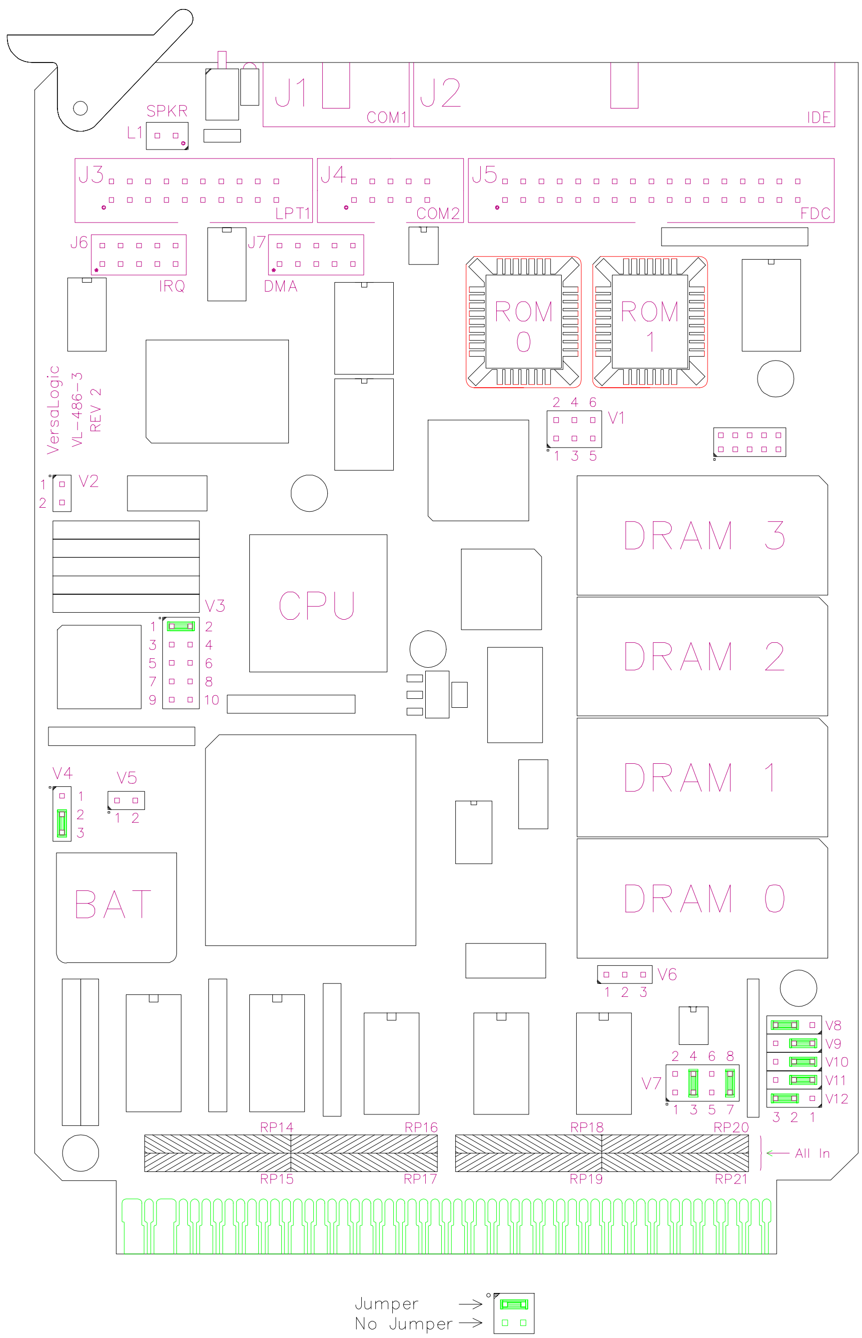


Figure 1. VL-486-3 CPU Card Layout

Card Installation

A typical VersaLogic DOS based system consists of an eight-slot V32-08T Card Cage, populated with:

- VL-486-3 CPU Card
- VL-FD1-1 Floppy Disk Drive Card
- VL-HD1-131 or VL-HD1-210 Hard Disk Drive Card
- VL-SVGA-1
- PC/AT Compatible Keyboard

Warning! To prevent damage, cards should be inserted in and removed from the card cage only when the system power is off.

Caution To avoid damaging cards, they must be oriented correctly (usually with the card ejector toward the top of the card cage.) Refer to the card cage documentation for the correct way to insert STD Bus cards.

For proper disk drive cable layout, the CPU card must be located between the disk drive cards. The hard disk drive card(s) must be installed to the right of the CPU card and the floppy disk drive card (if used) to the left. It does not matter what position the video card is installed in.

Table 1: Recommended Card Positions.

Slot #	Card	Part Number
0	Floppy Disk	VL-FD1
1	CPU	VL-486-3
2	Hard Disk	VL-HD1-xxx
Any	Video Card	VL-SVGA-1

Monitor and Keyboard Installation

A VGA monitor and IBM-AT compatible keyboard should be connected to the VL-SVGA-1 card as shown .

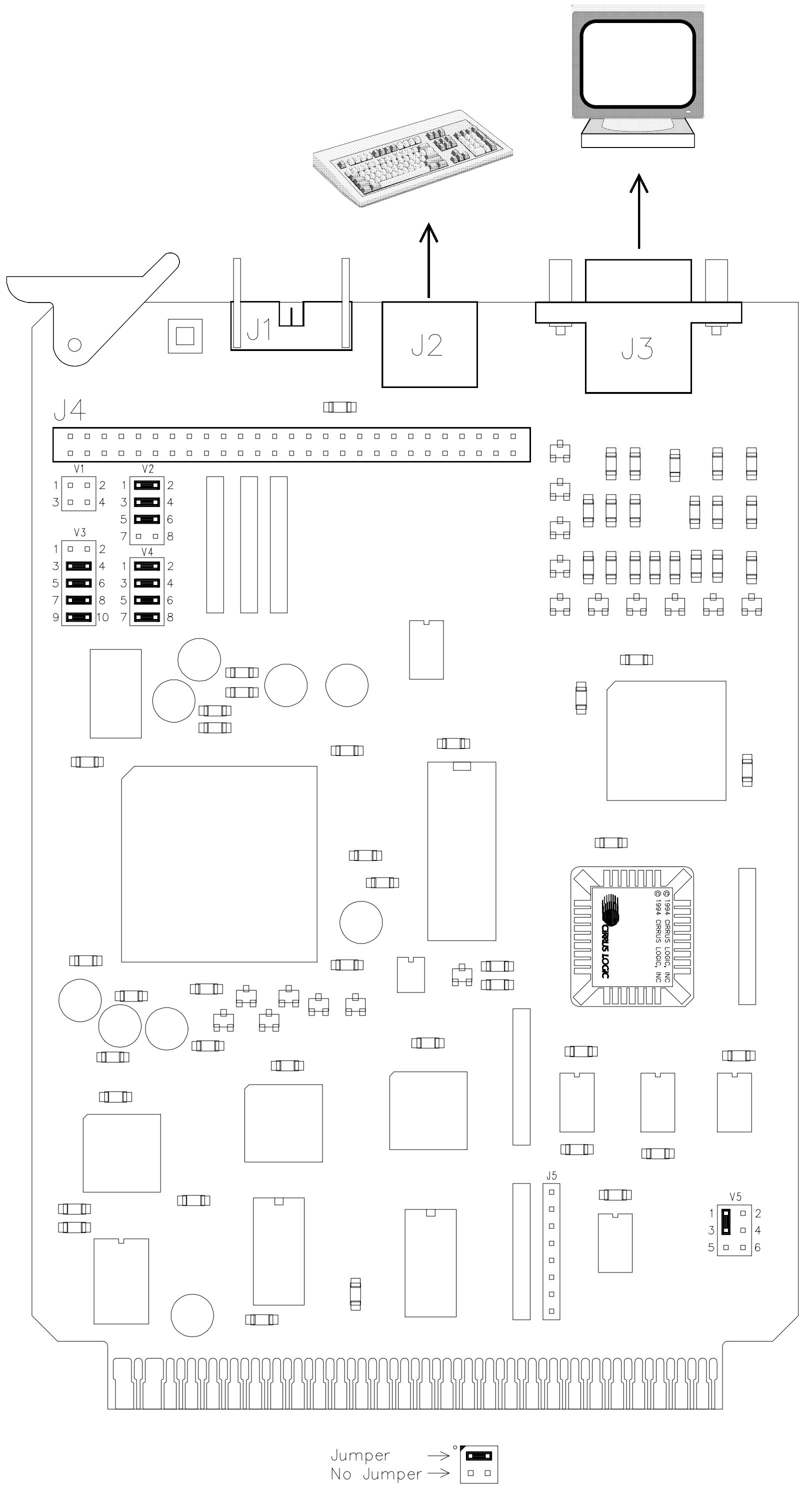


Figure 2. Jumpers/Connections for a VL-SVGA-1 Using a VGA Monitor

Cable Installation

To bring the header connectors on the VL-486-3 CPU card out to standard PC/AT style pinouts, the VersaLogic cable assemblies listed below are required.

Table 2: Cable Assemblies.

Connector	Part #	Description	Connects to:
J1 COM1	9575	1 ft. 10-pin IDC to DB-9P	External equipment (e.g., modem)
or	9551	6 ft. 10-pin IDC to DB-25S (Null Modem)	DTE device (e.g., host PC)
J2 IDE	9578	3 in. 40-pin IDC to 40-pin IDC	IDE hard disk drive
J3 LPT1	9576	1 ft. 20-pin IDC to DB-25S	External printer
J4 COM2	9575	1 ft. 10-pin IDC to DB-9S	External equipment (e.g., modem)
J5 FDC	9577	8 in. 34-pin IDC to 34-pin IDC	Floppy disk drive
J6 IRQ	N/A		Miscellaneous user circuitry
J7 DMA	N/A		Miscellaneous user circuitry
L1 Speaker	N/A		External 8Ω speaker

CMOS RAM Setup

The VL-486-3 CPU card uses battery-backed, non-volatile CMOS RAM provided by the real time clock chip to store system configuration settings. You can change these system settings with the Setup program (accessed manually at system boot.) The configuration information is read by the CPU upon system reset.

The Setup program is permanently stored in ROM, and can be run with or without an operating system present. To run Setup, reset the CPU card and press the `DEL` key when prompted.

Select "`BASIC CMOS CONFIGURATION`" to display a summary of the information stored in the CMOS RAM. To change the values shown you must enter new information. Use the cursor keys to move the highlight bar to the desired entry field, the press the `–` or `+` keys to change the values.

When you are finished, exit to the main Setup menu and select "`WRITE TO CMOS AND EXIT`" to save the changes and exit the Setup program.

CMOS Setup Options

MAIN CMOS SETUP MENU

SYSTEM BIOS SETUP - UTILITY VERSION 2.001.xxx (C) 1994-1996 VERSALOGIC, CORP. ALL RIGHTS RESERVED
BASIC CMOS CONFIGURATION ADVANCED CMOS CONFIGURATION IDE HDD AUTO DETECTION RESET CMOS TO LAST KNOWN VALUES RESET CMOS TO FACTORY DEFAULTS WRITE TO CMOS AND EXIT EXIT WITHOUT CHANGING CMOS
<ESC> TO CONTINUE (NO SAVE)

BASIC CMOS CONFIGURATION

This option goes to another menu which allows you to change the following:

- Date, Time
- Floppy Drive and Hard Drive types
- Console (VGA Card or Serial Port)

ADVANCED CMOS CONFIGURATION

This option goes to another menu which allows you to change the following:

- Memory Caching
- Boot Sequence
- Remote Disk
- Floppy Disk Drive Reset
- Information Displays
- Keyboard Parameters
- Memory Tests and Parity

IDE HDD Auto Detection

This option automatically sets the hard disk drive parameters.

It guides you through the process of reading the factory programmed values for heads, cylinders, and sectors in each attached IDE drive. The information is transferred to the *Basic CMOS Configuration* screen.

This option is included to make system setup easier. Use it instead of specifying the parameters manually.

Note This function may not work on older style IDE hard disk drives.

Reset CMOS to Last Known Values

This option acts like an undo function. It reverts all changes made in the *CMOS Setup Screens* to the values they had when Setup was first entered.

Reset CMOS to Factory Defaults

This option overwrites all information contained in the CMOS RAM with predefined parameters stored in the BIOS ROM, and reboots the CPU card.

The following parameters are loaded into CMOS RAM when this option is selected:

Table 3: Factory Default CMOS Parameters.

Date:	Jan 01, 1980
Time:	00:00:00
Floppy Drive A:	1.44MB 3½" or FLASH*
Floppy Drive B:	Not Installed
Hard Disk C: Type:	Not Installed
Hard Disk D: Type:	Not Installed
Console:	VGA/Keyboard or COM2†
Boot Sequence:	A: → C:
Seek Floppy at Boot:	Disabled
Numlock State at Boot:	Disabled
Display “Hit <Del>...”	Enabled
System Configuration Box	Enabled
Wait for F1 on Error	Disabled
Memory Parity Check	Disabled
Memory Test Tick	Enabled
Test Above 1M	Enabled
System BIOS Shadow	Disabled
Video BIOS Shadow	Disabled
Typematic Programming	Enabled
Typematic Rate Delay	250 ms
Typematic Rate	30 cps

* Regular BIOS (part no. 9620) defaults to 1.44MB 3½".
Flash File System BIOS (part nos. 9621 and 9622) default to FLASH.

† Permanent master defaults to **VGA/Keyboard**
Temporary master and dual master defaults to **COM2**

WRITE TO CMOS AND EXIT

This option updates the CMOS RAM with the information in the *CMOS Setup Screens*. After writing, the CMOS checksum is updated and the CPU card is rebooted.

EXIT WITHOUT CHANGING CMOS

This option acts like a cancel function. Use it to exit Setup without changing CMOS RAM.

Hard Disk Drive Parameters

All VersaLogic hard disk drives are defined by type 47. Hard disk type 47 is reserved for user specified drive parameters.

Table 4: Hard Disk Parameters for CMOS Setup Screen.

Part Number	Cyln	Heads	WPcom	LZone	Sect	Size (MB)
VL-HD1-131	419	13	0	0	47	131
VL-HD1-210	988	8	0	0	52	210

Clearing the CMOS RAM

Jumper V4[1-2] allows you clear the CMOS RAM contents if you remove the battery, install incorrect setup information, or otherwise corrupt CMOS RAM. To ensure integrity of the CMOS RAM, the Setup program calculates and stores an internal checksum of the setup data. Upon reset, the CPU detects if the CMOS RAM is corrupted by analyzing the checksum. If you wish to completely clear the contents of the CMOS RAM, briefly move jumper V4 to position [1-2] (top position) then back to the position [2-3] (lower position) and reboot the system. This process will load the factory default setup parameters into the CMOS RAM.

Warning! Do not apply power to the CPU card with jumper V4[1-2] installed, doing so may damage the chipset and void the warranty. Jumper V4[1-2] is only briefly used to clear the CMOS RAM.

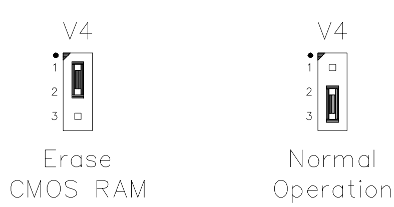


Figure 3. CMOS RAM Jumper

Configuration 3

This chapter describes how to configure the on-board options for the VL-486-3 CPU card. Configuration involves both hardware (jumper) and software (chipset) configuration. The jumpers configure the circuitry on the card for various modes of operation. The software configuration completes the process by initializing the circuits within the chipset. This chapter does not describe how to initialize the standard DOS peripheral devices such as the serial ports and disk drive interfaces.

Hardware Jumper Summary

Hardware option configuration is accomplished by installing or removing jumper plugs. In this chapter, the term “in” is used to indicate an installed jumper and “out” is used to indicate a removed jumper.

Use the following key to interpret the jumper diagrams used in this manual:

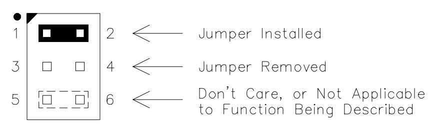


Figure 4. Jumpering Key

JUMPER BLOCK LOCATIONS

Note Jumpers and resistor packs shown in as-shipped configuration.

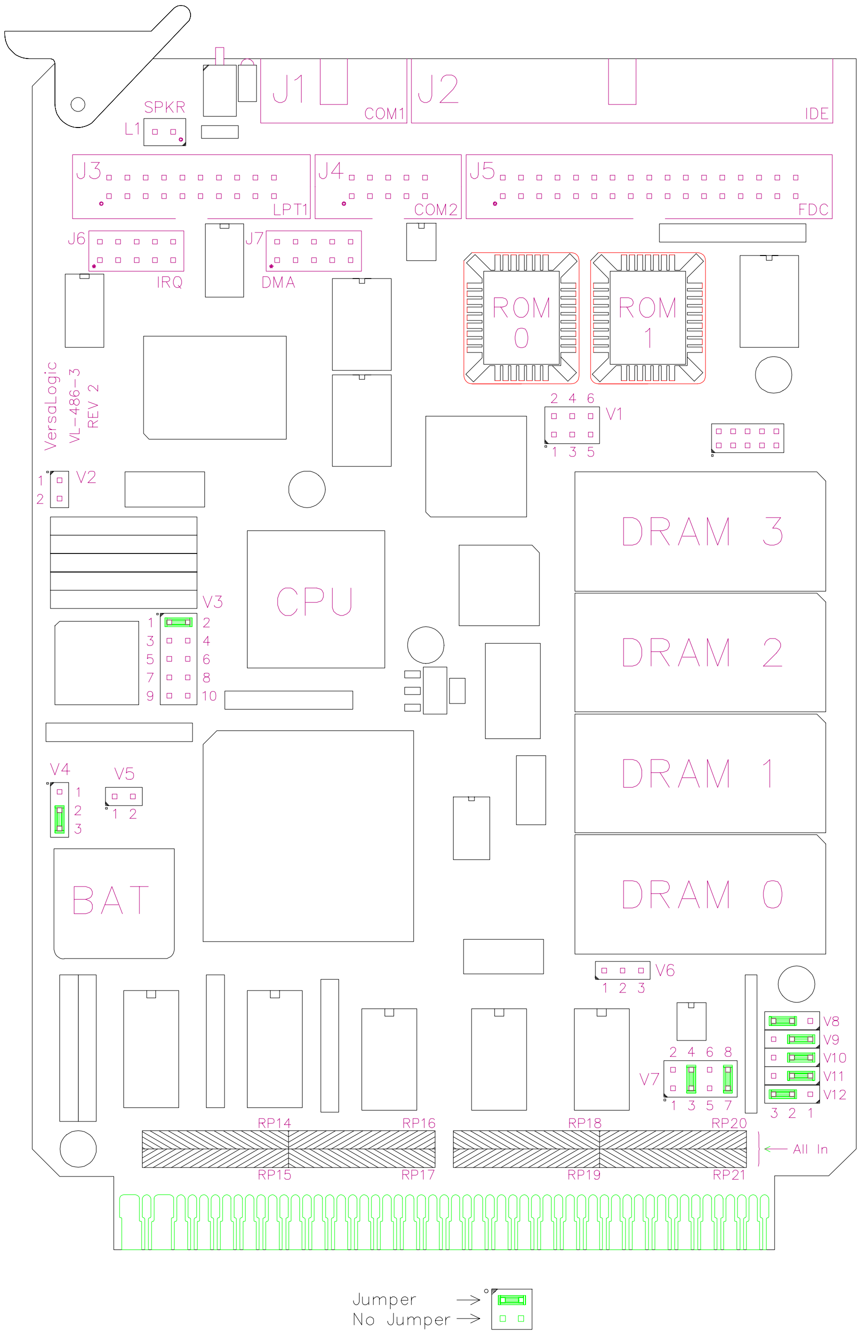


Figure 5. Jumper Block Locations

Table 5: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**General Purpose Digital Input** In — Causes bit D5 (GP0) of the SCR register ro read as “1” Out — Causes bit D5 (GP0) of the SCR register ro read as “0”	Out	59
V1[3-4]	**Multiprocessor Configuration** In — Dual master mode. Uses BUSAK* (P41) for bus arbitration. Out — Permanent or temporary master mode.	Out	24
V1[5-6]	**Multiprocessor Configuration** In — Dual master mode. Uses BUSRQ* (P42) for bus arbitration. Out — Permanent or temporary master mode.	Out	25
V2	**DMA Configuration** In — DMA from connector J7 serviced by DMA Channel 7 (16-bit) Out — DMA from connector J7 serviced by DMA Channel 3 (8-bit)	In	33
V3[1-2]	**RS-232 Signal Enable** In — RS-232 mode. Enables the RS-232 line drivers and receivers. Out — RS-485 mode. Disables the RS-232 line drivers and receivers.	In	24
V3[3-4]	**RS-485 Ground Circuit** In — RS-485 mode. Connects ground to J4 pin 6. Out — RS-232 mode. Frees J4 pin 6 for CTS2 (COM2).	Out	24
V3[5-6]	**RS-485 Receiver Enable** In — RS-485 mode. Enables the RS-485 line receiver. Out — RS-232 mode. Disables the RS-485 line receiver.	Out	24
V3[7-8]	**RS-485 Transmitter Control** In — RS-485 mode. Enables software control of the RS-485 line driver. Out — RS-232 mode. Disables the RS-485 line driver.	Out	24
V3[9-10]	**RS-485 Transmission Line Termination** In — Terminates data circuit with 100 Ω resistor (endpoint stations only) Out — Leaves data circuit unterminated (used for intermediate multidrop stations or for RS-232)	Out	24
V4[1-2]	**CMOS RAM Erase** In — Erases CMOS RAM and Real Time Clock contents Out — Normal operation (V4[2-3] must be in)	Out	21
V4[2-3]	**CMOS RAM Power** In — Connects power to CMOS RAM and Real Time Clock circuits Out — Power disconnected	In	21
V5[1-2]	**CMOS Battery Test Terminals** ***Note!*** *V5 is not a jumper. It is used as a test point to measure the current flowing in the CMOS battery circuit.*	—	26
V6[1-2]	**IPC Configuration (IPC / INTRQ* interconnect)** In — Connects IPC signal to STD Bus INTRQ* (P44) Out — Disconnects IPC from INTRQ*	Out	32
V6[2-3]	**IPC Configuration (IPC / INTRQ4* interconnect)** In — Connects IPC signal to STD Bus INTRQ4* (P05) Out — Disconnects IPC from INTRQ4*	Out	32

Table 5: Jumper Summary.

Jumper Block	Description	As Shipped	Page
V7[1-2]	**CPU response to SYSRESET*** In — CPU resets whenever STD Bus SYSRESET* (P47) goes low Out — CPU ignores activity on STD Bus SYSRESET* (P47)	Out	26
V7[3-4]	**Push-button Reset / Bus Interconnect** In — Connects STD Bus PBRESET* (P48) to CPU reset circuits Out — CPU ignores activity on, and does not drive STD Bus PBRESET* (P48)	In	26
V7[5-6]	**Non-Maskable Interrupt / BUS Interconnect** In — Connects STD Bus NMIRQ* (P46) to CPU NMI input Out — CPU ignores activity on STD Bus NMIRQ* (P46)	Out	32
V7[7-8]	**Permanent / Temporary Master Selection** In — Permanent Master Mode (V7[1-2] must be out, RP14 – RP21 must be in) Out — Temporary Master Mode (RP14 – RP21 must be out)	In	26
V8[1-2]	**Interrupt Configuration (IRQ1 / INTRQ* interconnect)** In — Connects STD Bus INTRQ* (P44) to IRQ1 Out — Disconnects INTRQ* from IRQ1	Out	26
V8[2-3]	**Interrupt Configuration (IRQ1 / INTRQ1* [Keyboard] interconnect)** In — Connects STD Bus INTRQ1* (P37) [Keyboard Interrupts] to IRQ1 Out — Disconnects INTRQ1* from IRQ1	In	26
V9[1-2]	**Interrupt Configuration (IRQ3 / COM2 interconnect)** In — Connects COM2 to IRQ3 Out — Disconnects COM2 from IRQ3	In	26
V9[2-3]	**Interrupt Configuration (IRQ3 / Front Plane 4 interconnect)** In — Connects Front Plane 4 (J6 pin 4) to IRQ3 Out — Disconnects FP4 from IRQ3	Out	26
V10[1-2]	**Interrupt Configuration (IRQ11 / INTRQ2* interconnect)** In — Connects STD Bus INTRQ2* (P50) to IRQ11 Out — Disconnects STD Bus INTRQ2* from IRQ11	In	26
V10[2-3]	**Interrupt Configuration (IRQ11 / Front Plane 6 interconnect)** In — Connects Front Plane 6 (J6 pin 6) to IRQ11 Out — Disconnects FP6 from IRQ11	Out	26
V11[1-2]	**Interrupt Configuration (IRQ12 / INTRQ3* Interconnect)** In — Connects STD Bus INTRQ3* (E67) to IRQ12 Out — Disconnects INTRQ3* from IRQ12	In	26
V11[2-3]	**Interrupt Configuration (IRQ12 / Front Plane 8 interconnect)** In — Connects Front Plane 8 (J6 pin 8) to IRQ12 Out — Disconnects FP8 from IRQ12	Out	26
V12[1-2]	**Interrupt Configuration (IRQ15 / CTC2 interconnect)** In — Connects Counter / Timer 2 to IRQ15 Out — Disconnects CTC2 from IRQ15	Out	26
V12[2-3]	**Interrupt Configuration (IRQ15 / Front Plane 10 interconnect)** In — Connects Front Plane 10 (J6 pin 10) to IRQ15 Out — Disconnects FP10 from IRQ15	In	26

Memory Configuration

ROM Configuration

The on-board ROM sockets (U5 and U8) accept one or two 128Kx8, 256Kx8, or 512Kx8, 32 pin plastic PLCC or 32 pin J-lead ceramic part(s). An extractor tool (such as VersaLogic part number 9685) is required to remove the rectangular PLCC device(s) without damage, and an adapter may be required to program PLCC parts when using EPROM programmers that support only 32-pin 0.6" DIP style packages.

The ROM contains BIOS and ROM disk data in DOS-based systems. In non-DOS-based systems, the ROM contains the CPU initialization code and application code.

There are no configuration jumpers for the ROM sockets.

Compatible ROM Devices

The following (non exhaustive) list of memory devices can be used in the ROM sockets. All parts must be 200 ns or less.

Caution VersaLogic makes no representation of the suitability, reliability, or availability of any of the memory devices.

Table 6: Compatible ROM/Flash Devices.

EPROM, UV Erasable (32-pin PLCC)	
27C010	128K x 8
27C020	256K x 8
27C040	512K x 8
Available from Catalyst, Cypress, and Texas Instruments	
Flash EPROM, 12 volt, Read-Only (32-pin PLCC)	
28F010	128K x 8
28F020	256K x 8
Available from AMD, Catalyst, Intel, and Texas Instruments	
Flash EPROM, 5 volt only, Read/Write (32-pin PLCC)	
29F010	128K x 8
29F040	512K x 8
Available from AMD, Texas Instruments, and Atmel	

RAM Configuration

The on-board RAM sockets (U13, U15, U16, and U19) accept up to four 1Mx16 or 1Mx18, 42 pin plastic or ceramic SOJ dynamic RAM chips. The use of 1M x 18 RAM chips will provide parity error detection if desired.

Table 7: RAM Sockets.

Socket Number	Address Range
U19	000000h – 1FFFFFh
U16	200000h – 3FFFFFh
U15	400000h – 5FFFFFh
U13	600000h – 7FFFFFh

Compatible RAM Devices

The following (non exhaustive) list of memory devices can be used. All parts must be 70 ns or faster, and must use 1024 refresh cycles.

Note The 1M x 16 RAM is available from VersaLogic as part number 9650.

Caution VersaLogic makes no representation of the suitability, reliability, or availability of any of the following memory devices.

Table 8: Compatible RAM Devices.

Dynamic RAM (42-pin SOJ) without Parity		
Brand	**Part Number**	**Size**
Hitachi	HM5118160AJ-70	1M x 16
NEC	uPD4218160LE-70	1M x 16
Toshiba	TC5118160AJ-70	1M x 16

Dynamic RAM (42-pin SOJ) with Parity		
Brand	**Part Number**	**Size**
Toshiba	TC5118180AJ-70	1M x 18

CMOS RAM CONFIGURATION

The VL-486-3 CPU card is shipped with the battery disconnected. Since the battery provides backup power to the CMOS RAM and the real time clock circuits when the card is powered down, the battery must be activated before putting the card in service.

To activate the battery, move jumper V4 to position [2-3] (bottom position) as shown.

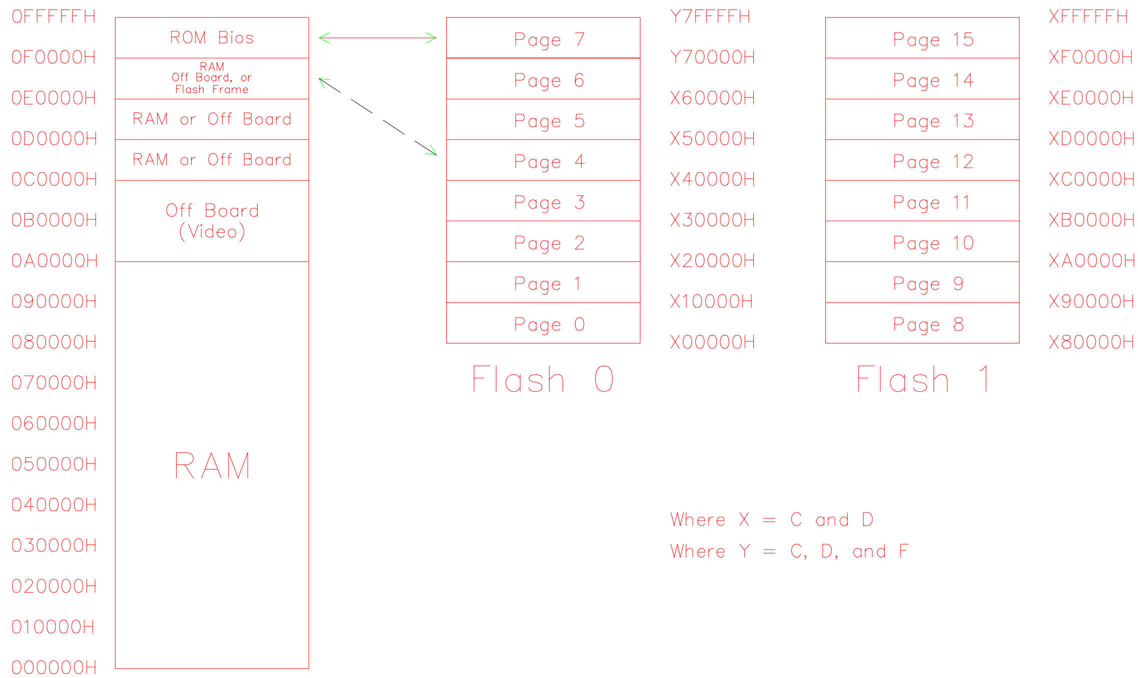
Jumper V4[1-2] (top position) can be briefly used to erase the contents of the CMOS RAM should it become necessary to do so.

Table 9: CMOS RAM Jumpers

Jumper Block	Description	As Shipped
V4[1-2]	**CMOS RAM Erase** In — Erases CMOS RAM and Real Time Clock contents Out — Normal operation (V4[2-3] must be in)	Out
V4[2-3]	**CMOS RAM Power** In — Connects power to CMOS RAM and Real Time Clock circuits Out — Power disconnected	In

MEMORY MAPPING

The memory map of the VL-486-3 is arranged as follows. Page 7 of Flash 0 is the system BIOS, and always appears from 0F0000h to 0FFFFFh. Bits D3–D0 in the MPCR register select which Flash ROM page is mapped into the Flash Frame (0E0000h to 0EFFFFh). See MPCR register description on page 61 for further information.



I/O Configuration

USING 8-BIT I/O CARDS

I/O cards which only decode 8 address bits (A0 - A7) will work properly with the VL-486-3 provided the STD Bus signal IOEXP is decoded low on the I/O card. IOEXP will be driven low in the I/O address range FC00h to FFFFh. The I/O card can be configured to use any 8-bit address in the range 00h to FFh.

- 00h – FFh (With IOEXP decoded low)

A card which does not support IOEXP will repeat every 256 (100h) bytes throughout the entire 64K I/O space. This will cause conflict with reserved I/O addresses used for on-board devices. Operation in this manner is not recommended.

Application software should be written to communicate with the I/O cards using the addresses listed above as X+FF00h. For example if your I/O card is addressed at 38h, the software should use FF38h as the I/O port address.

USING 10-BIT I/O CARDS

I/O cards which only decode 10 address bits (A0 - A9) will work properly with the VL-486-3 when addressed in the following I/O ranges:

- 100h – 1EFh
- 200h – 27Fh
- 300h – 3AFh

A card which does not decode IOEXP low will repeat every 1024 (400h) bytes throughout the entire 64K I/O space. This means the CPU will see the I/O addresses listed above as X+0000h, X+0400h, X+0800h, X+0C00h, X+1000h, X+1400h, etc.

If IOEXP is decoded low, the card will only appear in the FF00h to FFFFh range (assuming the card is addressed at 300h to 3FFh). Operation in this manner is not recommended.

Application software should be written to communicate with the I/O cards using the exact addresses listed above (i.e., X+0000h). For example if your I/O card is addressed at 220h, the software should use 0220h as the I/O port address.

USING 16-BIT I/O CARDS

I/O cards which decode all 16 address bits (A0 - A15) will work properly with the VL-486-3 when addressed in the following I/O ranges:

- 0100h – 01EFh
- 0200h – 027Fh
- 0300h – 03AFh
- 0400h – FFFFh

Use of the IOEXP signal is not supported in 16-bit address mode.

Serial Port COM2 Configuration

Serial Port COM2 can be operated in RS-232 or RS-485 modes. Jumper V3 is used to configure the port.

RS-232 OPERATION

For RS-232 operation, jumper V3 should be jumpered as shown on the left.

RS-485 OPERATION

Removing V3[9-10] leaves the data circuit unterminated so that COM2 can be used as an intermediate station in an RS-485 multidrop system. When COM2 is used in multidrop operations, remove jumper V3[9-10] from all stations except both ends of the line.

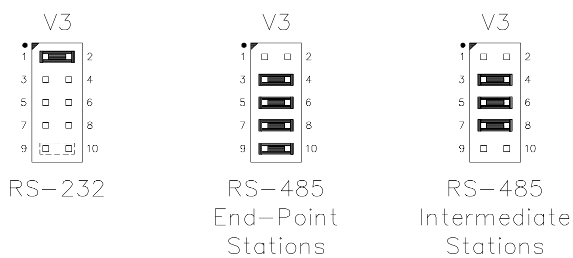


Table 10: Serial Port Jumpers

Jumper Block	Description	As Shipped
V3[1-2]	**RS-232 Signal Enable** In — RS-232 mode. Enables the RS-232 line drivers and receivers. Out — RS-485 mode. Disables the RS-232 line drivers and receivers.	In
V3[3-4]	**RS-485 Ground Circuit** In — RS-485 mode. Connects ground to J4 pin 6. Out — RS-232 mode. Frees J4 pin 6 for CTS2 (COM2).	Out
V3[5-6]	**RS-485 Receiver Enable** In — RS-485 mode. Enables the RS-485 line receiver. Out — RS-232 mode. Disables the RS-485 line receiver.	Out
V3[7-8]	**RS-485 Transmitter Control** In — RS-485 mode. Enables software control of the RS-485 line driver. Out — RS-232 mode. Disables the RS-485 line driver.	Out
V3[9-10]	**RS-485 Transmission Line Termination** In — Terminates data circuit with 100 Ω resistor (endpoint stations only) Out — Leaves data circuit unterminated (used for intermediate multidrop stations or for RS-232)	Out

Multiprocessor Configuration

The VL-486-3 CPU card supports multiple master operation for systems requiring additional processing capability or for "smart I/O" operations. In a multiple master system, one CPU must be configured as a permanent master and other CPUs are configured as temporary masters. In this scheme, a bus arbiter plugged into Slot X is used to arbitrate access to the bus. A special dualmaster mode is available for two CPUs to work together without a bus arbiter. In this configuration, one CPU should be jumpered as a permanent master and the other CPU should be jumpered as a dualmaster.

MULTIPROCESSOR JUMPER CONFIGURATION

Jumper blocks V1 and V7 are used to select the bus mastering mode.

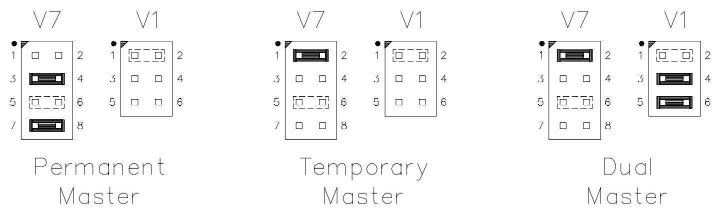


Table 11: Multiprocessor Configuration Jumpers

Jumper Block	Description	As Shipped
V1[3-4]	**Multiprocessor Configuration** In — Dual master mode. Uses BUSAK* (P41) for bus arbitration. Out — Permanent or temporary master mode.	Out
V1[5-6]	**Multiprocessor Configuration** In — Dual master mode. Uses BUSRQ* (P42) for bus arbitration. Out — Permanent or temporary master mode.	Out
V7[1-2]	**CPU response to SYSRESET*** In — CPU resets whenever STD Bus SYSRESET* (P47) goes low Out — CPU ignores activity on STD Bus SYSRESET* (P47)	Out
V7[3-4]	**Push-button Reset / Bus Interconnect** In — Connects STD Bus PBRESET* (P48) to CPU reset circuits Out — CPU ignores activity on, and does not drive STD Bus PBRESET* (P48)	In
V7[7-8]	**Permanent / Temporary Master Selection** In — Permanent Master Mode (V7[1-2] must be out, RP14 – RP21 must be in) Out — Temporary Master Mode (RP14 – RP21 must be out)	In

RESISTOR PACK CONFIGURATION

The eight resistor packs (RP14 through RP21) near the STD Bus connector must be removed for temporary master or dualmaster operation. Only one CPU in the card cage should have the resistor packs installed, the permanent master.

Note that two resistance values are used, 1.8KΩ and 330Ω.

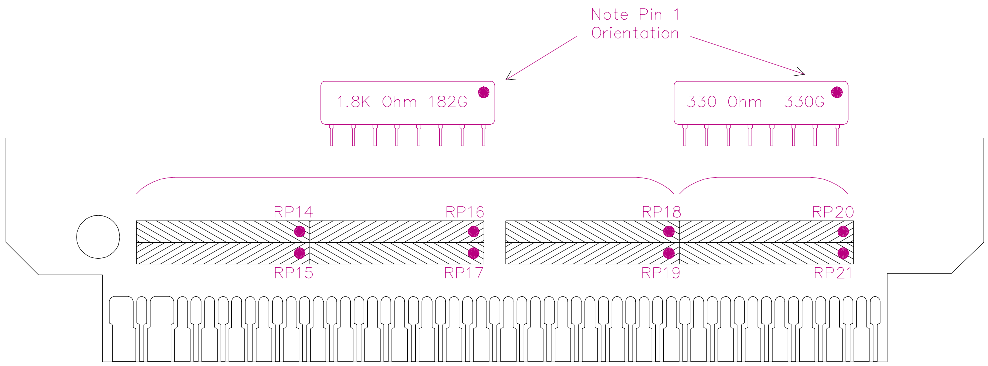


Figure 6. Multiprocessor Resistor Packs.

MULTIPROCESSOR CPU RESET

The CPU reset configuration depends upon the selected STD Bus master mode. Jumpers V7[1-2] and V7[3-4] configure the CPU to drive and respond to the STD Bus signals SYSRESET* and PBRESET* in different ways depending on the bus master mode.

Permanent Master — The CPU is reset by pressing the on-board push-button, and optionally, by a low level on PBRESET* arriving on the bus. Permanent masters are responsible for driving the SYSRESET* signal to reset temporary masters in the same card cage (which are configured to react to SYSRESET*). To prevent a persistent reset state, the permanent master is configured to ignore SYSRESET*.

Temporary Master — The CPU is reset by pressing the on-board push-button, and optionally, by a low level on SYSRESET* arriving from the permanent master via the bus. A temporary master should never respond directly to PBRESET* nor drive SYSRESET*.

Dual Master — Same as temporary master mode.

Interrupt Configuration

Six three-position jumper blocks are used to configure the interrupt sources on the VL-486-3. Each jumper block is used to select one of two interrupt sources and route it to the interrupt controller. Wire wrap techniques can be used on V8 through V12 to route interrupt sources to the CPU's IRQ inputs if the factory provided jumpers do not provide suitable connections.

Note Jumpers shown in as-shipped configuration.

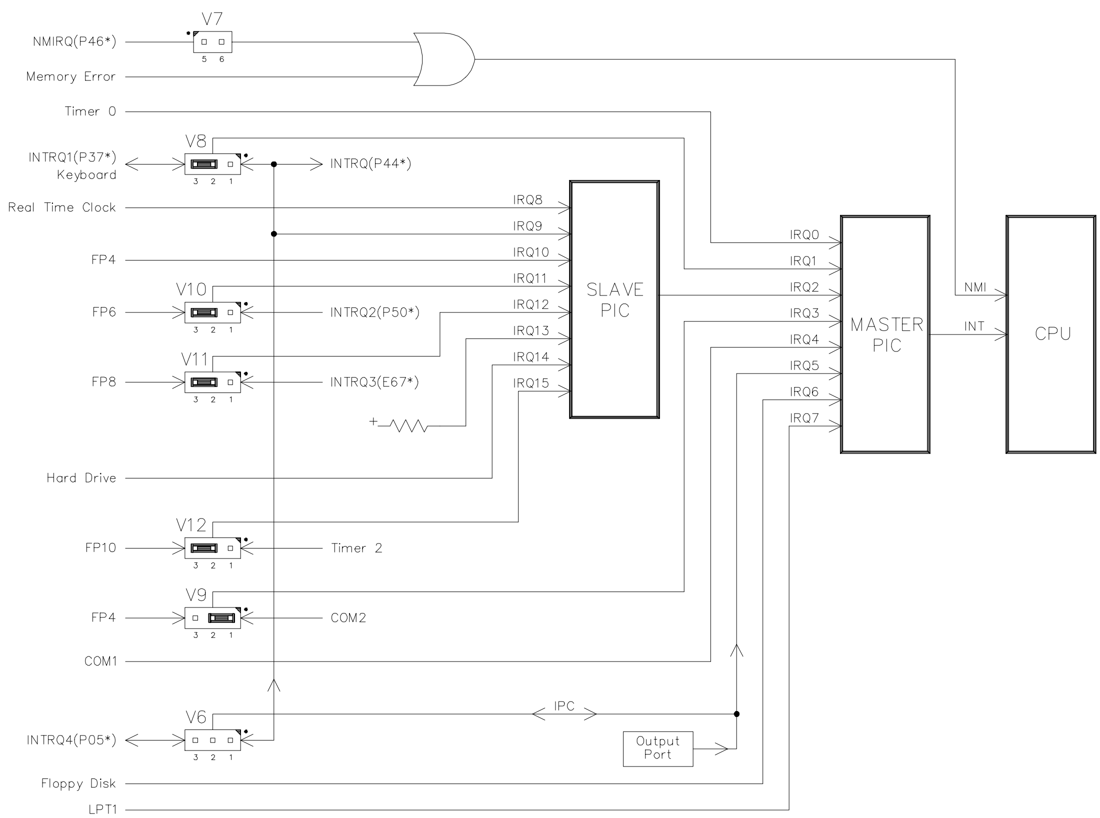


Figure 7. Interrupt Circuit Diagram

INTERRUPT CONFIGURATION JUMPERS

Table 12: Interrupt Configuration Jumpers

Jumper Block	Description	As Shipped
V6[1-2]	**IPC Configuration (IPC / INTRQ* interconnect)** In — Connects IPC signal to STD Bus INTRQ* (P44) Out — Disconnects IPC from INTRQ*	Out
V6[2-3]	**IPC Configuration (IPC / INTRQ4* interconnect)** In — Connects IPC signal to STD Bus INTRQ4* (P05) Out — Disconnects IPC from INTRQ4*	Out
V7[5-6]	**Non-Maskable Interrupt / BUS Interconnect** In — Connects STD Bus NMIRQ* (P46) to CPU NMI input Out — CPU ignores activity on STD Bus NMIRQ* (P46)	Out
V8[1-2]	**Interrupt Configuration (IRQ1 / INTRQ* interconnect)** In — Connects STD Bus INTRQ* (P44) to IRQ1 Out — Disconnects INTRQ* from IRQ1	Out
V8[2-3]	**Interrupt Configuration (IRQ1 / INTRQ1* [Keyboard] interconnect)** In — Connects STD Bus INTRQ1* (P37) [Keyboard Interrupts] to IRQ1 Out — Disconnects INTRQ1* from IRQ1	In
V9[1-2]	**Interrupt Configuration (IRQ3 / COM2 interconnect)** In — Connects COM2 to IRQ3 Out — Disconnects COM2 from IRQ3	In
V9[2-3]	**Interrupt Configuration (IRQ3 / Front Plane 4 interconnect)** In — Connects Front Plane 4 (J6 pin 4) to IRQ3 Out — Disconnects FP4 from IRQ3	Out
V10[1-2]	**Interrupt Configuration (IRQ11 / INTRQ2* interconnect)** In — Connects STD Bus INTRQ2* (P50) to IRQ11 Out — Disconnects STD Bus INTRQ2* from IRQ11	In
V10[2-3]	**Interrupt Configuration (IRQ11 / Front Plane 6 interconnect)** In — Connects Front Plane 6 (J6 pin 6) to IRQ11 Out — Disconnects FP6 from IRQ11	Out
V11[1-2]	**Interrupt Configuration (IRQ12 / INTRQ3* Interconnect)** In — Connects STD Bus INTRQ3* (E67) to IRQ12 Out — Disconnects INTRQ3* from IRQ12	In
V11[2-3]	**Interrupt Configuration (IRQ12 / Front Plane 8 interconnect)** In — Connects Front Plane 8 (J6 pin 8) to IRQ12 Out — Disconnects FP8 from IRQ12	Out
V12[1-2]	**Interrupt Configuration (IRQ15 / CTC2 interconnect)** In — Connects Counter / Timer 2 to IRQ15 Out — Disconnects CTC2 from IRQ15	Out
V12[2-3]	**Interrupt Configuration (IRQ15 / Front Plane 10 interconnect)** In — Connects Front Plane 10 (J6 pin 10) to IRQ15 Out — Disconnects FP10 from IRQ15	In

STD BUS INTERRUPT SIGNALS

The following table describes the six STD Bus interrupt signals. Some of these interrupt signals are hardwired to specific IRQ inputs, and others are connected to jumpers V8 through V12 for custom configuration.

Table 13: STD 32 Interrupt Signals.

Function	STD-32 Signal Name	STD-32 Pin Number	Typical Use	Notes
NMI*	NMIRQ*	P46	High priority interrupts which should not be ignored.	NMIRQ* can be connected to the CPU NMI interrupt input by inserting jumper V7[5-6]. If multiple CPU's are used, typically only one CPU will be jumpered to respond to NMI.
INTRQ*	INTRQ*	P44	General purpose or Interprocessor Communications Interrupt (IPC)	INTRQ* is hardwired into IRQ9. It can also be jumpered to drive IRQ1 by inserting jumper V8[1-2]. INTRQ* can also be used to carry the Interprocessor Communications Interrupt (IPC) between multiple CPU's by inserting jumper V6[1-2]. Activity on INTRQ* will drive IRQ5.
INTRQ1 *	INTRQ1*	P37	Carries Keyboard interrupts from VL-SVGA-1 to VL-486-3. INTRQ1* is general purpose on systems without keyboards.	INTRQ1* can be configured to drive IRQ1 by inserting jumper V8[2-3]. (As shipped configuration.)
INTRQ2 *	CNTRL*	P50	General purpose	INTRQ2* can be configured to drive IRQ11 by inserting jumper V10[1-2].
INTRQ3 *	INTRQ3*	E67	General purpose	INTRQ3* can be configured to drive IRQ12 by inserting jumper V11[1-2].
INTRQ4 *	VBAT	P05	General purpose	INTRQ4* can be jumpered to carry the Interprocessor Communications Interrupt (IPC) between multiple CPU's by inserting jumper V6[2-3]. The IPC signal is hardwired to IRQ5.

CPU INTERRUPT REQUEST INPUTS

The seventeen standard IBM compatible interrupt inputs (IRQs) are shown below.

Table 14: Interrupt Request Inputs

Interrupt Signal Name	Interrupt Number	Typical Source of Interrupt on an IBM AT	As Shipped Configuration	Notes
NMI	—	Parity Check and IOCHCK from ISA Bus.	Hardwired	STD Bus NMIRQ* routed to CPU NMI input, but can be disconnected by removing a jumper.
IRQ0	08h	Timer 0	Hardwired	Internal signal, not available to the outside world.
IRQ1	09h	Keyboard	INTRQ1*	DOS/BIOS expects keyboard interrupts on this input. Comes from STD Bus via INTRQ* or INTRQ1*. The interrupt jumper on the VL-SVGA-1 must match.
IRQ2	0Ah	Slave Interrupt Controller	Hardwired	Internal signal, not available to the outside world.
IRQ3	0Bh	COM2	COM2	DOS/BIOS usually expects COM2 interrupts on this input. Comes from the on-board COM2 circuitry or via Front-Plane connector J6 (FP4).
IRQ4	0Ch	COM1	COM1	Internal signal, not available to the outside world.
IRQ5	0Dh	LPT 2	Hardwired	IPC Interrupts.
IRQ6	0Eh	Floppy Disk	Hardwired	Internal signal, not available to the outside world.
IRQ7	0Fh	LPT1	Hardwired	Internal signal, not available to the outside world.

Table 14: Interrupt Request Inputs

Interrupt Signal Name	Interrupt Number	Typical Source of Interrupt on an IBM AT	As Shipped Configuration	Notes
IRQ8	70h	Real Time Clock	Hardwired	Internal signal, not available to the outside world. Can be used for alarms or perodic interrupts.
IRQ9	71h	Unassigned	Hardwired	Hardwired to STD Bus INTRQ*.
IRQ10	72h	Unassigned	Hardwired	Hardwired to Front-Plane connector J6 (FP4).
IRQ11	73h	Unassigned	INTRQ2*	IRQ11 can receive interrupts from STD Bus INTRQ2* or from the Front-Plane connector J6 (FP6).
IRQ12	74h	Unassigned	INTRQ3*	IRQ12 can receive interrupts from STD Bus INTRQ3* or from the Front-Plane connector J6 (FP8).
IRQ13	75h	Math Coprocessor	No Connection	Internal signal, not available to the outside world. Non-DOS users should mask this interrupt.
IRQ14	76h	Hard Disk Drive	Hardwired	Internal signal, not available to the outside world.
IRQ15	77h	Unassigned	Front Plane 10	IRQ15 can receive interrupts from the on-board Counter/Timer #2 or from the Front-Plane connector J6 (FP10).

INTERPROCESSOR COMMUNICATIONS INTERRUPT CONFIGURATION

Jumpers V6[1-2] and V6[2-3] are used to route the Interprocessor Communications (IPC) interrupt signal. Two choices are available: IPC can be carried on the STD Bus signal INTRQ* (P44) or INTRQ4* (P05). If IPC is not being used, both jumpers can be removed to free up INTRQ* and INTRQ4* for other purposes.

Table 15: Interprocessor Communications Interrupt Jumpers

Jumper Block	Description	As Shipped
V6[1-2]	**IPC Configuration (IPC / INTRQ* interconnect)** In — Connects IPC signal to STD Bus INTRQ* (P44) Out — Disconnects IPC from INTRQ*	Out
V6[2-3]	**IPC Configuration (IPC / INTRQ4* interconnect)** In — Connects IPC signal to STD Bus INTRQ4* (P05) Out — Disconnects IPC from INTRQ4*	Out

NON-MASKABLE INTERRUPT CONFIGURATION

Jumper V7[5-6] is used to connect the STD Bus NMIRQ* (P46) signal to the CPU NMI input. When this jumper is removed, NMIRQ* can be used for other purposes.

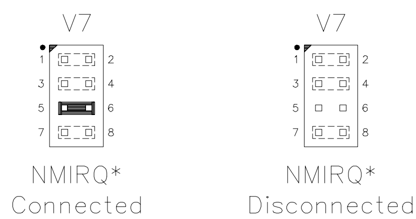


Table 16: Non-Maskable Interrupt Jumper

Jumper Block	Description	As Shipped
V7[5-6]	**Non-Maskable Interrupt / BUS Interconnect** In — Connects STD Bus NMIRQ (P46*) to CPU NMI input Out — CPU ignores activity on STD Bus NMIRQ (P46*)	Out

DMA Configuration

Jumper block V2 is used to select the data size for DMA transfers requested through the front plane connector J7.

Table 17: DMA Configuration Jumpers

Jumper Block	Description	As Shipped
V2	**DMA Configuration** In — DMA from connector J7 serviced by DMA Channel 7 (16-Bit) Out — DMA from connector J7 serviced by DMA Channel 3 (8-Bit)	In

DMA Channel Allocation

Four 16-bit and four 8-bit DMA channels are available on the VL-486-3 CPU card. Five of the channels are only available to software (handshaking lines are not accessible), one is dedicated to the floppy disk interface, and the remaining two channels are used by the front plane DMA connector (J7). Jumper V2 is used to select between 8-bit and 16-bit modes.

Table 18: DMA Channel Allocation.

DMA Channel	Data Width	Channel Allocation
0	8 Bit	***Not Used***
1	8 Bit	***Not Used***
2	8 Bit	***On-Card Floppy***
3	8 Bit	***General DMA via Front Plane*** Request: J2, Pin 2 (FPRQ*) Acknowledge: J2, Pin 4 (FPAK*) (V2=OUT)
4	16 Bit	***Not Used***
5	16 Bit	***Not Used***
6	16 Bit	***Not Used***
7	16 Bit	***General DMA via Front Plane*** Request: FPRQ* Acknowledge: FPAK* (V2=IN)

Board Initialization

Several registers on the VL-386/486 CPU board must be initialized for proper operation. In DOS-based systems, the BIOS automatically initializes the various registers, however, in non-DOS-based systems you must program the initialization sequence in ROM. Initialization must execute immediately upon reset, and in the following order:

- 82C836 Initialization
- 82C721 Initialization
- 486SXLC Initialization
- RAM Refresh Initialization

If the VL-386/486 is initialized exactly as presented in this manual, the CPU card will be configured with the following features:

- 16-Bit DMA transfers operate with one wait-state
- 8-Bit DMA transfers operate with one wait-state
- DRAM operates with zero wait-states
- ROM active in UMB from 0F0000h to 0FFFFFh
- Hidden refresh enabled
- 640K + 1M extended DRAM for 2M CPU card
- 640K + 3M extended DRAM for 4M CPU card
- 640K + 5M extended DRAM for 6M CPU card
- 640K + 7M extended DRAM for 8M CPU card
- COM1 is located at I/O address 3F8h
- COM2 is located at I/O address 2F8h
- LPT1 is located at I/O address 3BCh

This manual does not document the details of the data written to the chipset registers. Refer to the Chips & Technologies *82C836 Single-Chip 386sx AT* and *82C721 Universal Peripheral Controller II* data books listed in “Other References” on page vii.

The chips in the Chips & Technologies chipset, the 82C836 and the 82C721, have different methods of register access which are described in the following sections.

82C836 Initialization

The Internal Configuration Registers (ICR) of the 82C836 are accessed using I/O ports 0022h and 0023h. The initialization data must be written to the 82C836 immediately after CPU reset.

To initialize the 82C836:

1. Output the ICR index number to port 0022h.
2. Output the initialization data to port 0023h (see table).
3. Repeat steps 1 and 2 for all the registers.

Table 19: Chips & Technologies 82C836 Initialization Data

Index Number	Initialization Data: 2M DRAM	4M DRAM	6M DRAM	8M DRAM	Description
01h	00h	00h	00h	00h	DMA Wait-State Control Register
40h	—	—	—	—	Version Register
41h	08h	08h	08h	08h	Channel Environment Register
42h	—	—	—	—	Reserved
43h	—	—	—	—	Reserved
44h	01h	01h	01h	01h	Peripheral Control Register
45h	—	—	—	—	Miscellaneous Status Register
46h	01h*	01h*	01h*	01h*	Power Management Register
47h	—	—	—	—	Reserved
49h	00h	00h	00h	00h	RAM Write Protect Register
4Ah	00h	00h	00h	00h	Shadow RAM Enable Register 1
4Bh	00h	00h	00h	00h	Shadow RAM Enable Register 2
4Ch	00h	00h	00h	00h	Shadow RAM Enable Register 3
4Dh	0Bh	0Ch	0Dh	0Eh	DRAM Configuration Register
4Eh	59h	59h	59h	59h	Extended Boundary Register
4Fh	00h	00h	00h	00h	EMS Control Register
60h	00h	00h	00h	00h	Laptop Features
61h	—	—	—	—	Fast Video Control
62h	—	—	—	—	Fast Video RAM Enable
63h	B0h	B0h	B0h	B0h	High Performance Refresh
64h	03h	03h	03h	03h	CAS Timing for DMA/Master

* When DRAM parity detection is enabled, this should be 41h.

82C721 Initialization

The Internal Configuration Registers (ICR) of the 82C721 are accessed using I/O ports 03F0h and 03F1h. The initialization data must be written to the 82C721 immediately after initializing the 82C836. A three step configuration sequence is used to prevent accidental changes by an errant program. Any deviation from the sequence described below will return the 82C721 to its initial idle state.

Configuration steps:

1. Enter Configuration Mode
   Output two consecutive 55h to port 03F0h.
2. Initialize the Configuration Registers
   a. Output the index number to port 03F0h
   b. Output the initialization data to port 03F1h (see table).
3. Exit Configuration Mode
   Output AAh to port 03F0h.

Table 20: Chips & Technologies 82C721 Initialization Data

Index Number	Initialization Data	Description
00h	9Bh	Configuration Register 0
01h	15h	Configuration Register 1
02h	DCh	Configuration Register 2
03h	00h	Configuration Register 3

486SXLC Initialization

Several registers in the 486SXLC microprocessor must be initialized for proper operation of the VL-486-1 and VL-486-2. In DOS-based systems, the BIOS automatically initializes the CPU; however, in non-DOS-based systems you must program the initialization sequence in ROM.

This manual does not document the details of the data written to the 486SXLC registers. Refer to the Texas Instruments *486SXLC Data Book* listed in "Other References" on page vii.

To initialize the 486SXLC:

1. Output the index number to port 0022h.
2. Output the initialization data to port 0023h (see table).
3. Repeat steps 1 and 2 for all the registers.

Table 21: 486SXLC Initialization Data

Index Number	Initialization Data	Description
C0h	53h	Register C0h
C1h	00h	Register C1h
C5h	0Ah	Register C5h
C6h	06h	Register C6h
C8h	0Ch	Register C8h
C9h	07h	Register C9h
CBh	00h	Register CBh
CCh	00h	Register CCh
CEh	00h	Register CEh
CFh	00h	Register CFh

RAM Refresh Initialization

The DRAM refresh must be initialized by sending the data listed in table below directly to the ports indicated.

Table 22: Refresh Initialization

Port Number	Initialization Data	Description
61h	04h	Mask DRAM Parity Interrupt
43h	54h	Refresh Timer Command
41h	18h	Refresh Time Constant

Installation 4

Introduction

Before installing the CPU card in a card cage, you must confirm that the on-board battery is activated.

Caution Electrostatic discharge (ESD) can damage cards, disk drives, and other components. Do the installation procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part on the card cage.

Caution Cards can be extremely sensitive to ESD and always require careful handling. After removing the card from its protective wrapper or from the card cage, place the card on a grounded, static-free surface, component side up. Use an anti-static foam pad if available, but not the card wrapper. Do not slide the card over any surface.

The card should also be protected during shipment or storage with anti-static foam or bubble wrap. To prevent damage to the lithium battery, do not use black conductive foam or metal foil.

Warning! The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Activating the Battery

The VL-486-3 CPU card is shipped with the battery disconnected. Since the battery provides backup power to the CMOS RAM and the real time clock circuits when the card is powered down, the battery must be activated before putting the card in service.

To activate the battery, move jumper V4 to position [2-3] (bottom position) as shown on page 21.

Card Insertion and Extraction

Cards should be inserted or removed from the STD Bus card cage only when the system power is off. If you meet resistance when extracting a card, make sure the retainer bar on the card cage is out of the way.

CARD INSTALLATION

The VL-486-3 card can be used alone, as a single board computer; as the only computer in a card cage with other I/O cards; or in conjunction with several other CPUs in a multiprocessing arrangement.

Cards must be oriented correctly in the card cage (usually with the card ejector toward the top of the card cage). Refer to the card cage documentation for the correct way to insert STD Bus cards.

CARD PLACEMENT

The CPU can be inserted into any available slot in an STD Bus card cage. When using an STD 32 card cage, the left most slot position is designated as Slot X and is not bussed in parallel with the other slots. Do not insert the CPU or any I/O card into this slot; it is reserved for a bus artbiter or a power supply card.

For proper disk drive cable layout, the CPU must be situated between the disk drive cards. The Hard Disk card(s) must be situated to the right of the CPU and the Floppy Disk card (if used) to the left. It does not matter which slot the Video card is plugged into.

Table 23: Recommended Card Positions.

Slot #	Card	Part Number
0	Floppy Disk	VL-FD1
1	CPU	VL-486-3
2	Hard Disk	VL-HD1-xxx
Any	Video Card	VL-SVGA-1

STD 32 BUS INSTALLATION GUIDELINES

The VL-486-3 card complies with all STD 32 specifications. If the CPU is used with other STD 32 compatible I/O cards, the highest performance will be realized by plugging all the cards into an STD 32 card cage.

An 8-bit STD 80 card cage can be used if cost savings are a prime consideration over performance. If the I/O cards are 8-bit STD Bus cards, or if the system is a single-board (CPU only) design, an 8-bit STD Bus card cage is good choice.

A variety of STD 80 (8-bit) and STD 32 (8 or 16-bit) cards can be mixed in an STD 32 card cage. Dynamic bus sizing signals automatically determine the data bus width.

External Connections

This chapter describes the external interfaces available on the VL-486-3 CPU card.

CONNECTOR FUNCTIONS

Table 24: Connector Functions

Connector	Function
J1	COM1 Serial Port Connector
J2	IDE Hard Disk Drive Connector
J3	LPT1 Parallel Port Connector
J4	COM2 Serial Port Connector
J5	Floppy Disk Drive Connector
J6	Interrupt Connector
J7	DMA Connector
L1	Speaker Connector
STD	STD 32 BUS Interface

CONNECTOR LOCATIONS

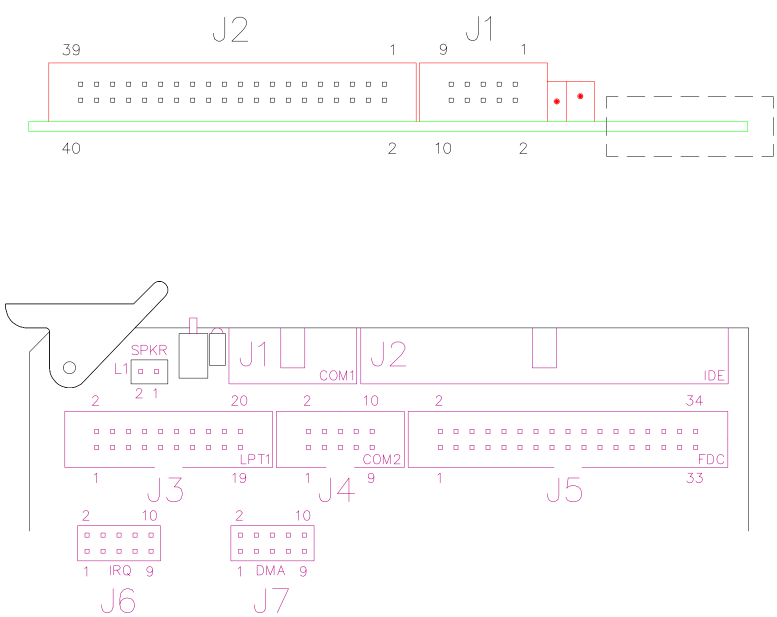


Figure 8. Connector Locations

MATING CONNECTORS AND CABLE ASSEMBLIES

Connections to the VL-486-3 can be made using flat ribbon cable and mass-terminated mating connectors. To bring the connectors on the VL-486-3 card out to standard PC/AT style pinouts, the VersaLogic cable assemblies listed below can be used.

Schematic diagrams for the cable assemblies are shown on the following pages.

Table 25: Mating Connectors and Cable Assemblies

Connector	Mating Connector	Cable Part #	Description	Connects to:
J1 (COM1)	3M 3473-6610	9575 9551	1 ft. 10-pin IDC to DB-9P 9 ft. 10-pin IDC to DB-25S (null modem)	External equipment (e.g., modem) DTE device (e.g., host PC)
J2 (IDE)	3M 3417-6640	9578	3 in. 40-pin IDC to 40-pin IDC	IDE hard disk drive
J3 (LPT1)	3M 3421-6620	9576	1 ft. 20-pin IDC to DB-25S	External printer
J4 (COM2)	3M 3473-6610	9575	1 ft. 10-pin IDC to DB-9S	External equipment (e.g., modem)
J5 (FDC)	3M 3414-6634	9577	8 in. 34-pin IDC to 34-pin IDC	Floppy disk drive
J6 (IRQ)	3M 3385-6614	N/A	Not Available	Miscellaneous user circuitry
J7 (DMA)	3M 3473-6610	N/A	Not Available	Miscellaneous user circuitry
L1 (Speaker)	—	N/A	Not Available	External 8Ω speaker

CABLE ASSEMBLY DIAGRAMS

The following diagrams show how to construct the cables which attach to the external connectors.

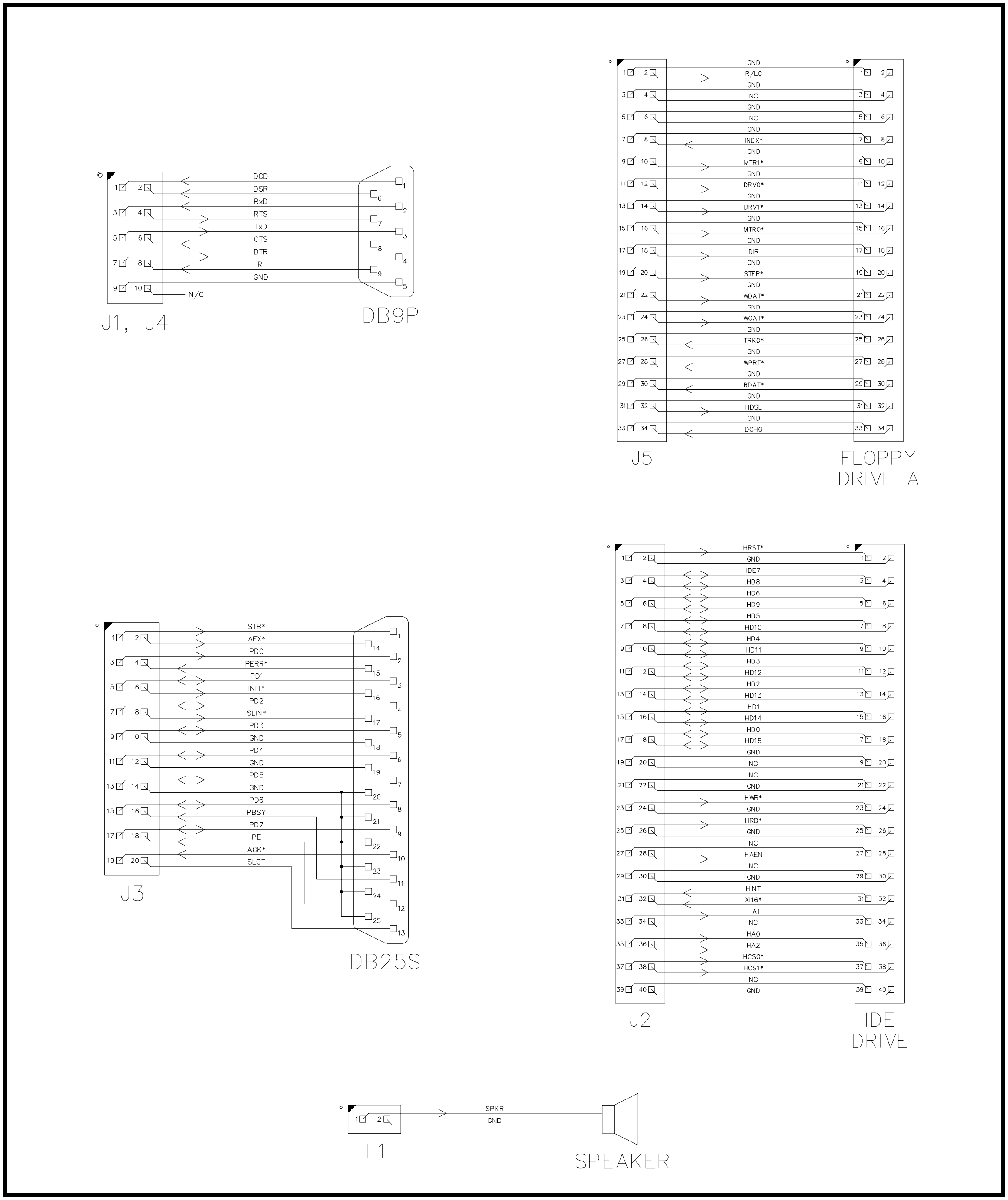


Figure 9. Cable Assemblies

J1, J4 – Serial Port Connectors

Connectors J1 and J4 provide signals for two serial I/O ports: COM1 and COM2. COM1 signals connect to the 10-pin header connector at J1. COM2 signals connect to the 10-pin header connector at J4. COM1 supports RS-232 operation only, and COM2 operates in RS-232 or RS-485 mode.

Table 26: J1, J4 RS-232 Serial Port Connector Pinout

J1, J4 Pin	Signal Name	RS-232 Signal Description	Signal Direction
1	DCD	Data Carrier Detect	In
2	DSR	Data Set Ready	In
3	RXD*	Receive Data	In
4	RTS	Request To Send	Out
5	TXD*	Transmit Data	Out
6	CTS	Clear To Send	In
7	DTR	Data Terminal Ready	Out
8	RI	Ring Indicator	In
9	Ground	Ground	—
10	N/C	—	—

Table 27: J4 RS-485 Serial Port Connector Pinout

J4 Pin	Signal Name	RS-485 Signal Description	Signal Direction
1	N/C	—	—
2	N/C	—	—
3	N/C	—	—
4	N/C	—	—
5	N/C	—	—
6	Ground	Ground	—
7	TD2/RD2–	Transmit/Receive Data Neg.	Out/In
8	TD2/RD2+	Transmit/Receive Data Pos.	Out/In
9	N/C	—	—
10	N/C	—	—

J2 – HARD DISK DRIVE CONNECTOR

Caution Cable length must be 18” or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 28: IDE Hard Disk Connector Pinout

J2 Pin	Signal Name	IDE Signal Name	Function
1	HRST*	Host Reset	Reset signal from CPU
2	Ground	Ground	Ground
3	IDE7	DATA 7	Data bit 7
4	HD8	DATA 8	Data bit 8
5	HD6	DATA 6	Data bit 6
6	HD9	DATA 9	Data bit 9
7	HD5	DATA 5	Data bit 5
8	HD10	DATA 10	Data bit a
9	HD4	DATA 4	Data bit 4
10	HD11	DATA 11	Data bit 11
11	HD3	DATA 3	Data bit 3
12	HD12	DATA 12	Data bit 12
13	HD2	DATA 2	Data bit 2
14	HD13	DATA 13	Data bit 13
15	HD1	DATA 1	Data bit 1
16	HD14	DATA 14	Data bit 14
17	HD0	DATA 0	Data bit 0
18	HD15	DATA 15	Data bit 15
19	Ground	Ground	Ground
20	NC	NC	No connection
21	NC	NC	No connection
22	Ground	Ground	Ground
23	HWR*	HOST IOW*	I/O write
24	Ground	Ground	Ground
25	HRD*	HOST IOR*	I/O read
26	Ground	Ground	Ground
27	NC	NC	No connection
28	HAEN	ALE	Address latch enable
29	NC	NC	No connection
30	Ground	Ground	Ground
31	HINT	HOST IRQ14	IRQ14
32	XI16*	HOST IOCS16*	Drive register enabled
33	HA1	HOST ADDR1	Address bit 1
34	NC	NC	No connection
35	HA0	HOST ADDR0	Address bit 0
36	HA2	HOST ADDR2	Address bit 2
37	HCS0*	HOST CS0*	Reg. access chip select 0
38	HCS1*	HOST CS1*	Reg. access chip select 1
39	NC	NC	No connection
40	Ground	Ground	Ground

J3 – LPT1 Parallel Port Connector

The bi-directional parallel port at J3 can be used as a standard PC/AT compatible LPT1 port or as 17 general purpose TTL I/O signals.

Table 29: LPT1 Parallel Port Pinout

J3 Pin	Signal Name	Centronics Signal	Signal Direction
1	STB*	Strobe	Out
2	AFX*	Auto feed	Out
3	PD0	Data bit 1	In/Out
4	PERR*	Printer error	In
5	PD1	Data bit 2	In/Out
6	INIT*	Reset	Out
7	PD2	Data bit 3	In/Out
8	SLIN*	Select input	Out
9	PD3	Data bit 4	In/Out
10	Ground	Ground	—
11	PD4	Data bit 5	In/Out
12	Ground	Ground	—
13	PD5	Data bit 6	In/Out
14	Ground	Ground	—
15	PD6	Data bit 7	In/Out
16	PBSY	Port busy	In
17	PD7	Data bit 8	In/Out
18	PE	Paper end	In
19	ACK*	Acknowledge	In
20	SLCT	Select	In

J5 – Floppy Disk Drive Connector

The VL-486-3 CPU card supports a standard 34-pin PC/AT style floppy disk interface at connector J5.

Caution Cable length must be 18” or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 30: Floppy Disk Interface Connector Pinout.

J5 Pin	Signal Name	Function
1	Ground	Ground
2	R/LC	Load Head
3	Ground	Ground
4	NC	No Connection
5	Ground	Ground
6	NC	No Connection
7	Ground	Ground
8	INDX*	Beginning Of Track
9	Ground	Ground
10	MTR1*	Motor Enable 1
11	Ground	Ground
12	DRV0*	Drive Select 0
13	Ground	Ground
14	DRE1*	Drive Select 1
15	Ground	Ground
16	MTR0*	Motor Enable 0
17	Ground	Ground
18	DIR	Direction Select
19	Ground	Ground
20	STEP*	Motor Step
21	Ground	Ground
22	WDAT*	Write Data Strobe
23	Ground	Ground
24	WGAT*	Write Enable
25	Ground	Ground
26	TRK0*	Track 0 Indicator
27	Ground	Ground
28	WPRT*	Write Protect
29	Ground	Ground
30	RDAT*	Read Data
31	Ground	Ground
32	HDSL	Head Select
33	Ground	Ground
34	DCHG	Drive Door Open

J6 – Interrupt Connector

A 10-pin header connector, J6, provides external access to four interrupt lines.

Table 31: Front Plane Interrupt Connector Pinout.

J6 Pin	Signal Name	Function
1	Ground	Ground
2	NC	No Connection
3	Ground	Ground
4	FP4*	Front Plane 4 Interrupt
5	Ground	Ground
6	FP6*	Front Plane 6 Interrupt
7	Ground	Ground
8	FP8*	Front Plane 8 Interrupt
9	Ground	Ground
10	FP10*	Front Plane 10 Interrupt

FP4* — Front Plane 4 Interrupt. This TTL input signal is used as a general purpose interrupt request input. If jumper V9[2-3] is inserted, a low level (or high-to-low transition) applied to the FP4* pin will request an interrupt via IRQ3. In DOS configuration, this will cause an INT 0Bh resulting in a dispatch through the interrupt vector at 000:002Ch.

FP6* — Front Plane 6 Interrupt. This TTL input signal is used as a general purpose interrupt request input. If jumper V10[2-3] is inserted, a low level (or high-to-low transition) applied to the FP6* pin will request an interrupt via IRQ11. In DOS configuration, this will cause an INT 0Bh resulting in a dispatch through the interrupt vector at 000:002Ch.

FP8* — Front Plane 8 Interrupt. This TTL input signal is used as a general purpose interrupt request input. If jumper V11[2-3] is inserted, a low level (or high-to-low transition) applied to the FP8* pin will request an interrupt via IRQ12. In DOS configuration this will cause an INT 74h resulting in a dispatch through the interrupt vector at 0000:01D0h.

FP10* — Front Plane 10 Interrupt. This TTL input signal is used as a general purpose interrupt request input. If jumper V12[2-3] is inserted, a low level (or high-to-low transition) applied to the FP10* pin will request an interrupt via IRQ15. In DOS configuration this will cause an INT 77h resulting in a dispatch through the interrupt vector at 0000:01DCh.

J7 – DMA CONTROL SIGNALS CONNECTOR

A 10-pin header connector, J7, provides external access to the on-board DMA channels.

Table 32: DMA Control Signals Connector Pinout.

J7 Pin	Signal Name	Function
1	Ground	Ground
2	FPRQ*	Front plane DRQ
3	Ground	Ground
4	FPAK*	Front plane DAK
5	Ground	Ground
6	XIWR*	Front plane WR
7	Ground	Ground
8	XIRD*	Front plane RD
9	Ground	Ground
10	TC*	Terminal Count

FPRQ* — Front Plane DMA Request. This TTL input signal is used to request DMA transfer cycles. If jumper V2 is inserted, a low level applied to the FPRQ* pin will initiate a 16-bit transfer using DMA channel 7. If jumper V2 is removed, an 8-bit transfer using DMA channel 3 is performed. FPRQ* should be held low until FPAK* makes a low-to-high transition.

FPAK* — Front Plane DMA Acknowledge. A low level on this TTL output signal indicates that the DMA controller has accepted a DMA request on the FPRQ* input signal and is preparing to transfer data. When FPAK* returns high, FPRQ* should be returned to the high state.

FPWR* — Front Plane DMA Write. A low level on this TTL output signal tells external equipment to latch data from the STD Bus. The DMA controller provides this data from a previous memory fetch.

FPRD* — Front Plane DMA Read. A low level on this TTL output signal tells external equipment to drive data onto the STD Bus. The DMA controller receives the data and saves it in memory.

TC* — Terminal Count. A low level on this TTL output signal indicates that the count register has decremented from 0000h to FFFFh, signaling completion of a block of DMA transfers.

L1 – Speaker Connector

Connector L1 is provided for connecting an 8Ω speaker to the card.

Table 33: Speaker Connector Pinout.

L1 Pin	Signal Name	Function
1	Timer 2 Out	Speaker drive
2	Ground	Ground

Register Descriptions 5

Introduction

This chapter lists all the user-programmable registers on the VL-486-3 CPU card. Programming information is included for VersaLogic specific registers only. Programming information for the standard PC/AT registers can be found in the *The Programmer's PC Sourcebook* or *The Undocumented PC* listed in "Other References" on page vii. Information on the registers internal to the CPU chip can be found in the TI486SXLC2 data book.

Register Summary

The tables in this section list all programmable registers on the VL-486-3 CPU card. They are organized in the following groups:

Table 34: Programmable Registers

Registers	Page
DMA 1 Controller	52
DMA 2 Controller	53
DMA Page	53
COM1 Serial Port	54
COM2 Serial Port	54
LPT1 Parallel Port	55
82C721 Configuration	55
Floppy Disk Drive Controller	55
IDE Hard Disk Drive Controller	56
Interrupt Controller (Master)	57
Interrupt Controller (Slave)	57
Counter/Timer	58
VersaLogic Registers	58

DIRECT MEMORY ACCESS — CHANNEL 1

Table 35: DMA 1 Controller Registers

Mnemonic	R/W	Address	Name
DMA0ADRA	R/W	0000h	DMA Channel 0 Current Address
DMA0CNTA	R/W	0001h	DMA Channel 0 Current Word Count
DMA1ADRA	R/W	0002h	DMA Channel 1 Current Address
DMA1CNTA	R/W	0003h	DMA Channel 1 Current Word Count
DMA2ADRA	R/W	0004h	DMA Channel 2 Current Address
DMA2CNTA	R/W	0005h	DMA Channel 2 Current Word Count
DMA3ADRA	R/W	0006h	DMA Channel 3 Current Address
DMA3CNTA	R/W	0007h	DMA Channel 3 Current Word Count
DMACSA	R/W	0008h	DMA Command/Status Register
DMARQA	R/W	0009h	DMA Request Register
DMAMASKA	R/W	000Ah	DMA Single Bit Mask Register
DMAMODEA	R/W	000Bh	DMA Mode Register
DMACBPA	R/W	000Ch	DMA Clear Byte Pointer
DMAMCA	R/W	000Dh	DMA Master Clear
DMACMA	R/W	000Eh	DMA Clear Mask Register
DMAWAMA	R/W	000Fh	DMA Write All Mask Register Bits

DIRECT MEMORY ACCESS — CHANNEL 2

Table 36: DMA 2 Controller Registers

Mnemonic	R/W	Address	Name
DMA0ADRB	R/W	00C0h	DMA Channel 0 Current Address
DMA0CNTB	R/W	00C2h	DMA Channel 0 Current Word Count
DMA1ADRB	R/W	00C4h	DMA Channel 1 Current Address
DMA1CNTB	R/W	00C6h	DMA Channel 1 Current Word Count
DMA2ADRB	R/W	00C8h	DMA Channel 2 Current Address
DMA2CNTB	R/W	00CAh	DMA Channel 2 Current Word Count
DMA3ADRB	R/W	00CCh	DMA Channel 3 Current Address
DMA3CNTB	R/W	00CEh	DMA Channel 3 Current Word Count
DMACSB	R/W	00D0h	DMA Command/Status Register
DMARQB	R/W	00D2h	DMA Request Register
DMAMASKB	R/W	00D4h	DMA Single Bit Mask Register
DMAMODEB	R/W	00D6h	DMA Mode Register
DMACBPB	R/W	00D8h	DMA Clear Byte Pointer
DMAMCB	R/W	00DAh	DMA Master Clear
DMACMB	R/W	00DCh	DMA Clear Mask Register
DMAWAMB	R/W	00DEh	DMA Write All Mask Register Bits
DMAWAXB	R/W	00DFh	DMA Write All Mask Register Bits X

DIRECT MEMORY ACCESS — PAGE REGISTERS

Table 37: DMA Page Registers

Mnemonic	R/W	Address	Name
DMA2PG	W	0081h	DMA Channel 2 Page Register
DMA3PG	W	0082h	DMA Channel 3 Page Register
DMA1PG	W	0083h	DMA Channel 1 Page Register
DMA0PG	W	0087h	DMA Channel 0 Page Register
DMA6PG	W	0089h	DMA Channel 6 Page Register
DMA7PG	W	008Ah	DMA Channel 7 Page Register
DMA5PG	W	008Bh	DMA Channel 5 Page Register
RAPREG	W	008Fh	Refresh Address Page Register

COM1 Serial Port

Table 38: COM1 Serial Port Registers

Mnemonic	R/W	Address	Name
RBRA	R	03F8h	Receiver Buffer Register A
THRA	W	03F8h	Transmit Holding Register A
DLLA	R/W	03F8h	Divisor Latch (LSB) A
IERA	R/W	03F9h	Interrupt Enable Register A
DLMA	R/W	03F9h	Divisor Latch (MSB) A
IIRA	R	03FAh	Interrupt Identification Register A
LCRA	R/W	03FBh	Line Control Register A
MCRA	R/W	03FCh	Modem Control Register A
LSRA	R	03FDh	Line Status Register A
MSRA	R	03FEh	Modem Status Register A
SCRA	R/W	03FFh	Scratchpad Register A

COM2 Serial Port

Table 39: COM2 Serial Port Registers

Mnemonic	R/W	Address	Name
RBRB	R	02F8h	Receiver Buffer Register B
THRB	W	02F8h	Transmit Holding Register B
DLLB	R/W	02F8h	Divisor Latch (LSB) B
IERB	R/W	02F9h	Interrupt Enable Register B
DLMB	R/W	02F9h	Divisor Latch (MSB) B
IIRB	R	02FAh	Interrupt Identification Register B
LCRB	R/W	02FBh	Line Control Register B
MCRB	R/W	02FCh	Modem Control Register B
LSRB	R	02FDh	Line Status Register B
MSRB	R	02FEh	Modem Status Register B
SCRB	R/W	02FFh	Scratchpad Register B

LPT1 Parallel Port

Table 40: LPT1 Parallel Port Registers

Mnemonic	R/W	Address	Name
LPRD	R	03BCh	Line Printer Read Data Register
LPWD	W	03BCh	Line Printer Write Data Register
LPS	R	03BDh	Line Printer Status Register
LPRC	R	03BEh	Line Printer Read Control Register
LPWC	W	03BEh	Line Printer Write Control Register

Chipset Registers

Table 41: 82C721 Configuration Registers

Mnemonic	R/W	Address	Name
CAR	R/W	03F0h	Configuration Access Register
CR0	R/W	03F1h	Configuration Register 0
CR1	R/W	03F1h	Configuration Register 1
CR2	R/W	03F1h	Configuration Register 2
CR3	R/W	03F1h	Configuration Register 3

Table 42: 82C836 Configuration Registers

Mnemonic	R/W	Address	Name
ICRI	W	0022h	Internal Register Index
ICRD	R/W	0023h	Internal Register Data

FLOPPY DISK DRIVE CONTROLLER

Table 43: Floppy Disk Drive Controller Registers

Mnemonic	R/W	Address	Name
FDCMSR	R	03F4h	Main Status Register
FDCDR	R/W	03F5h	Data Register
FDCST0	R	03F5h	Status Register 0
FDCST1	R	03F5h	Status Register 1
FDCST2	R	03F5h	Status Register 2
FDCST3	R	03F5h	Status Register 3
FDCDCR	W	03F2h	Drive Control Register
FDCDRR	W	03F7h	Data Rate Register
FDCFDR	R	03F7h	Fixed Disk Register

IDE HARD DISK DRIVE CONTROLLER

Table 44: IDE Hard Disk Drive Controller Registers

Mnemonic	R/W	Address	Name
IDEDR	R/W	01F0h	Data Register
IDEER	R	01F1h	Error Register
IDEWP	W	01F1h	Write Precompensation Register
IDESC	R/W	01F2h	Sector Count Register
IDESN	R/W	01F3h	Sector Number Register
IDECNL	R/W	01F4h	Cylinder Number Register Low
IDECNH	R/W	01F5h	Cylinder Number Register High
IDEDH	R/W	01F6h	Drive/Head Register
IDEST	R	01F7h	Status Register
IDECMD	W	01F7h	Command Register
IDEDIR	R	03F7h	Digital Input Register
IDEFDR	W	03F6h	Fixed Disk Register

Interrupt Controller — Master

Table 45: Master Interrupt Controller Registers

Mnemonic	R/W	Address	Name
ICW1A	W	0020h	Initialization Command Word 1
ICW2A	W	0021h	Initialization Command Word 2
ICW3A	W	0021h	Initialization Command Word 3
ICW4A	W	0021h	Initialization Command Word 4
OCW1A	W	0021h	Operation Command Word 1 (Interrupt Mask)
OCW2A	W	0020h	Operation Command Word 2 (Priority & Finish Control)
OCW3A	W	0020h	Operation Command Word 3 (Mode Control)
ISRA	R	0020h	In-Service Register
IRRA	R	0020h	Interrupt Request Register
IPWA	R	0020h	Interrupt Poll Word
IMRA	R	0021h	Interrupt Mask Register

Interrupt Controller — Slave

Table 46: Slave Interrupt Controller Registers

Mnemonic	R/W	Address	Name
ICW1B	W	00A0h	Initialization Command Word 1
ICW2B	W	00A1h	Initialization Command Word 2
ICW3B	W	00A1h	Initialization Command Word 3
ICW4B	W	00A1h	Initialization Command Word 4
OCW1B	W	00A1h	Operation Command Word 1 (Interrupt Mask)
OCW2B	W	00A0h	Operation Command Word 2 (Priority & Finish Control)
OCW3B	W	00A0h	Operation Command Word 3 (Mode Control)
ISRB	R	00A0h	In-Service Register
IRRB	R	00A0h	Interrupt Request Register
IPWB	R	00A0h	Interrupt Poll Word
IMRB	R	00A1h	Interrupt Mask Register

COUNTER/TIMERS

Table 47: Counter / Timer Registers

Mnemonic	R/W	Address	Name
T0CNT	R/W	0040h	Timer 0 Count Load/Read
T1CNT	R/W	0041h	Timer 1 Count Load/Read
T2CNT	R/W	0042h	Timer 2 Count Load/Read
TCW	W	0043h	Timer Control Word

MISCELLANEOUS

Table 48: Miscellaneous PC/AT-Style Registers

Mnemonic	R/W	Address	Name
CSP	R/W	0061h	Control/Status Port
RTCIDX	W	0070h	Real Time Clock Index and NMI Mask
RTCDP	R/W	0071h	Real Time Clock Data Port

SPECIAL CONTROL REGISTER

SCR (READ/WRITE) 00E0H

D7	D6	D5	D4	D3	D2	D1	D0
LED	Reserved	GP0	IPC	Reserved	Reserved	PM*	WDOGEN

Table 49: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	LED	**Light Emitting Diode** — Controls the on-board LED. LED = 0 Turns LED off. LED = 1 Turns LED on.
D6	—	**Reserved** — This bit has no function. Always reads as 0.
D5	GP0	**General Purpose Jumper Input** — This bit reflects the state of jumper V1[1-2]. GP0 = 0 Jumper in. GP0 = 1 Jumper out.
D4	IPC	**Interprocessor Communication** — Used to signal the attention of other CPU cards in a multiprocessor environment. IPC controls an open collector signal, TIPC*. Jumper block V6 configures the TIPC* signal to be carried on the STD Bus signal INTRQ* (P44). As an alternative, TIPC* can be carried on the STD Bus signal INTRQ4 (P05). An active low signal on this circuit (generated locally by writing a 0 to this bit, or received from the STD Bus) requests an interrupt on IRQ5. In DOS configuration, this causes an INT 0Dh resulting in a dispatch through the interrupt vector at 0000:0034h. IPC = 0 TIPC* signal is driven active low. IPC = 1 TIPC* released for other cards to drive.
D3	—	**Reserved** — This bit has no function. Always reads as 0.
D2	—	**Reserved** — This bit has no function. Always reads as 0.
D1	PM*	**Permanent Master** — This status bit reflects the state of jumper V7[7-8]. Writing to this bit has no effect. PM* = 0 Jumper in. PM* = 1 Jumper out.
D0	WDOGEN	**Watchdog Enable** — Enables and disables the watchdog timer reset circuit. WDOGEN = 0 Disables the watchdog timer. WDOGEN = 1 Enables the watchdog timer.

WATCHDOG TIMER HOLD-OFF REGISTER

WDHOLD (WRITE ONLY) 00E1H

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

A watchdog timer circuit is included on the CPU card to reset the CPU if proper software execution fails or a hardware malfunction occurs. The watchdog timer is enabled/disabled by writing to bit D0 of SCR

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (250 ms). Writing a 5Ah to WDHOLD resets the watchdog timeout period, preventing the CPU from being reset for the next 250 ms.

MAP AND PAGING CONTROL REGISTER

MPCR (READ/WRITE) 00E3H

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	FPAGE	Reserved	RPG3	RPG2	RPG1	RPG0

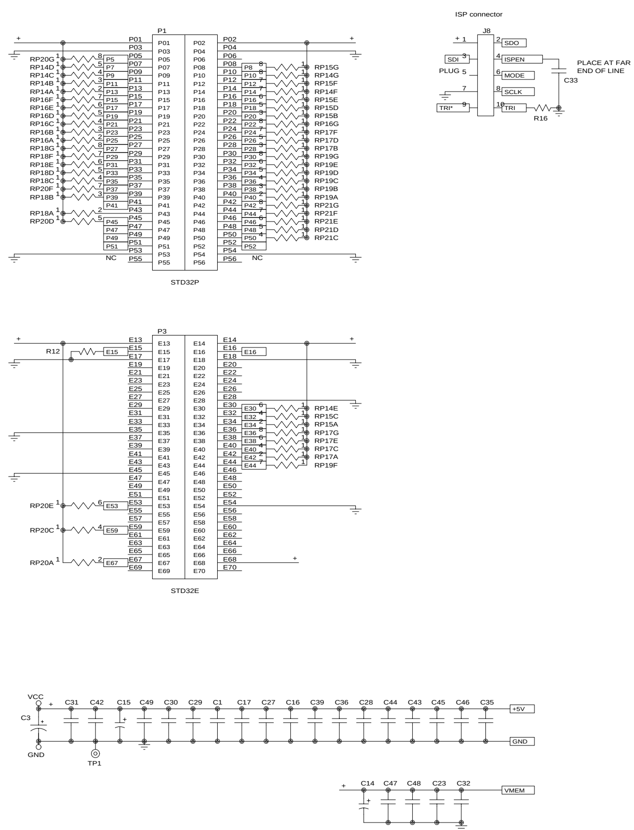
Table 50: Map and Paging Control Register Bit Assignments

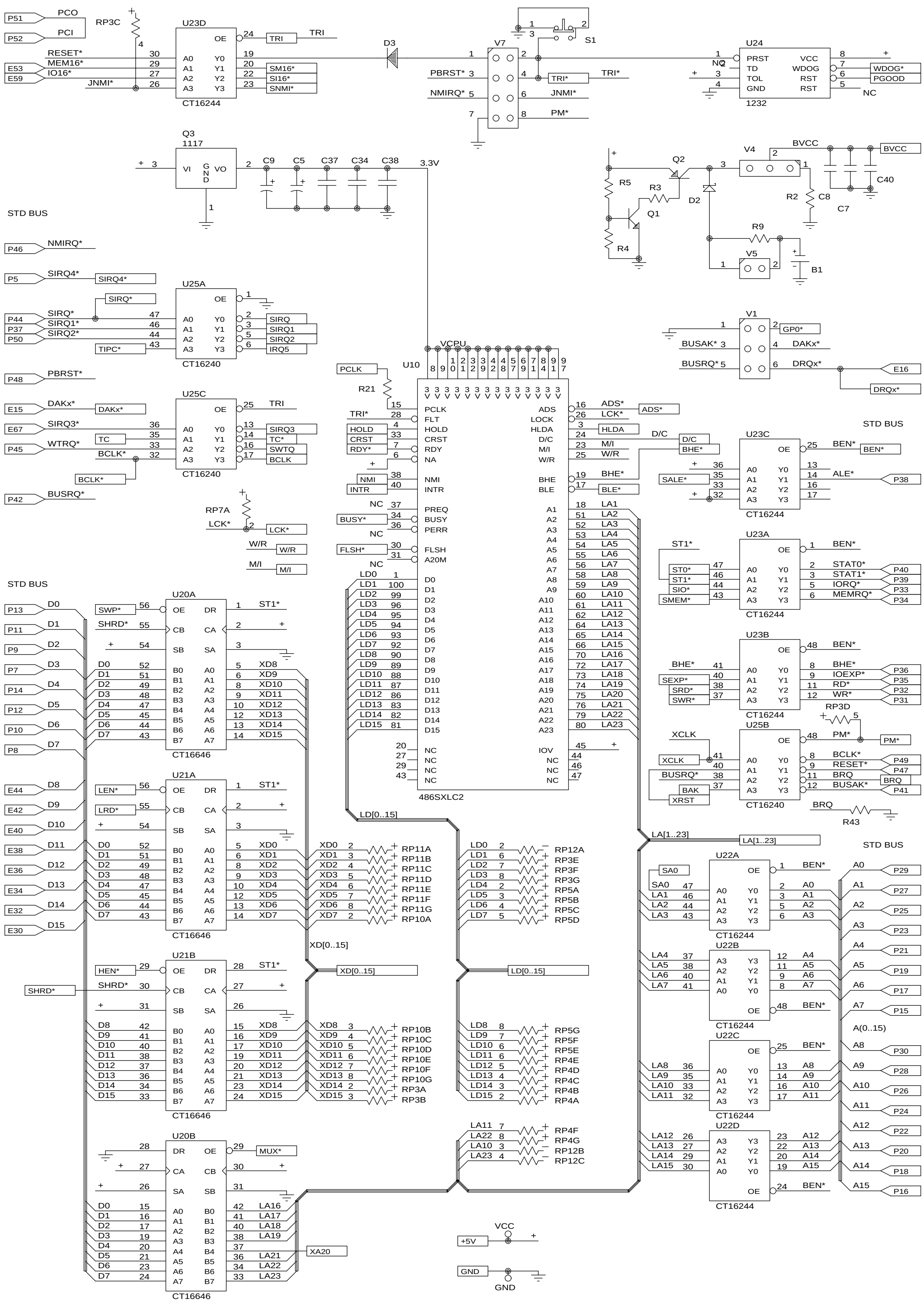
Bit	Mnemonic	Description
D7	—	**Reserved** — This bit has no function. Always reads as 0.
D6	—	**Reserved** — This bit has no function. Always reads as 0.
D5	FPAGE	**Flash Paging Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to the on-board ROM. FPAGE = 0 ROM Page Frame Disabled. FPAGE = 1 ROM Page Frame Enabled.
D4	—	**Reserved** — This bit has no function. Always reads as 0.
D3-D0	RPG3-RPG0	**ROM Page Select 3-0** — Selects which 64K block of ROM will be mapped into the ROM page frame.

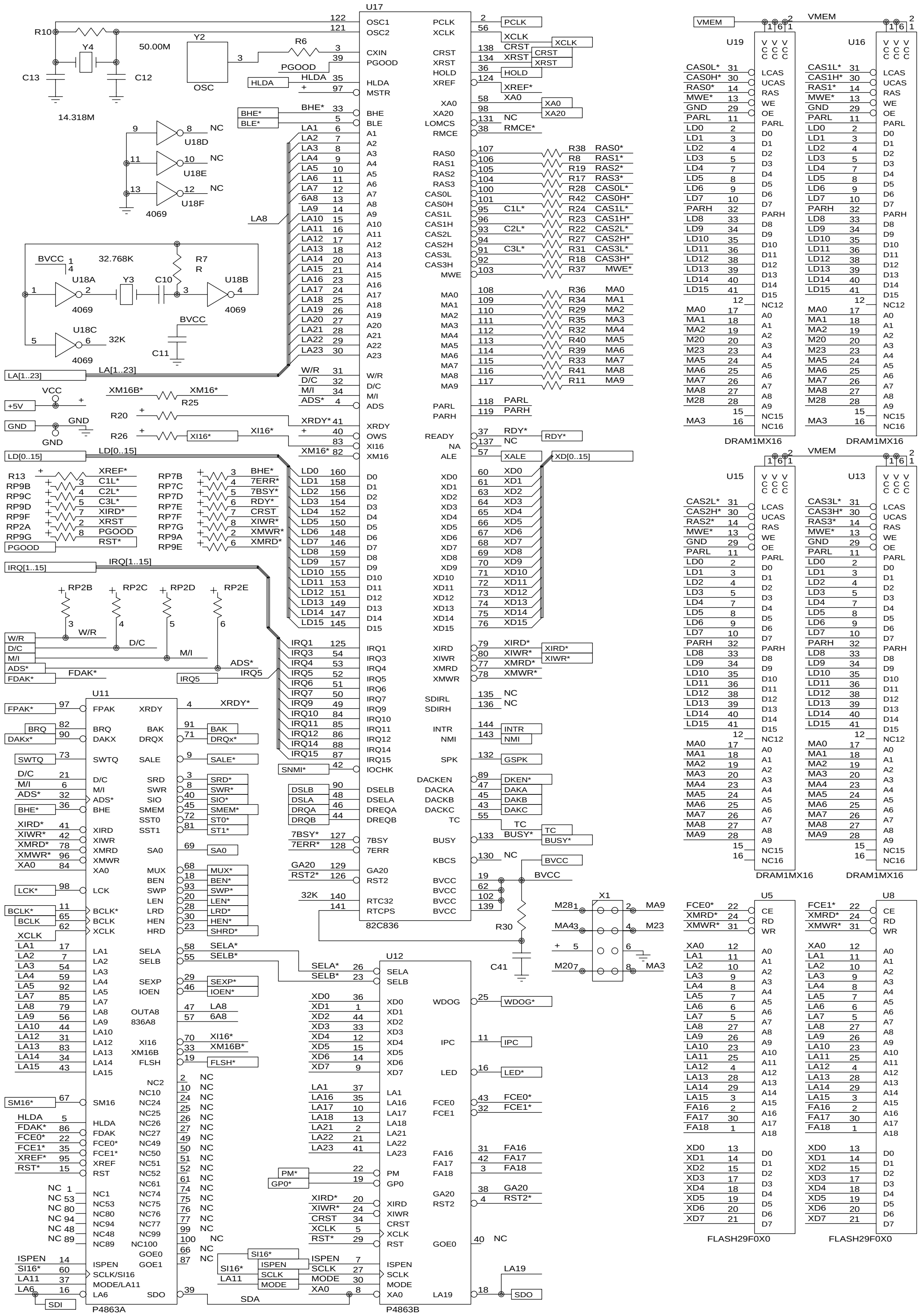
RPG3	RPG2	RPG1	RPG0	ROM Memory Range
0	0	0	0	00000h to 0FFFFh
0	0	0	1	10000h to 1FFFFh
0	0	1	0	20000h to 2FFFFh
0	0	1	1	30000h to 3FFFFh
0	1	0	0	40000h to 4FFFFh
0	1	0	1	50000h to 5FFFFh
0	1	1	0	60000h to 6FFFFh
0	1	1	1	70000h to 7FFFFh
1	0	0	0	80000h to 8FFFFh
1	0	0	1	90000h to 9FFFFh
1	0	1	0	A0000h to AFFFFh
1	0	1	1	B0000h to BFFFFh
1	1	0	0	C0000h to CFFFFh
1	1	0	1	D0000h to DFFFFh
1	1	1	0	E0000h to EFFFFh
1	1	1	1	F0000h to FFFFFh

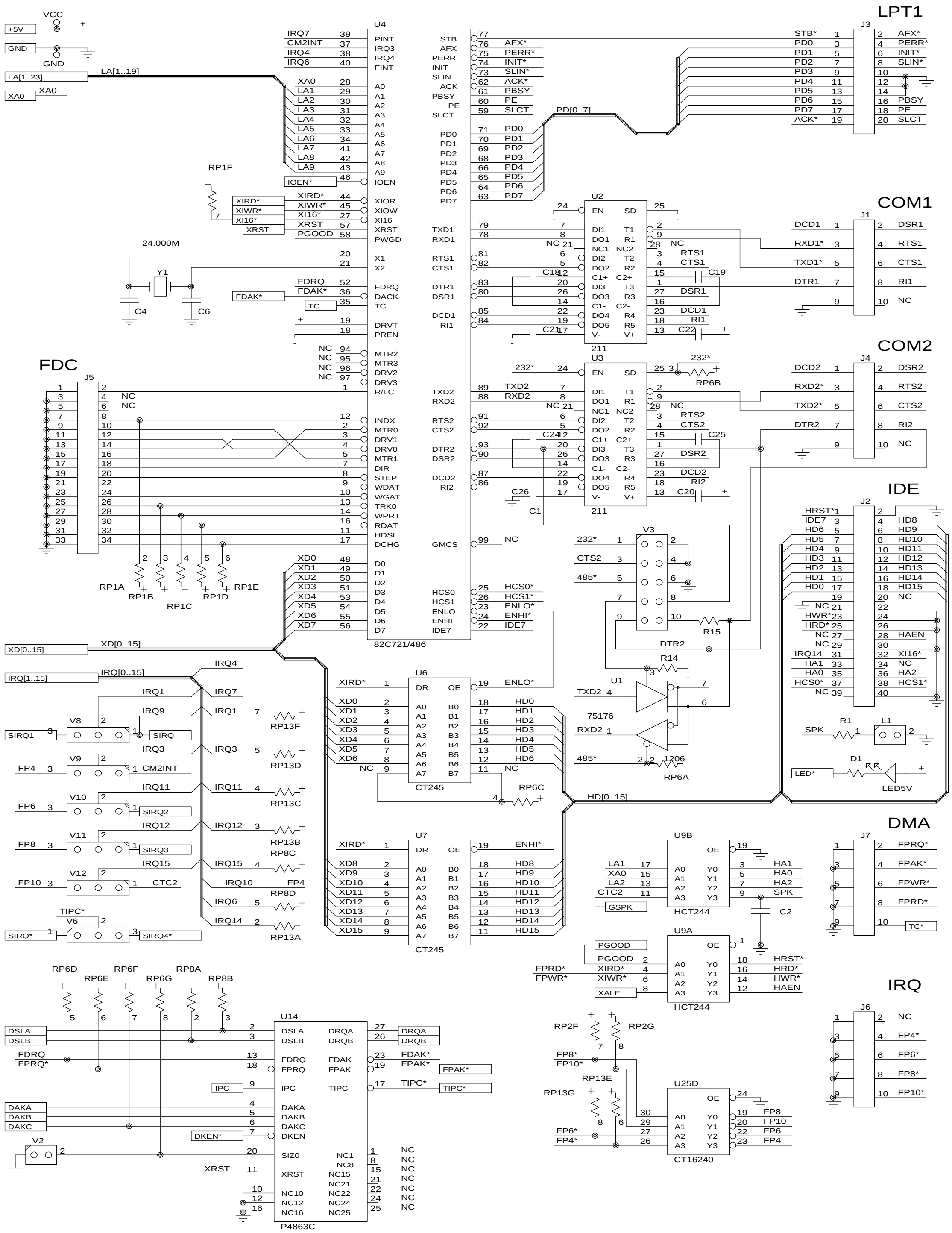
Appendix A — Schematic

A









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U9B
HCT244
U9A
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U14
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U25D
CT16240
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LED5V

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