Reference Manual

REV. 7/13/2017

Copperhead (VL-EBX-41)

Intel® 3rd Generation Core™ Quad or Dual Core SBC with Ethernet, HD Graphics, ACPI 4.0, SATA, RAID, USB, eUSB, mSATA, SUMIT, HD Audio, Serial, Analog + Digital I/O, and SPX

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Notice:

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VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

Product Release Notes

Rev 1.03 – Updated Web links

Rev 1.02 – Updated miniDisplayport cable information in Table 1

Rev 1.01 – Updated nominal battery voltage content

Updated CBR-5013 content in Table 2

Rev 1.0x – Commercial Release.

Support Page

The Copperhead support page, at **https://versalogic.com/support/product_support.asp?ProductID=231**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- Photograph of the circuit board
- BIOS information and upgrades

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

Table of Contents

1 Introduction

Description

The Copperhead (VL-EBX-41) is a feature-packed single board computer designed for OEM control projects requiring fast processing, industrial I/O, flexible memory options and designed-in reliability and longevity (product lifespan). Its features include:

- Intel® 3rd Generation Core™ CPU:
  - Core™ i7 Quad-Core (2.3 GHz) or
  - Core™ i7 Dual-Core (1.7 GHz) or
  - Core™ i3 Dual-Core (1.6 GHz) or
  - Celeron® Dual-Core (1.4 GHz)
- Up to 16 GB DDR3 socketed memory, two SO-DIMMs
- Intel QM77 Platform Controller Hub
- Two Intel 82574IT-based Ethernet interfaces, autodetect 10BaseT / 100BaseTX / 1000BaseT
- Intel HD 4000 graphics core with GPU Turbo Boost; DirectX 11, MPEG-2, H.264, and OGL 3.1 compliant; supports three independent displays
- Two DisplayPort interfaces, one VGA and one LVDS interface
- Four RS-232/422 serial ports
- Two SATA 6 Gb/s ports and two SATA 3 Gb/s ports
- RAID 0/1/5/10 support
- Ten USB 2.0 ports and two USB 3.0 ports
- One mSATA only socket
- One PCIe Mini Card/mSATA socket
- One eUSB bootable flash interface
- Industrial I/O
  - Sixteen 12-bit analog inputs
  - Eight 12-bit analog outputs
  - Thirty-two digital I/O lines
- Trusted Platform Module (option) for on-board security
- SPX interface supports up to four external SPI devices either of user design or any of the SPX™ series of expansion boards, with clock frequencies from 1-8 MHz
- Intel High Definition Audio (HDA) compatible. Stereo line in and line out.
- PCIe/104 Type 1 or SUMIT expansion
- EBX standard 5.75” x 8.00” footprint
- Field-upgradeable BIOS with OEM enhancements
- Customization available

The Copperhead is compatible with a variety of popular operating systems including Windows 7 (32- and 64-bit), XP (32-bit), WES (32- and 64-bit), Linux (32- and 64-bit), and VxWorks.

The Copperhead features high-reliability design and construction, including voltage sensing reset circuits and self-resetting fuses on the +5V and +3.3V supplies to the user I/O connectors.

Copperhead boards are subjected to 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service and product longevity for this exceptional SBC.

The Copperhead is equipped with a multifunction utility cable (breakout board) that provides standard I/O interfaces, including four USB ports, four serial ports, pushbutton reset, programmable LED, audio, and speaker. Additional I/O expansion is available through the stackable SUMIT and ISA connectors, PCIe Mini Card socket, and SPX expansion interface.

Technical Specifications

Board Size:
EBX standard: 5.75" x 8" (146 mm x 203 mm)

Storage Temperature:
-40°C to 85°C

Operating Temperature:
Standard temp. models: 0°C to +60°C
Industrial temp. models: -40°C to +85°C

Power Requirements: *(at +25°C and +12V running Windows 7 with 4 GB RAM, LVDS display, SATA, GbE, COM, and USB keyboard/mouse.)*
VL-EBXs-41SAK, EAF, VL-EBXe-41EHF: 7.6W idle, 20.7W typical, 33.7W max.
VL-EBXe-41SJF, EJP: 16.2W idle, 37.2W typical, 58.1W max.
VL-EBXe-41ELF, SLK: 8.8W idle, 14.4W typical, 20.0W max.
VL-EBXe-41SMK, EMF: 9.8W idle, 13.3W typical, 16.9W max.
+3.3V might be required by some expansion modules; +5V is needed when current above 4A is required for expansion modules

System Reset and Hardware Monitors:
All voltage rails monitored. Watchdog timer with programmable timeout. Push-button sleep, reset, and power.

DRAM:
Two SO-DIMM sockets, up to 16 GB DDR3 with up to 1600 MT/s

Video Interface:
Intel HD Graphics 4000 core
Analog output for VGA
Up to 2048x1536 at 75 MHz
LVDS output for TFT FPDs
18 bits RGB plus 3 bits timing control or
24 bits RGB plus 4 bits timing control
Two mini DisplayPort interfaces, one VGA, one LVDS

SATA Interface:
Two SATA 6 Gb/s ports
Two SATA 3 Gb/s ports

Flash Interface:
One 2 mm eUSB bootable device interface
One mSATA socket
One PCIe Mini Card / mSATA socket

Ethernet Interface:
Two Intel 82574IT based 10BaseT / 100BaseTX / 1000BaseT Ethernet Controllers

Analog Input:
16-channel, 12-bit, single-ended, 100 Ksps, channel independent input range: bipolar ±5, ±10, or unipolar 0 to +5V or 0 to +10V

Analog Output:
8-channel, 12-bit, single-ended, 100 Ksps, 0 to 4.096V

Serial Interface: (COM Ports)
Four RS-232/422 ports, 16C550 compatible, 921 Kbps max., 4-wire RS-232

USB:
Ten USB 2.0 host ports
Two USB 3.0 host ports

Audio:
Intel HD Audio, IDT 92HD75 HD audio CODEC
Stereo Line In and Stereo Line Out

SPX:
Supports four external SPI chips of user design or any SPX series expansion board

BIOS:
American Megatrends (AMI) Aptio UEFI Technology with OEM enhancements.
Field upgradeable with BIOS update utility

Bus Speed:
CPU: Intel i7 Dual-Core: 1.7 GHz, i7 Quad-Core: 2.3 GHz, i3 Dual-Core: 1.6 GHz, or Celeron Dual-Core: 1.4 GHz
DDR3: 1333 or 1600 MT/s
USB 2.0: 480 Mbps
USB 3.0: 5 Gbps
LPC: 33.33 MHz
PCIe/104: 100 MHz
SPX: 8 MHz max.

Bus Compatibility:
PCIe/104
SUMIT

Weight: *(no memory installed)*
VL-EBXs-41SAK – 0.861 lbs (0.390 kg)
VL-EBXs-41EAF – 1.238 lbs (0.561 kg)
VL-EBXe-41SJF – 1.268 lbs (0.575 kg)
Other models TBD

SUMIT Resources

Form Factor: EBX

	SUMIT A	SUMIT B
PCIe x1	1	2
PCIe x4		–
USB	4	
ExpressCard	–	
LPC	✓	
SPI / uWire	SPI	
SMBus/ I²C	SMBus	
+12V	✓	
+5V	✓	✓
+5Vsb	✓	✓
+3.3V	✓	✓

Specifications are typical at +25°C with +12V supply unless otherwise noted. Specifications are subject to change without notification.

Copperhead Block Diagram

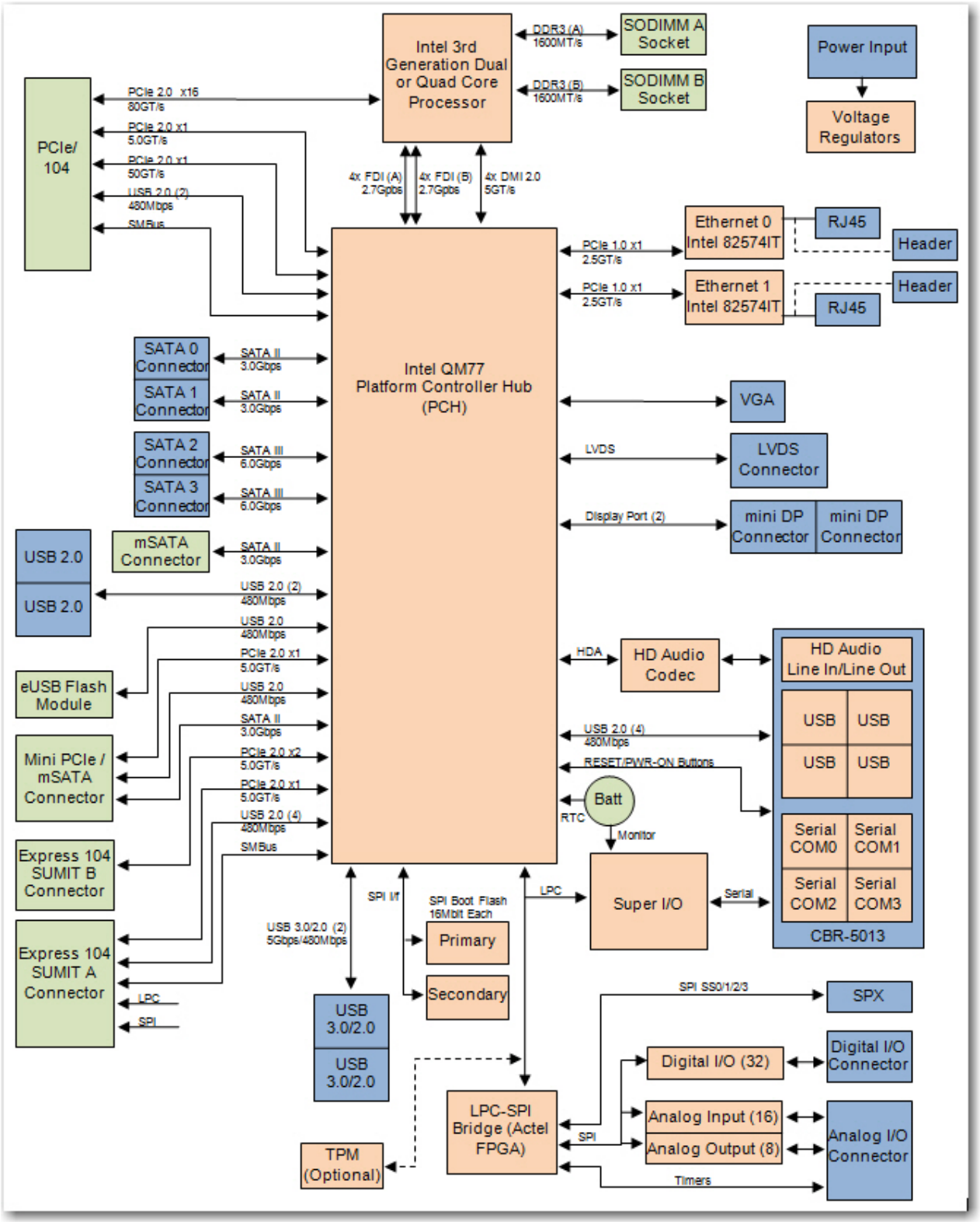

Figure 1. VL-EBX-41 Block Diagram

Thermal Considerations

CPU Die Temperature

The CPU die temperature is affected by numerous conditions, such as CPU utilization, CPU speed, ambient air temperature, air flow, thermal effects of adjacent circuit boards, external heat sources, and many others.

The CPU is protected from over-temperature conditions by several mechanisms, including Minimum Frequency Mode (MFM), coreclock modulation, and THERMTRIP#.

See the 3rd Generation Intel® Embedded Mobile Processor Datasheet, Vol. 1 for complete information on CPU thermal considerations.

As a failsafe, if the CPU die temperature climbs above +105°C, the CPU will turn itself off to prevent damage to the chip. Note that Intel does not warrant their CPUs in the event of this occurrence.

Model Differences

VersaLogic offers both commercial and industrial temperature models of the VL-EBX-41. The basic operating temperature specification for Copperhead models is shown below.

Thermal Solution	Temp. Range	Airflow
Heat plate	0°C to +60°C	Zero airflow
	-40°C to +85°C	125 Linear Feet per Minute (0.5 Linear Meters per Second)
Heat sink (fanless)	0°C to +60°C	125 Linear Feet per Minute (0.5 Linear Meters per Second)
Fan + heat sink	-40°C to +85°C	125 Linear Feet per Minute (0.5 Linear Meters per Second)

For heat plate only models, the customer-provided thermal solution must keep the heat plate below 90°C, measured top dead center of the heat plate. For example, for an 85°C ambient temperature, the thermal solution needs to:

- Dissipate 45W with a 5°C delta between ambient and the heat plate
- Thermal resistance = 0.11°C / W for the 45W unit

See Figure 6 for heat plate dimensions and mounting holes.

Warnings

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the VL-EBX-41.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner.

HANDLING CARE

Warning! Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of BIOS RAM to become corrupted through careless handling, resulting in BIOS resetting to factory defaults.

EARTH GROUND REQUIREMENT

Warning! All mounting holes (eight on EBX and EPIC boards, four on PC/104 boards) should be connected to earth ground (chassis ground). This provides proper grounding for ESD and EMI purposes. In portable applications, the mounting holes should be connected to the ground reference of the system power supply.

Technical Support

If you are unable to solve a problem after reading this manual, please visit the Copperhead Product Support web page below. The support page provides links to component datasheets, device drivers, and BIOS and PLD code updates.

Copperhead Support Page

The VersaTech KnowledgeBase contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the VL-EBX-41.

VersaTech KnowledgeBase

If you have further questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Please provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item (see Figure 8 for location)
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All approved non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning.

Configuration and Setup

2

Initial Configuration

The following components are recommended for a typical development system.

- VL-EBX-41 computer
- VL-PS-ATX12-300A – ATX power supply
- VGA or LVDS display
- USB keyboard
- USB mouse
- VL-HDS35-xxx – SATA hard drive
- USB CD-ROM drive
- VL-MM9-xxxx – DDR3 SO-DIMM module

The following VersaLogic cables are recommended.

- VL-CBR-1201 – VGA adapter cable, or
- VL-CBR-2010, 2011, or 2012 – LVDS cable
- VL-CBR-0701 – SATA data cable
- VL-CBR-0401 – ATX to SATA power cable
- VL-CBR-0808 – Main power cable

You will also need an operating system installation CD.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The VL-EBX-41 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the VL-EBX-41 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the VL-EBX-41 and their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

Figure 2 shows a typical start-up configuration.

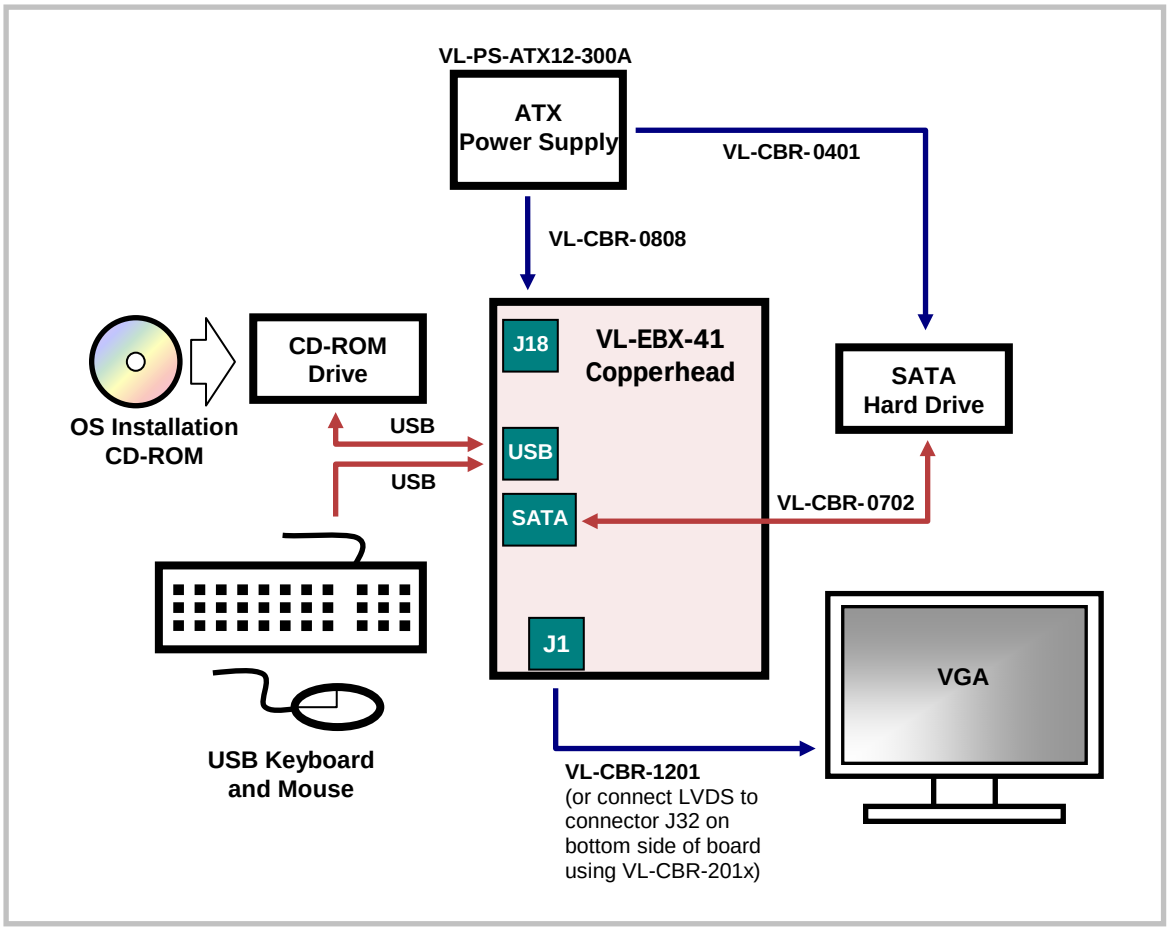

Figure 2. Typical Start-up Configuration

1. Install Memory

- Insert DDR3 DRAM module(s) into SO-DIMM sockets J2 and J33 and latch them into place.

2. Attach Cables and Peripherals

- Plug the either the VGA adapter cable VL-CBR-1201 into socket J1 or the LVDS adapter cable VL-CBR-201x into socket J32 (on the bottom of the board). Attach the adapter cable to the display.
- Plug the USB CD-ROM drive, keyboard, and mouse into on-board USB ports (J12, J13, J15, or J16).
- Plug the SATA data cable VL-CBR-0701 into a SATA socket (J3, J5, J7, or J9) and attach the SATA hard drive to the cable.
- Attach the ATX SATA power cable (VL-CBR-0401) to the ATX power supply and to the SATA hard drive.

3. Attach Power

- Plug the power adapter cable VL-CBR-0808 into connector J18.
  - Attach the 24-pin motherboard connector of the ATX power supply to the adapter.
  - Attach the 4-pin 12V CPU connector of the ATX power supply to the adapter. There will be 4 unused housing receptacles on the VL-CBR-0808, and keying will prevent incorrect insertion.

Warning! Do not use the six-pin (2x3) auxiliary power connector intended for PCI Express video cards.

4. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the VL-EBX-41 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the display. If the system is correctly configured, a video signal should be present.

6. Select a Boot Drive

- During startup, press the B key to display the boot menu. Insert the OS installation CD in the CD-ROM drive, and select to boot from the CD-ROM drive.

7. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

Note If you intend to operate the VL-EBX-41 under Windows XP or Windows XP Embedded, be sure to use Service Pack 3 (SP3) and all updates for full support of the latest hardware features.

CMOS Setup

See VersaLogic KnowledgeBase article VT1717 - Copperhead (VL-EBX-41 BIOS Setup Reference for complete information on CMOS Setup parameters.

Operating System Installation

The standard PC architecture used on the VL-EBX-41 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the VL-EBX-41 Product Support web page at https://versalogic.com/support/product_support.asp?ProductID=231.

Dimensions and Mounting

The VL-EBX-41 complies with all EBX standards which provide for specific mounting hole and PCIe/104 stack locations as shown in the diagram below.

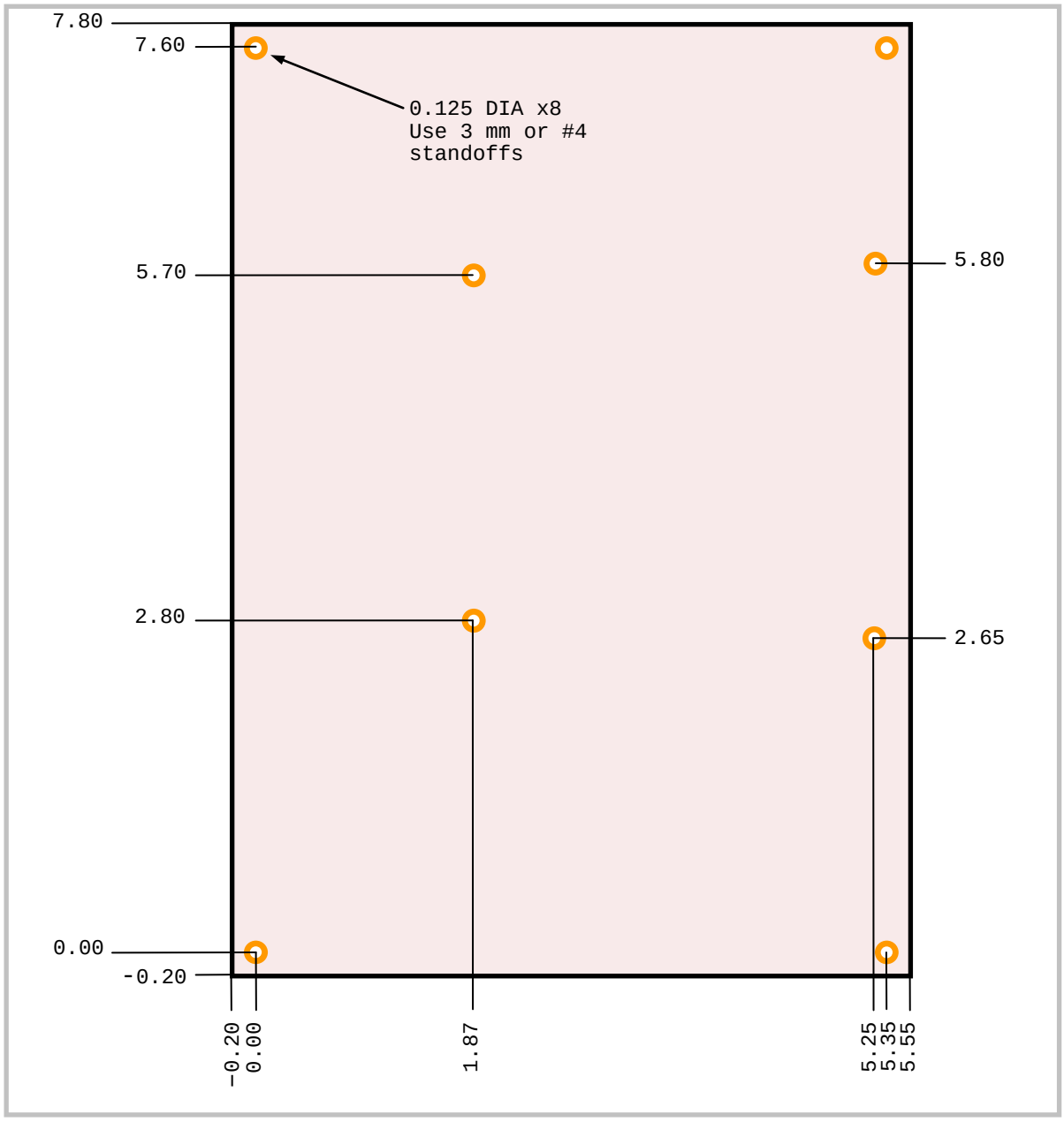

Figure 3. VL-EBX-41 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

Caution The VL-EBX-41 must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and de-mated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

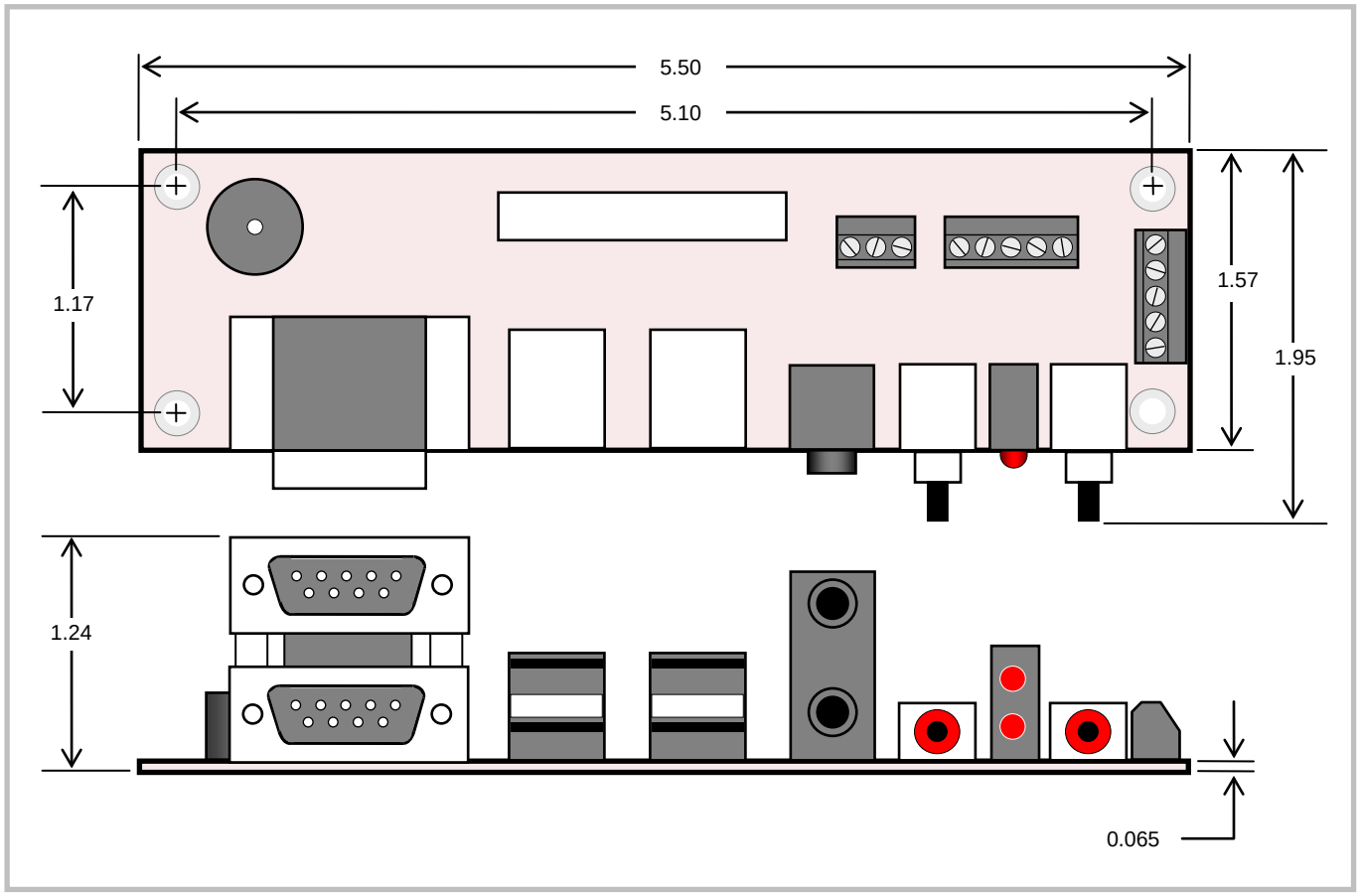

Figure 4. VL-CBR-5013 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

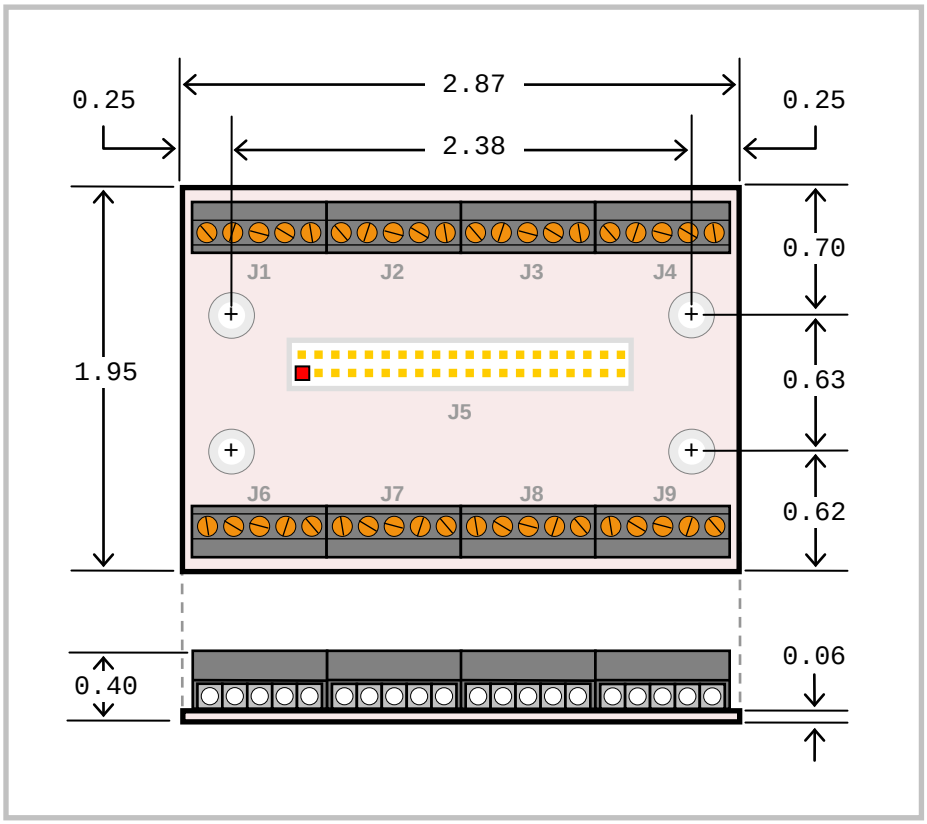

Figure 5. VL-CBR-4004 Dimensions and Mounting Holes

(Not to scale. All dimensions in inches.)

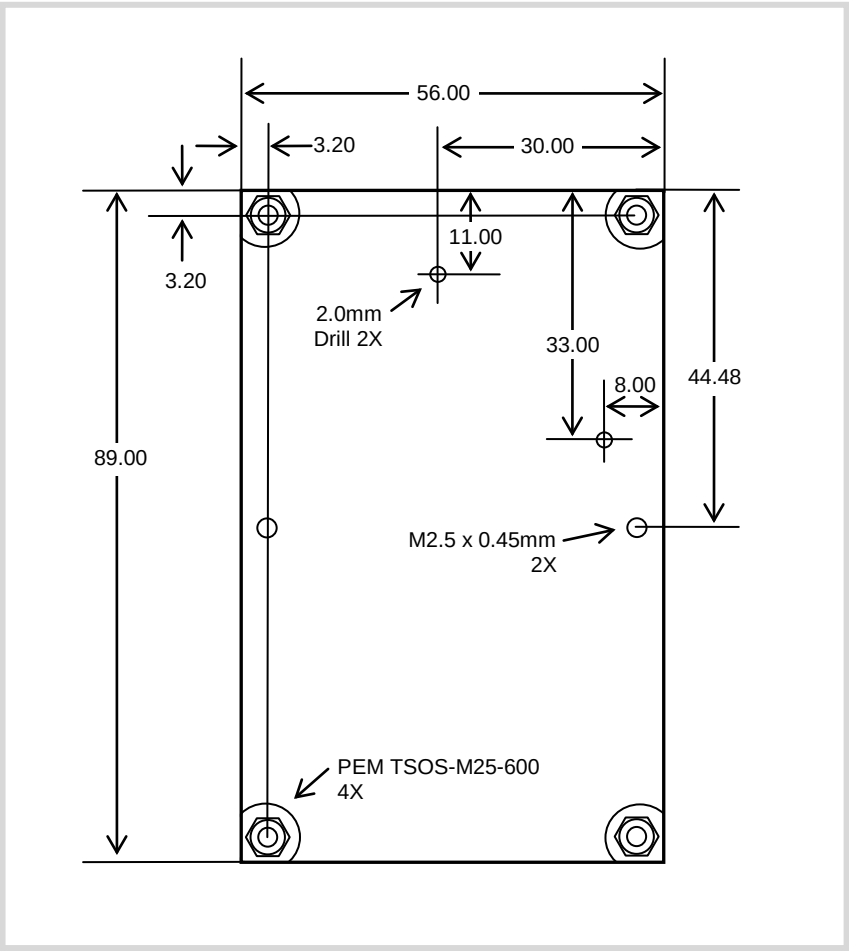

Figure 6. Heat Plate Dimensions and Mounting Holes

(Not to scale. All dimensions in millimeters.)

HARDWARE ASSEMBLY

The VL-EBX-41 mounts on four hardware standoffs using the corner mounting holes (A). These standoffs are secured to the underside of the circuit board using pan head screws.

Four additional standoffs (B) must be used under the circuit board to prevent excessive flexing when expansion modules are mated and separated. These are secured with four male-female standoffs (C), threaded from the top side, which also serve as mounting struts for the expansion stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing.

An extractor tool is available (part number VL-HDW-203) to separate expansion modules from the stack.

Note Standoffs and screws are available as part number VL-HDW-105 (metric M3 thread) or VL-HDW-106 (English thread).

Note Where possible, all eight mounting standoffs should be connected to earth ground (chassis ground). This provides proper grounding for ESD and EMI protection.

STANDOFF LOCATIONS

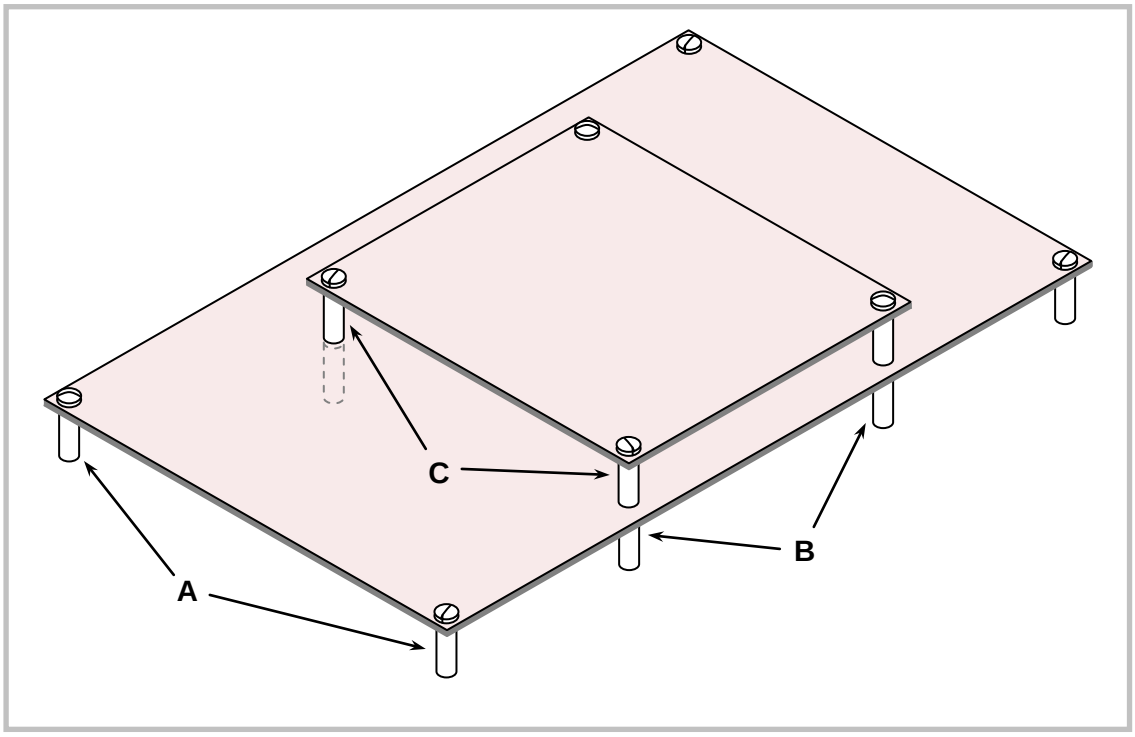

Figure 7. Standoff Locations

External Connectors

VL-EBX-41 Connector Locations – Top

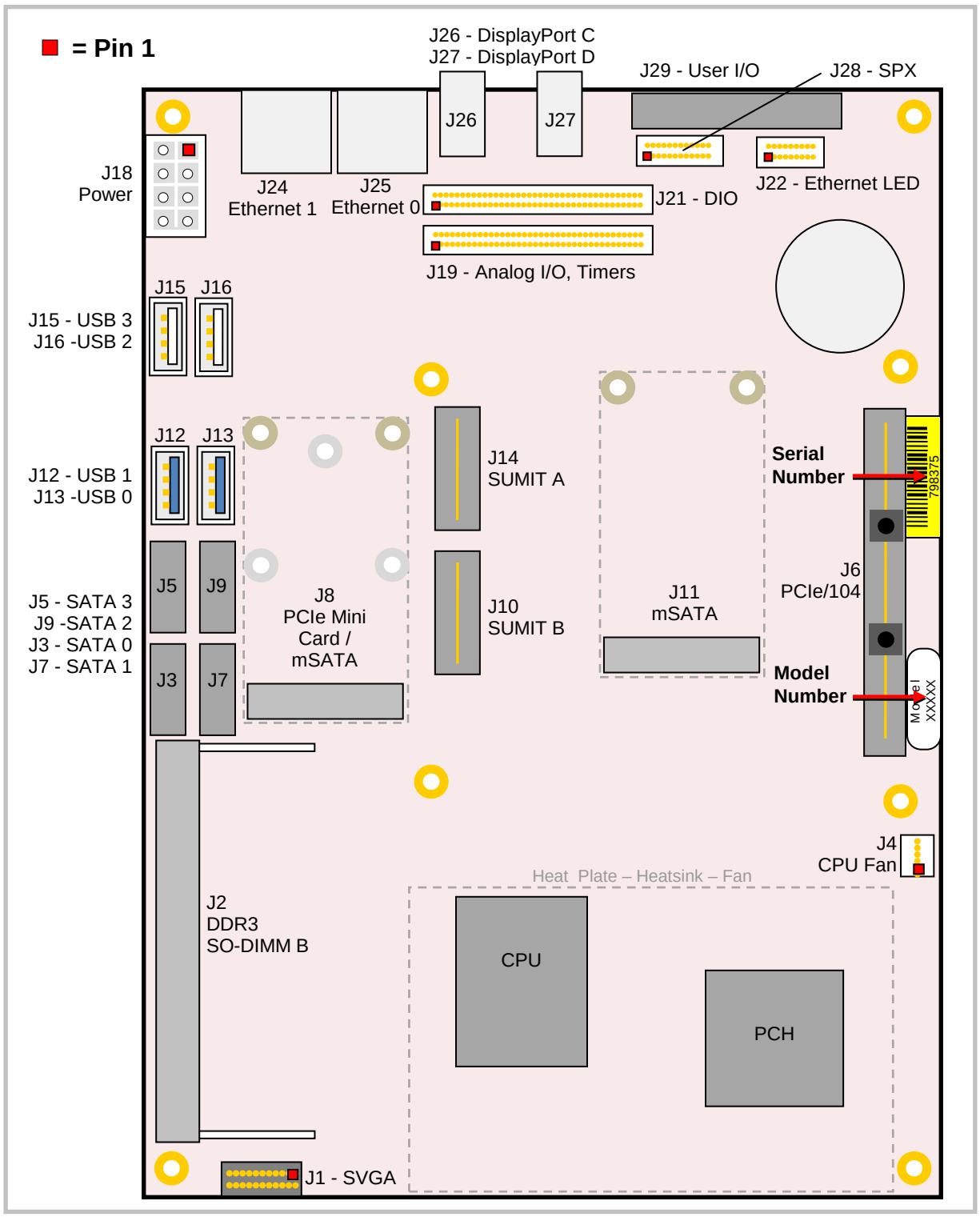

Figure 8. VL-EBX-41 Connector Locations - Top

VL-EBX-41 Connector Locations – Bottom

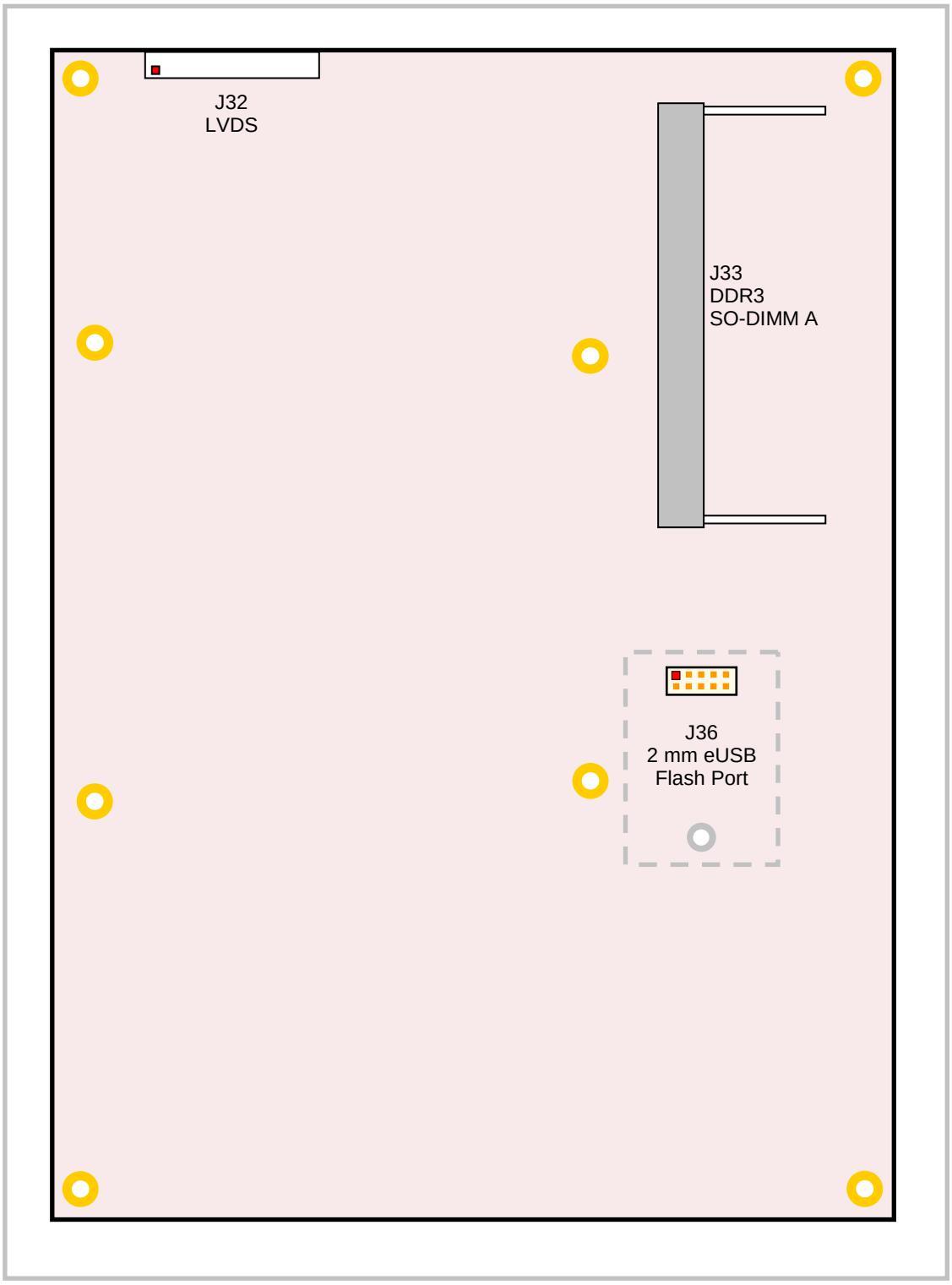

Figure 9. VL-EBX-41 Connector Locations - Bottom

VL-EBX-41 CONNECTOR FUNCTIONS AND INTERFACE CABLES

The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector[1]	Function	Mating Connector	Transition Cable	Cable Description	Page
J1	VGA Video Output	FCI 89361-712LF or FCI 89947-712LF	VL-CBR-1201	12" 12-pin 2 mm IDC to 15-pin HD D-Sub VGA	28
J2	DDR3 SO-DIMM B	(DDR3 RAM)	—	—	24
J3	SATA 0 (6 GB/s)	Standard SATA	VL-CBR-0702; VL-CBR-0401	20" SATA data, latching; ATX to SATA power adapter	31
J4	CPU Fan	—	—	Fan power cable with 3-pin connector	—
J5	SATA 3 (3 GB/s)	Standard SATA	VL-CBR-0702; VL-CBR-0401	20" SATA data, latching; ATX to SATA power adapter	31
J6	PCIe/104	—	—	—	26
J7	SATA 1 (6 GB/s)	Standard SATA	VL-CBR-0702; VL-CBR-0401	20" SATA data, latching; ATX to SATA power adapter	31
J8	PCIe Mini Card / mSATA	—	—	—	47
J9	SATA 2 (3 GB/s)	Standard SATA	VL-CBR-0702; VL-CBR-0401	20" SATA data, latching; ATX to SATA power adapter	31
J10	SUMIT B Top	Samtec ASP-129646-01	—	—	26
J11	mSATA	—	—	—	31
J12	USB1 3.0	Standard USB Type A	—	—	35
J13	USB0 3.0	Standard USB Type A	—	—	35
J14	SUMIT A Top	Samtec ASP-129646-01	—	—	26
J15	USB3 2.0	Standard USB Type A	—	—	35
J16	USB2 2.0	Standard USB Type A	—	—	35
J18	Main Power Input	Molex 39-01-2080 Molex 39-00-0181 (8 ea.)	VL-CBR-0808	12” ATX12 power cable to Copperhead	23
J19	Analog I/O, Timers	FCI 89361-340LF	VL-CBR-4004A	12” 2 mm 40-pin to 40-pin IDC to VL-CBR-4004 board	37, 39, 47
J21	Digital I/O 1-32	FCI 89361-340LF	VL-CBR-4004A	12” 2 mm 40-pin to 40-pin IDC to VL-CBR-4004 board	41
J22	Ethernet LED	—	—	—	34
J24	Gigabit Ethernet 1	RJ45	—	—	33
J25	Gigabit Ethernet 0	RJ45	—	—	33
J26	mini DisplayPort C	—	VL-CBR-2031 VL-CBR-2033	36” miniDisplayPort to MiniDisplayPort miniDisplayPort to HDMI Active Adapter, 6” (Commercial Temp. video only)	29
J27	mini DisplayPort D	—	VL-CBR-2031 VL-CBR-2033	36” miniDisplayPort to MiniDisplayPort miniDisplayPort to HDMI Active Adapter, 6” (Commercial Temp. video only)	29

Connector[1]	Function	Mating Connector	Transition Cable	Cable Description	Page
J28	SPX	FCI 89361714LF	VL-CBR-1401; VL-CBR-1402	2 mm 14-pin IDC, 2 or 4 SPX device cable	53
J29	COM ports, USB, PLED, power LED, push-button reset, power button, audio jacks, PC speaker	Oupiin 1204-50G00B2A	VL-CBR-5013A	18" 1.27 mm IDC 50-pin to 50-pin	50
J32	LVDS	20-pin, PanelMate 1.25mm	VL-CBR-2010; VL-CBR-2011; VL-CBR-2012 (24-bit)	18-bit TFT FPD using 20-pin Hirose 18-bit TFT FPD using 20-pin JAE	28
J33	DDR3 SO-DIMM A	(DDR3 RAM)	—	—	24
J36	eUSB Flash Drive	2 mm eUSB flash module	—	—	33

1. Connectors are not installed at locations J20, J23, J30 and J31 (alternate latching Ethernet). Connectors J17, J34, and J35 are for factory use only.
2. The PCB origin is the mounting hole to the lower left as shown in Figure 3 (lower right when viewing bottom side of board).
3. Connectors J32, J34, and J35 are on the bottom of the board.

VL-CBR-5013 Connector Locations

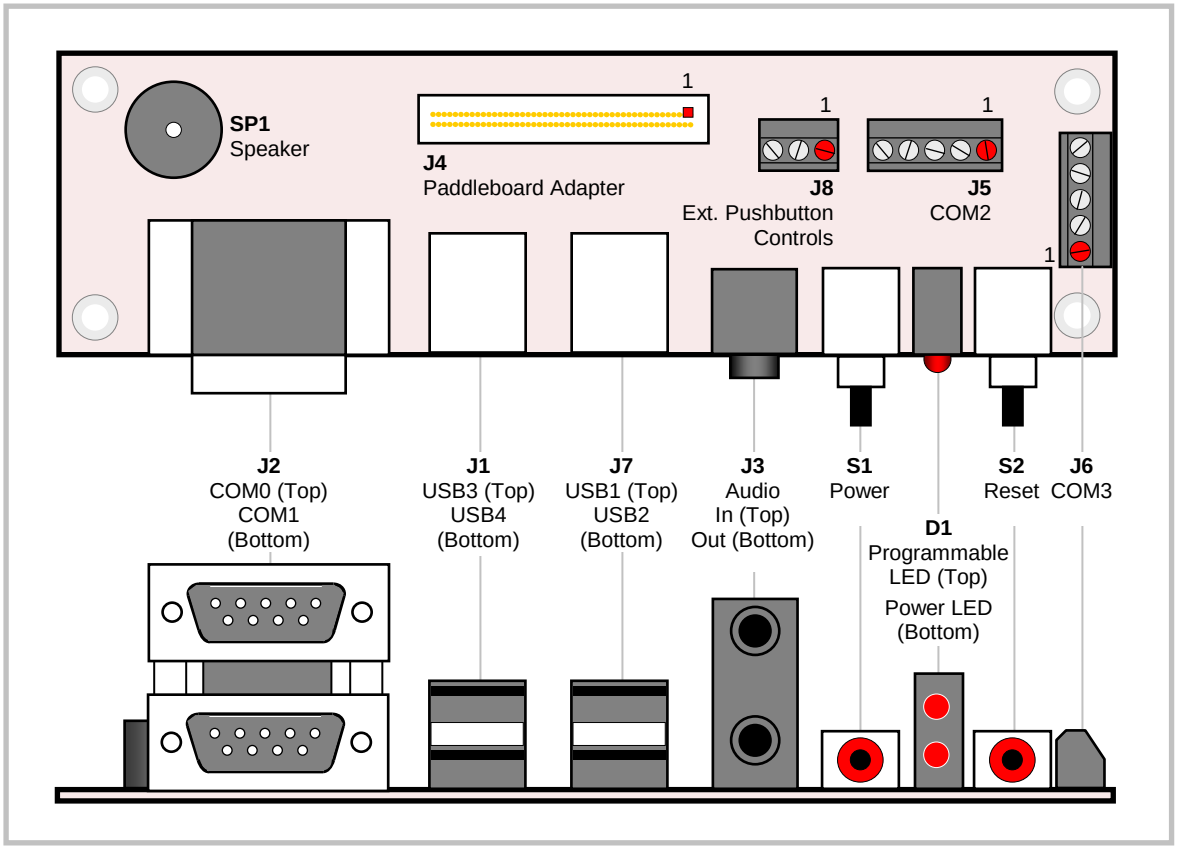

Figure 10. VL-CBR-5013 Connectors

VL-CBR-5013 Connector Functions

Table 2: VL-CBR-5013 Connector Functions

Connector	Function	PCB Connector	Description
J1	USB3, USB4	USB Type A	USB Host
J2	COM0, COM1	Kycon K42-E9P/P-A4N	Dual DB-9 male
J3	Audio In/Out	3.5 mm dual audio jack	–
J4	High Density Connector	FCI 20021511-00050T1LF Oupiin 3216-A50G00SBA Samtec SHF-125-01-F-D-TH	1.27 mm, 50-pin, keyed header
J5	COM2	Conta-Clip 10250.4	5-pin screw terminal
J6	COM3	Conta-Clip 10250.4	5-pin screw terminal
J7	USB1, USB2	USB Type A	USB Host
J8	External Reset and Power Buttons	Conta-Clip 10250.4	3-pin screw terminal
D1	PLED (Top), Power LED (Bottom)	LED	–
S1	Power Button	Pushbutton	–
S2	Reset Button	Pushbutton	–
SP1	Speaker	Piezo speaker	–

VL-CBR-4004 Connector Locations

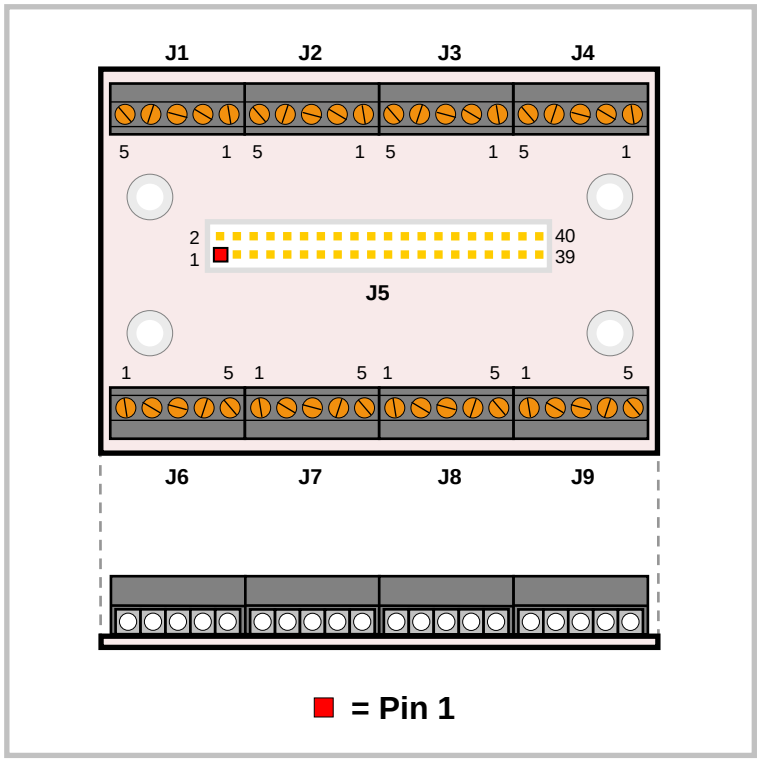

Figure 11. VL-CBR-4004 Connectors

The VL-CBR-4004 can be attached to connector J19 (analog I/O, timers) and connector J21 (digital I/O).

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION

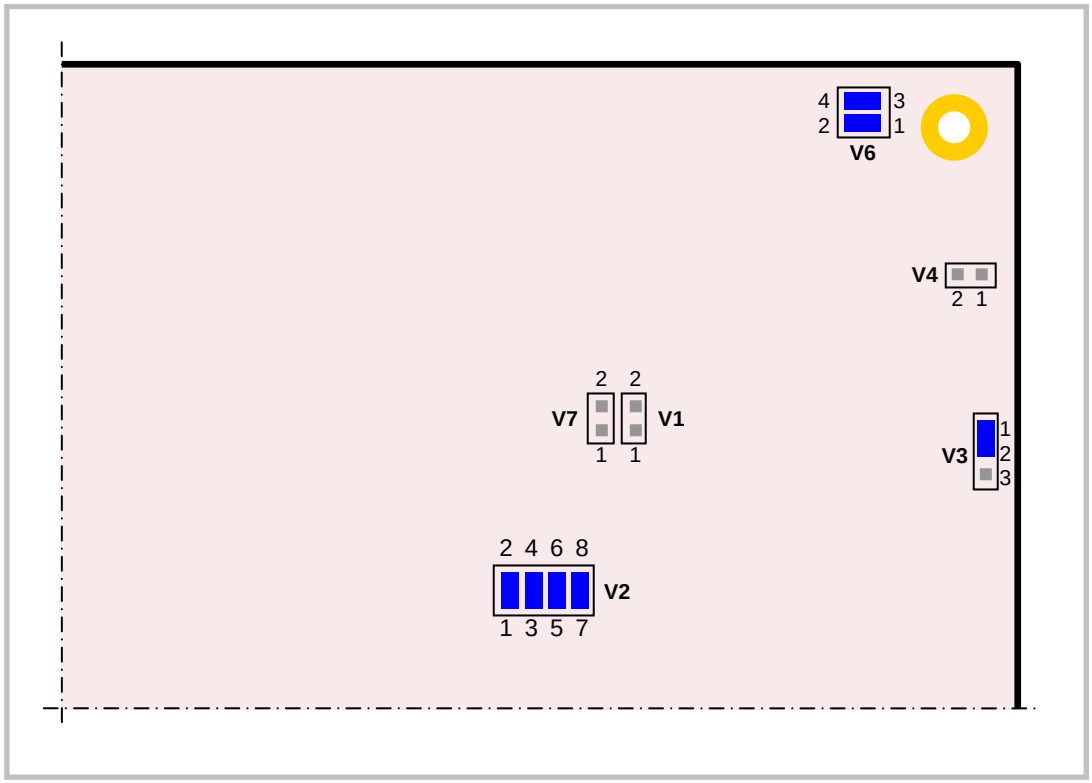

Figure 12. Jumper Block Locations

JUMPER SUMMARY

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**Clear Non-Volatile RAM (NVRAM)** In – Clear NVRAM Out – Normal operation **Note:** Whenever NVRAM cleared it is good practice to clear CMOS RAM (using Jumper V3) at the same time.	Out	25
V2[1-2]	**COM0 RS-422 Rx Termination** In – 120 Ohm terminated Out – COM1 not terminated	In	35
V2[3-4]	**COM1 RS-422 Rx Termination** In – 120 Ohm terminated Out – COM2 not terminated	In	35
V2[5-6]	**COM2 RS-422 Rx Termination** In – 120 Ohm terminated Out – COM3 not terminated	In	35
V2[7-8]	**COM3 RS-422 Rx Termination** In – 120 Ohm terminated Out – COM4 not terminated	In	35
V3	**CMOS RAM and Real-time Clock Erase** [1-2] In – Normal [2-3] In – Erase CMOS RAM and real-time clock **Note:** Whenever CMOS RAM is cleared it is good practice to clear NVRAM (using jumper V1[1-2]) at the same time.	[1-2] In	25
V4	**BIOS Force Recovery** In – Enable Out – Disable	Out	—
V5	**Jumper block not installed**	—	—
V6[1-2]	**System BIOS Selector** In – Primary system BIOS selected Out – Secondary system BIOS selected The Primary system BIOS is field upgradeable using the BIOS upgrade utility. See https://versalogic.com/support/product_support.asp?ProductID=231 for more information.	In	61
V6[3-4]	**General Purpose Input** In – Causes the GPI_JMP bit in the BIOS and Jumper Status Register (BIOSJSR) at I/O port CA2h to read as '1' Out – Causes the GPI_JMP bit in the BIOS and Jumper Status Register (BIOSJSR) at I/O port CA2h to read as '0'	In	61
V7[1-2]	**MM# Jumper** In – Test BIOS Out – Normal operation	Out	—

Power Supply

POWER CONNECTOR

Main power is applied to the Copperhead through an 8-pin polarized connector at location J18.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use all pins to prevent excess voltage drop.

Table 4: Main Power Connector Pinout

J18 Pin	Signal Name	Description
1	GND	Ground
2	GND	Ground
3	$+12V_{DC}$	Power Input
4	$+3.3V_{DC}$	Power Input
5	9-15V	Power Input
6	9-15V	Power Input
7	GND	Ground
8	$+5V_{DC}$	Power Input

POWER REQUIREMENTS

The Copperhead requires an input voltage of 9-15V for proper operation. Power to the PCIe/104 and SUMIT expansion slots (+12V, +5V[see note], and +3.3V) is not provided by voltage regulators on the Copperhead circuit board. These voltages, if needed, must be provided externally by the user. The Copperhead circuit board passes the voltages from connector J18 to the expansion slots.

Note: Up to 4A @ 5V is provided from an on-board supply. If additional amperage is needed (8.4A max) , an external supply must be used.

The exact power requirement of the VL-EBX-41 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices.

POWER DELIVERY CONSIDERATIONS

Using the VersaLogic approved power supply (VL-PS-ATX12-300A) and power cable (VL-CBR-0808) will ensure high quality power delivery to the board. Customers who design their own power delivery methods should take into consideration the guidelines below to ensure good power connections.

Also, the specifications for typical operating current do not include any off-board power usage that may be fed through the VL-EBX-41 power connector. Expansion boards and USB devices plugged into the board will source additional power through the VL-EBX- 41 power connector.

- Do not use wire smaller than 18 AWG. Use high quality UL 1007 compliant stranded wire.
- The length of the wire should not exceed 18".
- Avoid using any additional connectors in the power delivery system.
- The power and ground leads should be twisted together, or as close together as possible to reduce lead inductance.
- A separate conductor must be used for each of the power pins.
- All power input pins and all ground pins must be independently connected between the power source and the power connector.
- Use a high quality power supply that can supply a stable voltage while reacting to widely varying current draws.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Nominal battery voltage is 3.0V. If the voltage drops below 2.7V, contact the factory for a replacement (part number HB3/0-1). The life expectancy under normal use is approximately 10 years.**Note:** The Copperhead can operate normally with low battery voltage (or no battery installed), however the date/time will not be maintained when the power is turned off.

CPU

The Copperhead features 3rd Generation Intel® Core™ Embedded Mobile Processors (code named Ivy Bridge), including the i7, i3 and Celeron. The Intel® Core™ processor family are a 64-bit, multi-core processors built on 22-nanometer process technology. They include a memory controller, a point-to-point Direct Media Interface (DMI) for PCH connectivity, and two Flexible Display Interface (FDI) channels to support legacy display in the PCH. For more CPU information see the Copperhead support page.

System RAM

COMPATIBLE MEMORY MODULES

The Copperhead accepts two 204-pin SO-DIMM memory modules with the following characteristics:

- Size — Up to 16 GB total or 8 GB per module, supports 1333 and 1600 MT/s
- Voltage — 1.35V
- Type — DDR3 (VersaLogic VL-MM9 Series modules)

Clearing Non-volatile RAM (NVRAM)

You can clear NVRAM and reset the BIOS settings to factory defaults by following the instructions below.

1. Power off the Copperhead.
2. Install a jumper on V1[1-2].
3. Power on the Copperhead and wait 10 seconds or more.
4. Power off the Copperhead.
5. Remove the jumper from V1[1-2]. The board will not boot if you do not remove this jumper.
6. Power on the Copperhead.

Note: Whenever NVRAM cleared, it is good practice to clear CMOS RAM (using Jumper V3) at the same time.

CMOS RAM

CLEARING CMOS RAM AND RTC

A jumper may be installed into V3[2-3] to erase the contents of the CMOS RAM and the Real-Time Clock. When clearing CMOS RAM:

1. Power off the Copperhead.
2. Remove the jumper from V3[1-2], install it on V3[2-3] and leave it for four seconds.
3. Move the jumper back to V3[1-2].
4. Power on the Copperhead.

Note: Whenever CMOS RAM is cleared, it is good practice to clear NVRAM (using jumper V1[1-2]) at the same time.

Real-time Clock

The Copperhead features a battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

CMOS Setup (accessed by pressing the Delete key during a system boot) can be used to set the time/date of the real-time clock.

Expansion Bus

PCIe/104

The PCIe/104 bus (connector J6) provides a PCIe x16 lane and two x1 lanes for add-on card expansion. It supports both PCIe Gen1 and Gen2. Gen1 has a data rate of 2.5 GT/s and a bandwidth of 250 MB/s. Gen2 has a data rate of 5.0 GT/s and a bandwidth of 500 MB/s. See the PCI/104-Express & PCIe/104 Express Specification for signal details.

SUMIT

The SUMIT A Top and SUMIT B Top connectors (J14 and J10, respectively) provide a subset of the PCI Express functionality, as shown in Table 5 and Table 6. See the SUMIT Specification for a complete description of the SUMIT interface.

Table 5: SUMIT A Top Connector Pinout

J14 Pin	Signal Name	Function	J14 Pin	Signal Name	Function
1	+5VSB	+5V power	2	+12V	+12V power
3	3.3V	+3.3V power	4	SMB/I2C_DATA	SMBus data
5	3.3V	+3.3V power	6	SMB/I2C_CLK	SMBus clock
7	NC	Not connected	8	SMB/I2C_ALERT#	SMBus interrupt line in
9	NC	Not connected	10	SPI/uWire_DO	SPI data out from master
11	NC	Not connected	12	SPI/uWire_DI	SPI data in to master
13	NC	Not connected	14	SPI/uWire_CLK	SPI clock
15	+5V	+5V power	16	SPI/uWire_CS0#	SPI chip select 0
17	USB3+	USB3 data +	18	SPI/uWire_CS1#	SPI chip select 1
19	USB3-	USB3 data –	20	NC	Not connected
21	+5V	+5V power	22	NC	Not connected
23	USB2+	USB2 data +	24	LPC_AD0	LPC line 0
25	USB2-	USB2 data –	26	LPC_AD1	LPC line 1
27	+5V	+5V power	28	LPC_AD2	LPC line 2
29	USB1+	USB1 data +	30	LPC_AD3	LPC line 3
31	USB1-	USB1 data –	32	LPC_FRAME#	LPC frame
33	+5V	+5V power	34	SERIRQ#	Serial IRQ legacy
35	USB0+	USB0 data +	36	NC	Not connected
37	USB0-	USB0 data –	38	CLK_33MHz	33 MHz clock out
39	GND	Ground	40	GND	Ground
41	A_PETp0	Link A, lane 0 transmit +	42	A_PERp0	Link A, lane 0 receive +
43	A_PETn0	Link A, lane 0 transmit –	44	A_PERn0	Link A, lane 0 receive –
45	GND	Ground	46	APRSNT#/GND	Link A card present
47	PERST#	Reset	48	A_CLKp	Link A clock +
49	WAKE#	Wake on event signal	50	A_CLKn	Link A clock –
51	+5V	+5V power	52	GND	Ground

Table 6: SUMIT B Top Connector Pinout

J10 Pin	Signal Name	Function
1	GND	Ground
3	B_PETp0	Link B, lane 0 transmit +
5	B_PETn0	Link B, lane 0 transmit –
7	GND	Ground
9	C_CLKp	Link C clock +
11	C_CLKn	Link C clock –
13	CPRSNT#/GND	Link C present
15	C_PETp0	PCIe link C, lane 0 transmit +
17	C_PETn0	PCIe link C, lane 0 transmit –
19	GND	Ground
21	C_PETp1	PCIe link C, lane 1 transmit +
23	C_PETn1	PCIe link C, lane 1 transmit –
25	GND	Ground
27	NC	Not connected
29	NC	Not connected
31	GND	Ground
33	NC	Not connected
35	NC	Not connected
37	GND	Ground
39	PERST#	Reset
41	NC	Not connected
43	+5V	+5V power
45	+5V	+5V power
47	+5V	+5V power
49	+5V	+5V power
51	+5V	+5V power

J10 Pin	Signal Name	Function
2	GND	Ground
4	B_PERp0	Link B, lane 0 receive +
6	B_PERn0	Link B, lane 0 receive –
8	BPRSNT#/GND	Link B present
10	B_CLKp	Link B clock +
12	B_CLKn	Link B clock –
14	GND	Ground
16	C_PERp0	PCIe link C, lane 0 receive +
18	C_PERn0	PCIe link C, lane 0 receive –
20	GND	Ground
22	C_PRTp1	PCIe link C, lane 1 transmit +
24	C_PERn1	PCIe link C, lane 1 transmit –
26	GND	Ground
28	NC	Not connected
30	NC	Not connected
32	GND	Ground
34	NC	Not connected
36	NC	Not connected
38	GND	Ground
40	NC	Not connected
42	NC	Not connected
44	NC	Not connected
46	3.3V	+3.3V power
48	3.3V	+3.3V power
50	3.3V	+3.3V power
52	+5VSB	+5V power

Video Interfaces

Standard video outputs on the Copperhead include LVDS for flat panel displays, dual DisplayPort™ outputs, and an analog VGA output. All outputs support multiple display modes including Extended Desktop and Clone. The integrated Intel HD4000 Graphics Processing Unit (GPU) provides hardware-accelerated MPEG-4/H.264 and MPEG-2 video encoding and decoding. The GPU supports graphics Turbo Boost and up to three simultaneous displays.

The VL- EBX-41 can also be operated without video attached. See “Console Redirection.”

VGA Connector

An adapter cable, part number VL-CBR-1201, is available to translate VGA connector J1 into a standard 15-pin D-Sub SVGA connector. The VGA port supports resolutions up to 2048x1536 at 75Hz. This connector is protected against ESD damage.

When the Copperhead is booted, the BIOS tests for a video monitor attached to the VGA port. If a monitor is not detected during this test, the VGA signals are disabled.

Table 7: VGA Video Output Pinout

J1 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	RED	Red Video	1
3	GND	Ground	7
4	GREEN	Green Video	2
5	GND	Ground	8
6	BLUE	Blue Video	3
7	GND	Ground	5
8	HSYNC	Horizontal Sync	13
9	GND	Ground	10
10	VSYNC	Vertical Sync	14
11	SCL	DDC Serial Data Line Clock	11
12	SDA	DDC Serial Data Line	12

LVDS Flat Panel Display

The integrated LVDS Flat Panel Display in the Copperhead is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 4 bits of timing control (HSYNC/VSYNC/DE) on the 4 differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 112 MHz.

CMOS Setup provides several options for standard LVDS flat panel types. If these options do not match the requirements of the panel you are attempting to use, contact Support@VersaLogic.com for a custom video BIOS.

Table 8: LVDS Flat Panel Display Pinout

J32 Pin	Signal Name	Function
1	GND	Ground
2	NC	Not Connected
3	LVDSA3	Diff. Data 3 (+)
4	LVDSA3#	Diff. Data 3 (-)
5	GND	Ground
6	LVDSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (-)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (-)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (-)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (-)
17	GND	Ground
18	GND	Ground
19	+3.3V	+3.3V (Protected)
20	+3.3V	+3.3V (Protected)

The +3.3V power provided to pins 19 and 20 of J32 is protected by a software-controllable power switch (1 Amp max.). This switch is controlled by the L_VDD_EN signal from the LVDS interface controller in the Intel® 7 Series Platform Controller Hub (PCH). See the Intel GM45 Datasheet for detailed information.

MINI DISPLAYPORT

Two DisplayPorts are provided using two 20-pin mini DisplayPort connectors at locations J26 and J27. DisplayPort consists of three interfaces; main Link, Auxiliary channel, and Hot Plug Detect. The main Link transfers high speed isochronous video and audio data. The Auxiliary channel is used for link management and device control. The EDID is read over this interface. The Hot Plug Detect signal alerts the PCH when a device is connected.

Table 9: mini DisplayPort Connector Pinout

J26, J27 Pin	Signal Name	J26, J27 Pin	Signal Name
1	GND	2	HOT PLUG DETECT
3	ML_LANE0_P	4	CONFIG 1
5	ML_LANE0_N	6	CONFIG 2
7	GND	8	GND
9	ML_LANE1_P	10	ML_LANE3_P
11	ML_LANE1_N	12	ML_LANE3_N
13	GND	14	GND
15	ML_LANE2_P	16	AUX_CH_P
17	ML_LANE2_N	18	AUX_CH_N
19	RTN	20	DP_POWER

CONSOLE REDIRECTION

The Copperhead can be operated without using the on-board video output by redirecting the console to a serial communications port. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

Console redirection settings are configured on the Serial Port Console Redirection submenu of the Advanced tab. It is disabled by default. When enabled, the console will be available both at the serial port and using the standard keyboard/video console. The video console may resize and slow down to accommodate the slower serial console connection. By default, the serial console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control.

Null Modem

The following figure illustrates a typical DB9 to DB9 RS-232 null modem adapter.

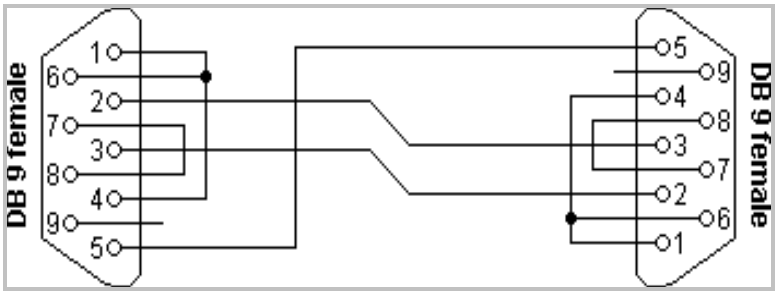

Figure 13. Null Modem with Loop-back Handshaking

Pins 1, 4, and 6 are shorted together on each connector.

SATA Ports

The Copperhead provides two 6 GB/s SATA ports (J3 and J7) and two 3 GB/s ports (J5 and J9). All SATA connectors are standard 7-pin straight SATA friction latching connectors. The housing for the 6GB/s connectors is blue in color, and for the 3GB/s connectors it is the standard black.

Power to SATA drives is supplied by the ATX power supply. Note that the standard SATA drive power connector is different than the common 4-pin Molex connector used on IDE drives. Most current ATX power supplies provide SATA connectors, and many SATA drives provide both types of power connectors. If the power supply you are using does not provide SATA connectors, adapters are available.

Table 10: SATA Port Pinout

SATA Pin	Signal Name	Function
1	GND	Ground
2	TX+	Transmit +
3	TX-	Transmit -
4	GND	Ground
5	RX-	Receive -
6	RX+	Receive +
7	GND	Ground

mSATA

The Copperhead provides one mSATA only slot at connector J11.

J11 Pin	Signal Name	Function
1	Reserved	Not connected
2	+3.3V	3.3V source
3	Reserved	Not connected
4	GND	Ground
5	Reserved	Not connected
6	+1.5V	1.5V power
7	Reserved	Not connected
8	Reserved	Not connected
9	GND	Ground
10	Reserved	Not connected
11	Reserved	Not connected
12	Reserved	Not connected
13	Reserved	Not connected
14	Reserved	Not connected
15	GND	Ground
16	Reserved	Not connected
17	Reserved	Not connected
18	GND	Ground
19	Reserved	Not connected
20	Reserved	Not connected

J11 Pin	Signal Name	Function
21	GND	Ground
22	Reserved	Not connected
23	+B	Host receiver diff. pair +
24	+3.3V	3.3V source
25	-B	Host receiver diff. pair –
26	GND	Ground
27	GND	Ground
28	+1.5V	1.5V power
29	GND	Ground
30	Two Wire I/F	Two wire I/F clock
31	-A	Host transmitter diff. pair –
32	Two Wire I/F	Two wire I/F data
33	+A	Host transmitter diff. pair +
34	GND	Ground
35	GND	Ground
36	Reserved	Not connected
37	GND	Ground
38	Reserved	Not connected
39	+3.3V	3.3V source
40	GND	Ground
41	+3.3V	3.3V source
42	Reserved	Not connected
43	GND/NC	Ground/Not connected [3]
44	Reserved	Not connected
45	Vendor	Not connected
46	Reserved	Not connected
47	Vendor	Not connected
48	+1.5V	1.5V power
49	DA/DSS	Device activity [4]
50	GND	Ground
51	GND	Ground [5]
52	+3.3V	3.3V source

eUSB

The Copperhead includes a 2 mm eUSB port at connector J36 on the bottom of the board. (Note that connector J36 does not accept 2.54 mm modules.) The VersaLogic VL-F15 Series of eUSB SSD modules are available in sizes of 2 GB or 4 GB. Contact VersaLogic Sales to order. eUSB modules are secured to the on-board standoff using M2.5 x 6mm pan head Philips nylon screws. These screws are available in quantities of 10 in the VL-HDW-108 hardware kit from VersaLogic.

Table 11: eUSB Port Locations

J36 Pin	Signal Name	Function
1	+5V	+5V Power Supply
2	NC	Not connected
3	D-	Data –
4	NC	Not connected
5	D+	Data +
6	NC	Not connected
7	GND	Ground
8	NC	Not connected
9	Key	Physical key
10	LED	SSD LED

The blue LED at location D9 lights with activity on the eUSB port, if supported by the eUSB module.

Ethernet

The Copperhead features two on-board Intel 82574IT Gigabit Ethernet controllers. The controllers provide a standard IEEE 802.3 Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications. RJ45 connectors are located at locations J25 (Ethernet 0) and J24 (Ethernet 1). While these controllers are not NE2000-compatible, they are widely supported. Drivers are readily available to support a variety of operating systems. These interfaces are protected against ESD damage.

ETHERNET CONNECTORS

Two board-mounted RJ45 connectors are provided to make connection with Category 5 or 6 Ethernet cables. The 82574IT Ethernet controller auto-negotiates connection speed. These interfaces use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

The RJ45 connectors have two built-in LEDs to provide an indication of the Ethernet status as shown in the following table.

Table 12: RJ45 Connector Status LEDs

LED	State	Description
Green/Orange (Link Speed)	Orange	1 Gbps speed
	Green	100 Mbps speed
	Off	10 Mbps speed or cable not connected
Yellow (Activity)	On	Cable connected (intermittent with activity)
	Off	Cable not connected

STATUS LED

Connector J22 provides an additional on-board Ethernet status LED interface. The +3.3V power supplied to this connector is protected by a 1 Amp fuse.

Table 13: Ethernet Status LED Pinout

J22 Pin	Signal Name	Function
1	+3.3V	Protected Power Supply
2	YEL0	Yellow LED - Ethernet 0
3	ORN0	Orange LED - Ethernet 0
4	GRN0	Green LED - Ethernet 0
5	+3.3V	Protected Power Supply
6	YEL1	Yellow LED - Ethernet 1
7	ORN1	Orange LED - Ethernet 1
8	GRN1	Green LED - Ethernet 1
9	GND	Ground
10	W_DISABLE#	PCIe Mini Card Disable

W_Disable# Signal

The W_DISABLE# is for use with optional wireless PCIe Mini Cards. The signal allows you to disable a wireless card's radio operation in order to meet public safety regulations or when otherwise desired. The W_DISABLE# signal is an active low signal that when driven low (shorted to ground) disables radio operation on the PCIe Mini Card wireless device. When the W_DISABLE# is not asserted, or in a high impedance state, the radio may transmit if not disabled by other means such as software.

USB

The VL-EBX-41 includes ten USB 2.0 ports and two USB 3.0 ports. There are eight USB ports with standard USB Type A connectors, located on the baseboard and paddleboard. The eUSB, SUMIT, PCIe/104, and PCIe Mini Card/mSATA connectors all provide USB ports, as shown in the USB Port Map table below. These connectors are protected against ESD damage.

The USB interface on the Copperhead is UHCI (Universal Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible, which provides a common industry software/hardware interface.

Table 14: USB Port Map

USB Port	Device
0	On-board Type A Connector
1	On-board Type A Connector
2	On-board USB3 Type A Connector
3	On-board USB3 Type A Connector
4	CRB-5013 paddle board Type A Connector
5	CRB-5013 paddle board Type A Connector
6	CRB-5013 paddle board Type A Connector
7	CRB-5013 paddle board Type A Connector
8	SUMIT
9	SUMIT
10	SUMIT / PCIe/104
11	SUMIT / PCIe/104
12	eUSB Module
13	PCIe Mini Card / mSATA

Serial Ports

The Copperhead features four on-board 16550-based serial communications channels located at standard PC I/O addresses. All serial ports can be operated in RS-232 4-wire or RS-422 mode. IRQ lines are chosen in BIOS setup. Each COM port can be independently enabled, disabled, or assigned a different I/O base address in BIOS setup.

COM Port Configuration

Use the BIOS setup screens to select between RS-232 and RS-422 operating modes.

Jumper block V2 is used to configure serial ports for RS-422 operation. See “Jumper Summary” for details. The 120-ohm termination resistor should be enabled for RS-422 endpoint stations. It should be disabled for RS-232 intermediate stations.

SERIAL PORT CONNECTORS

The pinouts of the DB9M connectors apply to the serial connectors on the VersaLogic breakout board VL-CBR-5013.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 15: COM0-1 Pinout – VL-CBR-5013 Connector J2

COM0	COM1		
Top DB9 J2 Pin	Bottom DB9 J2 Pin	RS-232	RS-422
1	1	—	—
2	2	RXD*	RxD-
3	3	TXD*	TxD-
4	4	—	—
5	5	Ground	Ground
6	6	—	—
7	7	RTS	TxD+
8	8	CTS	RxD+
9	9	—	—

Table 16: COM2-3 Pinout – VL-CBR-5013 Connectors J5-6

COM2	COM3		
J5 Pin	J6 Pin	RS-232	RS-422
1	1	Ground	Ground
2	2	RXD	RxD-
3	3	CTS	RxD+
4	4	TXD	TxD-
5	5	RTS	TxD+

Analog Input

The Copperhead uses two multi-range, 12-bit Linear Technology LTC1857 A/D converters, each with eight single-ended input signals (even and odd analog channels, for example inputs 1 and 2, can also be combined as differential inputs). The converter has a 100 kilo-sample-per-second (Ksps) sampling rate, with a 4 µs acquisition time, with per-channel input ranges of 0 to +5V, ±5V, 0 to +10V and ±10V.

The Copperhead A/D converter is controlled using the SPI registers. The A/D converter for channels 1-8 is accessed by setting SPI slave select 5 (writing 5h to the SS field in SPICONTROL). The A/D converter for channels 9-16 is accessed by first setting the ADIOMODE control bit to a '1' in the Miscellaneous Control Register MISCCON and then setting SPI slave select 3 (writing 3h to the SS field in SPICONTROL). The A/D converter for channels 1-8 can be accessed for either setting of ADIOMODE.

See "SPI Registers" for a complete description of the registers.

See the Linear Technology LTC1857 A/D Converter Datasheet for programming information.

Warning! Application of analog voltages greater than +25V or less than -25V can damage the converter.

External Connections

Single-ended analog voltages are applied to connector J19 as shown in the following table. Standard VL-EBX-41 models include eight analog input channels.

Table 17: Analog Input Pinout

J19 Pin	Signal	VL-CBR-4004 Connector	VL-CBR-4004 Pin (Silkscreen)
1	Analog Input 1	**J1 Analog Input**	5 (IO1)
2	Analog Input 2		4 (IO2)
3	Analog Input 3		3 (IO3)
4	Analog Input 4		2 (IO4)
5	Ground		1 (GND1)
6	Analog Input 5	**J2 Analog Input**	5 (IO5)
7	Analog Input 6		4 (IO6)
8	Analog Input 7		3 (IO7)
9	Analog Input 8		2 (IO8)
10	Ground		1 (GND1)
11	Analog Input 9	**J3 Analog Input (Custom*)**	5 (IO9)
12	Analog Input 10		4 (IO10)
13	Analog Input 11		3 (IO11)
14	Analog Input 12		2 (IO12)
15	Ground		1 (GND2)
16	Analog Input 13	**J4 Analog Input (Custom*)**	5 (IO13)
17	Analog Input 14		4 (IO14)
18	Analog Input 15		3 (IO15)
19	Analog Input 16		2 (IO16)
20	Ground		1 (GND2)

* Contact Sales@VersaLogic.com for information on custom orders.

ANALOG INPUT USING THE SPI INTERFACE

See "SPI Registers" for a description of the SPI interface and registers.

Initiating an Analog Conversion Using the SPI Interface

The following procedure can be used to initiate an analog conversion using the SPI interface

1. Set ADIOMODE = 1 for the A/D converter for channels 9-16. The A/D converter for channels 1-8 can be accessed for either setting of ADIOMODE.
2. For the A/D converter for channels 1-8 write 15h to the SPICONTROL register (I/O address CA8h) or write 13h for the A/D converter for channels 9-16. This value configures the SPI port to select the on-board A/D converter, 16-bit frame length, low SCLK idle state, rising edge SCLK edge, and automatic slave select.
3. Write 10h to the SPISTATUS register (I/O address CA9h) – This value selects 2 MHz SCLK speed, hardware IRQ disable, and left-shift data. A 2 MHz clock is used to avoid having to insert a delay after the SPI cycle to wait for the end of the 4 µs A/D signal acquisition interval. If a 4 MHz SPI clock is used then there must be a delay of 1.5 µs after the SPI cycle ends before starting an A/D conversion; if an 8 MHz SPI clock is used then there must be a delay of 2.75 µs after the end of the SPI cycle.
4. Write any value to SPIDATA2 (I/O address CACh) – This data will be ignored by the A/D converter.
5. Write bit 0 of the analog input channel number to Bit 6, bits 2-1 of the analog input channel number to bits 5-4, and a 2-bit input range code to bits 3-2 of SPIDATA3 (I/O address CADh) – Any write operation to this register triggers an SPI transaction. The 2-bit input-range codes are 0 (±5V), 1 (±10V), 2 (0 to +5V) or 3 (0 to +10V). Bit 7 must be set to a '1' for a single-ended channel (fyi - each A/D can be configured for either 8 single-ended inputs or 4 differential inputs). For example, if converting the 4th A/D channel (channel number 3) with a 0 to +5V range then SPIDATA3 is set to D8h
6. Poll the SPI BUSY bit in the SPISTATUS register until the conversion is completed.
7. For the A/D converter for channels 1-8 write a '1' to ADCONVST0 Bit 0 of the FPGA ADC, DAC control/status register (I/O address CAFh) to start a conversion. For the A/D converter for channels 9-16 write a '1' to the ADCONVST1 bit 1.For the A/D converter for channels 1-8 poll the ADCBUSY0 Bit 2 of the FPGA ADC/DAC control/status register (I/O address CAFh) until this bit is a '0' (not busy) to indicate a conversion is completed (a conversion takes a maximum of 5 µs). For the A/D converter for channels 9-16 poll the ADCBUSY1 Bit 3.Read the conversion data from SPIDATA2 (upper 8 bits of the 12-bit conversion) and SPIDATA3 (lower 4 bits of the 12-bit conversion are in the upper 4 bits of this byte). The data read is from the previous conversion not the one for the SPI values written in Steps 1–5. Another conversion cycle is required to retrieve that data. Typically a number of channels are sampled at one time so this conversion delay is not significant.

Anytime an SPI command is written to the A/D device a conversion must be issued for that command. Another command will not be accepted until a conversion is performed.

Analog Output

The Copperhead uses two 12-bit Linear Technology LTC2634 D/A converters, each with four (4) single-ended output signals. The converter has 5 µs per-channel update rate with a 0 to 4.096V output voltage range.

The Copperhead D/A converter is controlled using the SPI registers. The D/A converter for channels 1-4 is accessed by setting SPI slave select 7 (writing 7h to the SS field in SPICONTROL). The D/A converter for channels 5-8 is accessed by first setting the ADIOMODE control bit to a '1' in the Miscellaneous Control Register MISCCON and then setting SPI slave select 4 (writing 4h to the SS field in SPICONTROL). The D/A converter for channels 1-4 can be accessed for either setting of ADIOMODE. See "SPI Registers" for a description of the SPI interface and registers.

See the Linear Technology LTC2634 D/A Converter Datasheet for programming information.

Table 18: Analog Output Pinout

J19 Pin	Signal	VL-CBR-4004 Connector	VL-CBR-4004 Pin (Silkscreen)
21	Analog Output 1	**J6 Analog Output**	1 (IO17)
22	Analog Output 2		2 (IO18)
23	Analog Output 3		3 (IO19)
24	Analog Output 4		4 (IO20)
25	Ground		5 (GND3/PBRST#)
26	Analog Output 5	**J7 Analog Output (Custom*)**	1 (IO21)
27	Analog Output 6		2 (IO22)
28	Analog Output 7		3 (IO23)
29	Analog Output 8		4 (IO24)
30	Ground		5 (GND3)

* Contact Sales@VersaLogic.com for information on custom orders.

Analog Output Using the SPI Interface

The following procedure can be used to set an analog output using the SPI interface.

1. Set ADIOMODE = 1 for the D/A converter for channels 5-8. The D/A converter for channels 1-4 can be accessed for either setting of ADIOMODE.
2. For the D/A converter for channels 1-4 write 27h to the SPICONTROL register (I/O address CA8h) or write 24h for the D/A converter for channels 5-8 – This value configures the SPI port to select the D/A converter, 24-bit frame length, low SCLK idle state, rising edge SCLK edge, and automatic slave select.
3. Write 30h to the SPISTATUS register (I/O address CA9h) – This value selects 8 MHz SCLK speed, hardware IRQ disable, and left-shift data.
4. Write the LS 4-bits of the 12-bit output value into the MS 4-bits of SPIDATA1 (I/O address CABh). For example, if writing a 12-bit value of 123h the value of 30h is written to SPIDATA1.
5. Write the MS 8-bits of the 12-bit output value to SPIDATA2 (I/O address CACh). For example, if writing a 12-bit value of 123h the value of 12h is written to SPIDATA2.

6. Write the analog output channel number (0 to 3) to Bits 3-0 and the write-and-update-channel command 3h to Bits 7-4 of SPIDATA3 (I/O address CADh) – Any write operation to this register triggers an SPI transaction. For example, if writing to the third DAC channel (channel number 2) the value written to SPIDATA3 is 32h.
7. Poll the SPI BUSY bit in the SPISTATUS register until the conversion is completed.
8. The D/A output will be stable in no more than 5 µs.

Digital I/O

The 40-pin I/O connector (J21) incorporates 32 digital I/O lines. Table 19 shows the function of each pin. The digital I/O lines are controlled using the SPI registers. See "SPI Registers" for a complete description of the registers.

The digital lines are grouped into two banks of 16-bit bi-directional ports. The direction of each 8-bit port is controlled by software. The digital I/O lines power up in the input mode. The 24 mA source/sink drive and short protected outputs are an excellent choice for industrial LVTTL interfacing. All I/O pins use +3.3V signaling.

Warning! Damage may occur if the I/O pins are connected to +5V logic.

Table 19: J21 I/O Connector Pinout

J21 Pin	Signal	VL-CBR-4004 Connector	VL-CBR-4004 Pin (Silkscreen)
1	Digital I/O 1	**J1**	5 (IO1)
2	Digital I/O 2		4 (IO2)
3	Digital I/O 3		3 (IO3)
4	Digital I/O 4		2 (IO4)
5	Ground		1 (GND1)
6	Digital I/O 5	**J2**	5 (IO5)
7	Digital I/O 6		4 (IO6)
8	Digital I/O 7		3 (IO7)
9	Digital I/O 8		2 (IO8)
10	Ground		1 (GND1)
11	Digital I/O 9	**J3**	5 (IO9)
12	Digital I/O 10		4 (IO10)
13	Digital I/O 11		3 (IO11)
14	Digital I/O 12		2 (IO12)
15	Ground		1 (GND2)
16	Digital I/O 13	**J4**	5 (IO13)
17	Digital I/O 14		4 (IO14)
18	Digital I/O 15		3 (IO15)
19	Digital I/O 16		2 (IO16)
20	Ground		1 (GND2)
21	Digital I/O 17	**J6**	1 (IO17)
22	Digital I/O 18		2 (IO18)
23	Digital I/O 19		3 (IO19)
24	Digital I/O 20		4 (IO20)
25	Ground		5 (GND3/PBRST#)
26	Digital I/O 21	**J7**	1 (IO21)
27	Digital I/O 22		2 (IO22)
28	Digital I/O 23		3 (IO23)
29	Digital I/O 24		4 (IO24)
30	Ground		5 (GND3)
31	Digital I/O 25	**J8**	1 (IO25)
32	Digital I/O 26		2 (IO26)
33	Digital I/O 27		3 (IO27)
34	Digital I/O 28		4 (I028)
35	Ground		5 (GND4)
36	Digital I/O 29	**J9**	1 (IO29)
37	Digital I/O 30		2 (IO30)
38	Digital I/O 31		3 (IO31)
39	Digital I/O 32		4 (IO32)
40	Ground		5 (GND4)

DIGITAL I/O PORT CONFIGURATION USING THE SPI INTERFACE

Digital I/O channels 0-31 are accessed via SPI slave select 6 (writing 6h to the SS field in SPICONTROL). Each pair of I/O ports is configured by a set of paged I/O registers accessible through SPI. These registers control settings such as signal direction, input polarity, and interrupt source.

Digital I/O Initialization Using the SPI Interface

There are two Microchip MCP23S17 digital I/O devices used. Digital I/O channels 0-15 map to device #0 (address "000") and channels 15-31 to device #1 (address "001"). Please refer to the Microchip MCP23S17 datasheet for more information about the MCP23S17. Before accessing the digital I/O devices a '1' must be written to the control bit HAEN in the IOCON register (write a 8h to this register) in the MCP23S17 devices. This write is done to device address "000" which will actually write this HAEN bit to both devices. Once this HAEN bit is set then both devices can be independently accessed. This must be done anytime these parts are reset. Example code is shown below (this assumes the FPGA base address is the default setting CA0h).

```
      MOV   DX, CA8h
      MOV   AL, 26h     ;SPICONTROL: SPI Mode 00, 24bit, auto, SPI 6
      OUT   DX, AL
      MOV   DX, CA9h
      MOV   AL, 30h     ;SPISTATUS: 8MHz, no IRQ, left-shift
      OUT   DX, AL
      MOV   DX, CABh
      MOV   AL, 08h     ;SPIDATA1: Set HAEN Bit to a '1'
      OUT   DX, AL
      MOV   DX, CACh
      MOV   AL, 0Ah     ;SPIDATA2: MCP23S17 IOCON addr 0x0A
      OUT   DX, AL
      MOV   DX, CADh
      MOV   AL, 40h     ;SPIDATA3: MCP23S17 write to device "000"
      OUT   DX, AL

BUSY: MOV   DX, CA9h
      IN    AL, DX      ;Get SPI status
      AND   AL, 01h     ;Isolate the BUSY bit
      JNZ   BUSY        ;Loop back if SPI transaction is not complete
```

Digital I/O Interrupt Generation Using the SPI Interface

Digital I/O can be configured to issue hardware interrupts on the transition (high to low or low to high) of any digital I/O pin. IRQ assignment is made in SPI control register SPISTATUS. This IRQ is shared among all SPI devices connected to the VL-EBX-41 (the ADC and DAC devices on the SPI interface do not have interrupts). Digital I/O chip interrupt configuration is achieved through I/O port register settings. Please refer to the Microchip MCP23S17 datasheet for more information.

The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts. The following code example illustrates how to do this for device #0 on channels 0-15. Normally, the BIOS initializes the on-board digital I/O chips at boot time.

```
      MOV   DX, CA8h
      MOV   AL, 26h     ;SPICONTROL: SPI Mode 00, 24bit, auto SPI 6
      OUT   DX, AL
```

```
        MOV   DX, CA9h
        MOV   AL, 30h      ;SPISTATUS: 8MHz, no IRQ, left-shift
        OUT   DX, AL
        MOV   DX, CABh
        MOV   AL, 44h      ;SPIDATA1: Mirror & Open-Drain interrupts
        OUT   DX, AL
        MOV   DX, CACh
        MOV   AL, 0Ah      ;SPIDATA2: MCP23S17 address 0x0A
        OUT   DX, AL
        MOV   DX, CADh
        MOV   AL, 40h      ;SPIDATA3: MCP23S17 write command
        OUT   DX, AL

BUSY:   MOV   DX, CA9h
        IN    AL, DX       ;Get SPI status
        AND   AL, 01h      ;Isolate the BUSY bit
        JNZ   BUSY         ;Loop back if SPI transaction is not complete

        MOV   DX, CA8h
        MOV   AL, 27h      ;SPICONTROL: SPI Mode 00, 24bit, auto SPI 6
        OUT   DX, AL
        MOV   DX, CA9h
        MOV   AL, 30h      ;SPISTATUS: 8MHz, no IRQ, left-shift
        OUT   DX, AL
        MOV   DX, CABh
        MOV   AL, 44h      ;SPIDATA1: Mirror & Open-Drain interrupts
        OUT   DX, AL
        MOV   DX, CACh
        MOV   AL, 0Ah      ;SPIDATA2: MCP23S17 address 0x0A
        OUT   DX, AL
        MOV   DX, CADh
        MOV   AL, 40h      ;SPIDATA3: MCP23S17 write command
        OUT   DX, AL
```

Writing to a Digital I/O Port Using the SPI Interface

The following code example initiates a write of 55h to Digital I/O port bits DIO15-DIO8.

```
;Write 44h to configure MCP23S17 register IOCON

   MOV    DX, CA8h
   MOV    AL, 26h       ;SPICONTROL: SPI Mode 00, 24bit, SPI 6
   OUT    DX, AL
   MOV    DX, CA9h
   MOV    AL, 30h       ;SPISTATUS: 8MHz, no IRQ, left-shift
   OUT    DX, AL
   MOV    DX, CABh
   MOV    AL, 44h       ;SPIDATA1: mirror and open-drain interrupts
   OUT    DX, AL
   MOV    DX, CACh
   MOV    AL, 0Ah       ;SPIDATA2: MCP23S17 IOCON register address 0Ah
   OUT    DX, AL
   MOV    DX, CADh
   MOV    AL, 40h       ;SPIDATA3: MCP23S17 write command
   OUT    DX, AL
   CALL   BUSY          ;Poll busy flag to wait for SPI transaction

;Configure MCP23S17 register IODIRA for outputs

   MOV    DX, CABh
```

```
        MOV    AL, 00h       ;SPIDATA1: 00h for outputs
        OUT    DX, AL
        MOV    DX, CACh
        MOV    AL, 00h       ;SPIDATA2: MCP23S17 register address 00h
        OUT    DX, AL
        MOV    DX, CADh
        MOV    AL, 40h       ;SPIDATA3: MCP23S17 write command
        OUT    DX, AL
        CALL   BUSY          ;Poll busy flag to wait for SPI transaction

    ;Write 55h to MCP23S17 register GPIOA

        MOV    DX, CABh
        MOV    AL, 55h       ;SPIDATA1: data to write
        OUT    DX, AL
        MOV    DX, CACh
        MOV    AL, 14h       ;SPIDATA2: MCP23S17 register address 14h
        OUT    DX, AL
        MOV    DX, CADh
        MOV    AL, 40h       ;SPIDATA3: MCP23S17 write command
        OUT    DX, AL
        CALL   BUSY          ;Poll busy flag to wait for SPI transaction

BUSY:   MOV    DX, CA9h
        IN     AL, DX        ;Get SPISTATUS
        AND    AL, 01h       ;Isolate the BUSY flag
        JNZ    BUSY          ;Loop if SPI transaction not complete
```

Reading a Digital I/O Port Using the SPI Interface

The following code example reads the DIO15-DIO8 input lines.

```
'REGISTER ASSIGNMENT
'---------------------
CONST SPICONTROL1 = &HCA8
CONST SPICONTROL2 = &HCA9
CONST SPISTATUS = &HCA9
CONST SPIDATA1 = &HCAB
CONST SPIDATA2 = &HCAC
CONST SPIDATA3 = &HCAD

'INITIALIZE SPI CONTROLLER
'================================

'SPICONTROL1 Register
'---------------------------
'D7 CPOL      = 0 SPI Clock Polarity (SCLK idles low)
'D6 CPHA      = 0 SPI Clock Phase (Data read on rising edge)
'D5 SPILEN1   = 1 SPI Frame Length (24-Bit)
'D4 SPILEN0   = 0  "    "     "      "
'D3 MAN_SS    = 0 SPI Slave Select Mode (Automatic)
'D2 SS2       = 1 SPI Slave Select (On-Board DIO 0-15)
'D1 SS1       = 1  "    "     "          "     "
'D0 SS0       = 0  "    "     "          "     "
OUT SPICONTROL1, &H26

'SPICONTROL2 Register
'---------------------------
'D7 IRQSEL1   = 0 IRQ Select (IRQ3)
'D6 IRQSEL0   = 0  "    "      "
'D5 SPICLK1   = 1 SPI SCLK Frequency (8.333 MHz)
'D4 SPICLK0   = 1  "    "      "          "
'D3 HW_IRQ_EN = 0 Hardware IRQ Enable (Disabled)
```

```
'D2 LSBIT_1ST = 0 SPI Shift Direction (Left Shifted)
'D1 0         = 0 This bit has no function
'D0 0         = 0 This bit has no function
OUT SPICONTROL2, &H30


'INITIALIZE MCP23S17
'===================

'MCP23S17 IOCON Register
'-----------------------
'D7 BANK      = 0 Registers in same bank (addresses are sequential)
'D6 MIRROR    = 1 The INT pins are internally connected
'D5 SEQOP     = 0 Sequential op disabled. Addr ptr does not increment.
'D4 DISSLW    = 0 Slew rate control for SDA output (enabled)
'D3 HAEN      = 0 Hardware address enable (addr pins disabled)
'D2 ODR       = 1 INT pin is open-drain
'D1 INTPOL    = 0 Polarity of INT output pin (ignored when ODR=1)
'D0 0         = 0 This bit has no function
OUT SPIDATA1, &H44

'MCP23S17 IOCON Register Address
'-------------------------------
OUT SPIDATA2, &HA

'MCP23S17 SPI Control Byte (Write)
'---------------------------------
'D7 SLAVEFA3  = 0 Slave Address (Fixed Portion)
'D6 SLAVEFA2  = 1   "      "       "     "
'D5 SLAVEFA1  = 0   "      "       "     "
'D4 SLAVEFA0  = 0   "      "       "     "
'D3 SLAVEHA2  = 0 Slave Address Bits (Hardware Address Bits)
'D2 SLAVEHA1  = 0   "      "       "     "
'D1 SLAVEHA0  = 0   "      "       "     "
'D0 READWRITE = 0 Read/Write Bit = Write
OUT SPIDATA3, &H40

WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

'INITIALIZE DIRECTION OF DIO LINES D15-D8 AS INPUTS
'=================================================

'Direction = All Inputs
OUT SPIDATA1, &HFF

'MCP23S17 IODIRA Register Address
OUT SPIDATA2, &H0

'MCP23S17 SPI Control Byte (Write)
OUT SPIDATA3, &H40

WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

'Repeat until ESC key is pressed
WHILE INKEY$ <> CHR$(27)


  'READ DIO INPUT DATA FROM MCP23S17
  '---------------------------------

  'MCP23S17 GPIOA Register Address
  OUT SPIDATA2, &H12

  'MCP23S17 SPI Control Byte (Read)
  OUT SPIDATA3, &H41
```

```
  WHILE (INP(SPISTATUS) AND &H1) = &H1: WEND

  'DIO Input Data
  PRINT HEX$(INP(SPIDATA1))

WEND

SYSTEM
```

Audio

The audio interface on the Copperhead is implemented using an Integrated Device Technology, Inc. 92HD87 Audio Codec. This interface is Intel High Definition Audio compatible. Drivers are available for most Windows-based and Linux operating systems. To obtain the most current versions, consult the Copperhead product support page**.**

The J29 main I/O connector provides the line-level stereo input and line-level stereo output connection points. The outputs will drive most amplified PC speaker sets.

The following table shows the pinout of the audio connector J3 on the VL-CBR-5013 breakout board.

Table 20: VL-CBR-5013 J3 Audio Connector Pinout

J3 Pin	Signal Name	Function
1	LINE_INL	Line-In Left
2	LINE_INR	Line-In Right
3	HDA_GND	HDA Ground
4	LINE_OUTL	Line-Out Left
5	LINE_OUTR	Line-Out Right
6	HDA_GND	HDA Ground

Note: In Windows, the rear line-in audio input is configured by default as a microphone input. To configure it for audio input, disable the microphone boost to eliminate audio distortion.

Counter/Timers

The Copperhead includes three uncommitted 8254 type counter/timer channels for general program use. External control signals for the three channels are available on connector J19.

Table 21: J22 Counter Timer Pinout

J19 Pin	Signal Direction*	Signal Name	Function
31	Output	OCTC3	Timer 3 Counter Output
32	Input	GCTC3	Timer 3 Gate Input
33	Input	ICTC3	Timer 3 Clock Input
34	Output	OCTC4	Timer 4 Counter Output
36	Input	GCTC4	Timer 4 Gate Input
37	Input	ICTC4	Timer 4 Clock Input
38	Output	OCTC5	Timer 5 Counter Output
39	Input	GCTC5	Timer 5 Gate Input

VL-CBR-4004 Connector	VL-CBR-4004 Pin (Silkscreen)
J8	1 (IO25)
	2 (IO26)
	3 (IO27)
	4 (I028)
J9	1 (IO29)
	2 (IO30)
	3 (IO31)
	4 (IO32)

* Relative to Copperhead

The Custom Programming appendix discusses how to use and configure these timers using the following registers.

Register	Read/Write	Address	Name
IRQCTRL	R/W	CA3h	Interrupt Control Register
IRQSTAT	R-Status/Write-Clear	CA4h	Interrupt Status Register
TMCNTRL	R/W	CA5h	Timer Control Register
TIMBASEMS	R/W	CA6h	Timer Base MS Address Register
TIMBASELS	R/W	CA7h	Timer Base LS Address Register

PCIe Mini Card / mSATA

The socket at location J8 accepts a full-height PCI Express Mini Card or an mSATA module.

The PCIe Mini Card interface includes one PCIe x1 lane, one USB 2.0 channel, and the SMBus interface. The socket is compatible with plug-in Wi-Fi modems, GPS receivers, flash data storage, and other cards for added flexibility. An Intel WiFi Link 5300 PCI Express Mini Card (VL-WD10-CBN) is available from VersaLogic. A WiFi antenna (VL-CBR-ANT01) and a 12" WiFi card to bulkhead RP-SMA transition cable (VL-CBR-0201) are also available. For more information, contact Sales@VersaLogic.com.

The VL-MPEs-F1E series of mSATA modules provide flash storage of 4 GB, 16 GB, or 32 GB.

To secure a Mini Card or mSATA module to the on-board standoffs, use two M2.5 x 6mm pan head Philips nylon screws. These screws are available in quantities of 10 in the VL-HDW-108 hardware kit from VersaLogic.

Table 22: PCIe Mini Card / mSATA Pinout

J8 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
1	WAKE#	Wake	Reserved	Not connected
2	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
3	NC	Not connected	Reserved	Not connected
4	GND	Ground	GND	Ground
5	NC	Not connected	Reserved	Not connected
6	1.5V	1.5V power	+1.5V	1.5V power
7	CLKREQ#	Reference clock request	Reserved	Not connected
8	NC	Not connected	Reserved	Not connected
9	GND	Ground	GND	Ground
10	NC	Not connected	Reserved	Not connected
11	REFCLK-	Reference clock input –	Reserved	Not connected
12	NC	Not connected	Reserved	Not connected
13	REFCLK+	Reference clock input +	Reserved	Not connected
14	NC	Not connected	Reserved	Not connected
15	GND	Ground	GND	Ground
16	NC	Not connected	Reserved	Not connected
17	NC	Not connected	Reserved	Not connected
18	GND	Ground	GND	Ground
19	NC	Not connected	Reserved	Not connected
20	W_DISABLE#	Wireless disable [1]	Reserved	Not connected
21	GND	Ground	GND	Ground
22	PERST#	Card reset	Reserved	Not connected
23	PERn0	PCIe receive –	+B	Host receiver diff. pair +
24	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
25	PERp0	PCIe receive +	-B	Host receiver diff. pair –
26	GND	Ground	GND	Ground
27	GND	Ground	GND	Ground
28	1.5V	1.5V power	+1.5V	1.5V power
29	GND	Ground	GND	Ground
30	SMB_CLK	SMBus clock	Two Wire I/F	Two wire I/F clock
31	PETn0	PCIe transmit –	-A	Host transmitter diff. pair –
32	SMB_DATA	SMBus data	Two Wire I/F	Two wire I/F data
33	PETp0	PCIe transmit +	+A	Host transmitter diff. pair +
34	GND	Ground	GND	Ground
35	GND	Ground	GND	Ground
36	USB_D-	USB data –	Reserved	Not connected
37	GND	Ground	GND	Ground
38	USB_D+	USB data +	Reserved	Not connected
39	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
40	GND	Ground	GND	Ground
41	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
42	LED_WWAN#	Wireless WAN LED	Reserved	Not connected
43	GND	mSATA Detect [2]	GND/NC	Ground/Not connected [3]
44	LED_WLAN#	Wireless LAN LED	Reserved	Not connected
45	NC	Not connected	Vendor	Not connected
46	LED_WPAN#	Wireless PAN LED	Reserved	Not connected

J8 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
47	NC	Not connected	Vendor	Not connected
48	1.5V	1.5V power	+1.5V	1.5V power
49	Reserved	Reserved	DA/DSS	Device activity [4]
50	GND	Ground	GND	Ground
51	Reserved	Reserved	GND	Ground [5]
52	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source

Notes:

1. This signal can be driven by GPIO24 from the ICH8M or as a custom option from Pin 10 on the Ethernet LED connector at location J28.
2. This pin is not grounded on the Copperhead since it can be used to detect the presence of an mSATA module versus a PCIe Mini Card. Grounding this pin is available as an option on custom boards.
3. This pin is not grounded on the Copperhead to make it available for mSATA module detection.
4. This signal drives the blue LED activity indicator at location D11 (upper right corner of the board as shown in Figure 6). This LED lights with mSATA disk activity, if supported by the mSATA module.
5. Some PCIe modules use this signal as a second Mini Card wireless disable input. On the Copperhead, this signal is available for use for mSATA versus PCIe Mini Card detection. There is an option on the VersaLogic Features BIOS setup screen for setting the mSATA detection method.

PCIe Mini Card Wireless Status LEDs

Three wireless status LEDs are provided on the Copperhead at locations D10 and D8:

- D10 Yellow – Wireless WAN
- D8 Green – Wireless LAN
- D8 Yellow – Wireless PAN

These LEDs light when the associated device is installed and capable of transmitting.

User I/O Connector

The 50-pin user I/O connector (J29) incorporates the COM ports, four USB ports, programmable LED, power LED, pushbutton reset, power button, audio line in/out, and speaker interfaces. The table below illustrates the function of each pin.

Table 23: User I/O Connector Pinout

J29 Pin	CBR-5013 Connector	Signal	
		RS-232	RS-422
1	**COM0**	Ground	Ground
2	**J2**	RXD	RxD-
3	Top DB9	CTS	RxD+
4		Ground	Ground
5		TXD	TxD-
6		RTS	TxD+
7	**COM1**	Ground	Ground
8	**J2**	RXD	RxD-
9	Bottom DB9	CTS	RxD+
10		Ground	Ground
11		TXD	TxD-
12		RTS	TxD+
13	**COM2**	Ground	Ground
14	**J5**	RXD	RxD-
15		CTS	RxD+
16		Ground	Ground
17		TXD	TxD-
18		RTS	TxD+
19	**COM3**	Ground	Ground
20	**J6**	RXD	RxD-
21		CTS	RxD+
22		Ground	Ground
23		TXD	TxD-
24		RTS	TxD+

J29 Pin	CBR-5013 Connector	Signal
25	**USB 4**	USB4-5 +5.0V
26		Data +
27		Data -
28	**USB 5**	USB4-5 +5.0V
29		Data +
30		Data -
31	**USB 6**	USB6-7 +5.0V
32		Data +
33		Data -
34	**USB 7**	USB6-7 +5.0V
35		Data +
36		Data -
37		+5.0V (Protected)
38	**D1**	Programmable LED
39	**SP1**	Speaker
40	**S2, J8 Pin 1**	Pushbutton Reset
41	**S1, J8 Pin 3**	Power Button
42		Ground
43	**Audio In**	Audio In Left
44	J3 Top	HDA ground (isolated)
45		Audio In Right
46		HDA ground (isolated)
47	**Audio Out**	Audio Out Left
48	J3 Bottom	HDA ground (isolated)
49		Audio Out Right
50		HDA ground (isolated)

LEDs

PROGRAMMABLE LED

Connector J29 includes an output signal for a programmable LED. Connect the cathode of the LED to J29 pin 38; connect the anode to +5V. A 332Ω on-board resistor limits the current to 15 mA. A programmable LED is provided on the VL-CBR-5013 breakout board. The programmable LED is the top LED at position D1.

To turn the LED on and off, set or clear bit D7 in I/O port CA0h. When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn the LED on and off.

LED On

```
MOV    DX,CA0H
IN     AL,DX
OR     AL,80H
OUT    DX,AL
```

LED Off

```
MOV    DX,CA0H
IN     AL,DX
AND    AL,7FH
OUT    DX,AL
```

POWER LED

The power LED on the VL-CBR-5013 indicates that the paddle board is being powered by the 5V supply (though it does not indicate that all S0 power supplies are good). The LED is lit only on when the board is in the S0 power state. If the board enters a Sleep or Hibernate mode, the LED will not be lit.

There is also an on-board green "Power-OK" LED (at location D10). This will illuminate when all power rails are good, and indicates that the board is in the S0 power state. If any power rail is not good, the LED will not illuminate. It also goes out when the board enters a sleep or hibernate power mode.

Pushbutton Reset

Connector J29 includes an input for a pushbutton reset switch. Shorting J29 pin 40 to ground causes the Copperhead to reboot.

The input can be connected to ground using the normally open contacts of a pushbutton switch or a relay, or with a switching transistor (open-collector or open-drain) capable of sinking 1 mA. The input must be driven to a voltage between 0V and 500mV to be recognized by the Copperhead. Do not add an external pull-up resistor to this signal.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the VL-CBR-5013 breakout board. Terminal block J8 on the breakout board also provides a reset signal on pin 1 and ground on pin 2.

Power Button

Connector J19 includes an input for a power button. Shorting J19 pin 41 to ground causes the board to enter an S5 power state (similar to the Windows Shutdown state). Shorting it again will return the board to the S0 power state and reboot the board. The button can be configured in Windows to enter an S3 power state (Sleep, Standby, or Suspend-to-RAM), an S4 power state (Hibernate or Suspend-to-Disk), or an S5 power state (Shutdown or Soft-Off).

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A power button is provided on the VL-CBR-5013 breakout board. Terminal block J8 also provides a power button signal on pin 3 and ground on pin 2.

In configurations where a power button is not connected to the board, if the system is put into an S5 state, power can be restored by turning off the power supply and turning it back on. This behavior is set by default by the BIOS. The behavior can be changed using the Restore AC Power Loss parameter on the Chipset > South Bridge menu of the BIOS setup screens.

SUPPORTED POWER STATES

The Copperhead supports the following power states:

- S0 (G0): Working.
- S1 (G1-S1): All processor caches are flushed, and the CPUs stop executing instructions. Power to the CPUs and RAM is maintained. Devices that do not indicate they must remain on may be powered down.
- S3 (G1-S3): Commonly referred to as Standby, Sleep, or Suspend-to-RAM. RAM remains powered.
- S4 (G1-S4): Hibernation or Suspend-to-Disk. All content of main memory is saved to non-volatile memory, such as a hard drive, and is powered down.
- S5 (G2): Soft Off. Almost the same as G3 Mechanical Off, except that the power supply still provides power, at a minimum, to the power button to allow return to S0. A full reboot is required. No previous content is retained. Other components may remain powered so the computer can "wake" on input from the keyboard, clock, modem, LAN, or USB device.
- G3: Mechanical off (ATX supply switch turned off).

Speaker

Connector J29 includes a speaker output signal at pin 39. The VL-CBR-5013 breakout board provides a Piezo electric speaker.

SPX Expansion Bus

Up to four serial peripheral expansion (SPX) devices can be attached to the Copperhead at connector J28 using the VL-CBR-1401 or VL-CBR-1402 cable. The SPX interface provides the standard serial peripheral interface (SPI) signals: SCLK, MISO, and MOSI, as well as four chip selects, SS0# to SS3#, and an interrupt input, SINT#.

The +5V power provided to pins 1 and 14 of J28 is protected by a 1 Amp resettable fuse.

Table 24: SPX Expansion Bus Pinout

J28 Pin	Signal Name	Function
1	V5_0	+5V (Protected)
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Serial Data In
5	GND	Ground
6	MOSI	Serial Data Out
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1
10	SS2#	Chip Select 2
11	SS3#	Chip Select 3
12	GND	Ground
13	SINT#	Interrupt Input
14	V5_0	+5V (Protected)

SPI is, in its simplest form, a three wire serial bus. One signal is a Clock, driven only by the permanent Master device on-board. The others are Data In and Data Out with respect to the Master. The SPX implementation adds additional features, such as chip selects and an interrupt input to the Master. The Master device initiates all SPI transactions. A slave device responds when its Chip Select is asserted and it receives Clock pulses from the Master.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. Please note that since this clock is divided from a 33 MHz PCI clock, the actual generated frequencies are not discrete integer MHz frequencies. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

VersaLogic SPX Expansion Modules

VersaLogic offers a number of SPX modules that provide a variety of standard functions, such as analog input, digital I/O, CANbus controller, and others. These are small boards (1.2” x 3.78”) that can mount on the PC/104 stack, using standard standoffs, or up to two feet away from the baseboard. For more information, contact VersaLogic at Info@VersaLogic.com.

SPI REGISTERS

A set of control and data registers are available for SPI transactions. The following tables describe the SPI control registers (SPICONTROL and SPISTATUS) and data registers (SPIDATA3-0).

SPICONTROL (READ/WRITE) CA8h

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 25: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge
D5-D4	SPILEN(1:0)	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes. **SPILEN1 SPILEN0 Frame Length** 0 0 8-bit 0 1 16-bit 1 0 24-bit 1 1 32-bit
D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (CADh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual

Bit	Mnemonic	Description
D2-D0	SS(2:0)	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the baseboard will be directly controlled by these bits when MAN_SS = 1. There are two sets of definitions which depend on the state of the **ADIOMODE** bit in the Miscellaneous Control Register (**MISCCON**). **ADIOMODE** = 0 (default mode) **SS2 SS1 SS0 Slave Select** 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, J28 pin-8 0 1 0 SPX Slave Select 1, J28 pin-9 0 1 1 SPX Slave Select 2, J28 pin-10 1 0 0 SPX Slave Select 3, J28 pin-11 1 0 1 A/D Converter Channels 1-8 (on-board **U34**) 1 1 0 Digital I/O Channels 1-32 (on-board **U22**,**U51**) 1 1 1 D/A Converter Channels 1-4 (on-board **U26**) **ADIOMODE** = 1 **SS2 SS1 SS0 Slave Select** 0 0 0 Same as for ADIOMODE = 0 0 0 1 SUMIT SPI I/F Chip Select 0, J14 pin-16 0 1 0 SUMIT SPI I/F Chip Select 1, J14 pin-18 0 1 1 A/D Converter Channels 9-16 (on-board **U56**) 1 0 0 D/A Converter Channels 5-8 (on-board **U31**) 1 0 1 Same as for ADIOMODE = 0 1 1 0 Same as for ADIOMODE = 0 1 1 1 Same as for ADIOMODE = 0

SPISTATUS (READ/WRITE) CA9h

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 26: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL(1:0)	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10
D5-D4	SPICLK(1:0)	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPIDATA0 (READ/WRITE) CAAh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) CABh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) CACh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) CADh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit uses the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.

Data returning from the SPI target will normally have its most significant data in the SPIDATA3 register. An exception will occur when LSBIT_1ST = 1 to indicate a right-shift transaction. In this case the most significant byte of an 8-bit transaction will be located in SPIDATA0, a 16-bit transaction's most significant byte will be located in SPIDATA1, and a 24-bit transaction's most significant byte will be located in SPIDATA2.

On-board I/O Devices

Table 27: On-board I/O Devices

I/O Device	Standard I/O Addresses
Reserved	C80h-C9Bh
PLD Internal 8254 Timers	C9Ch-C9Fh
PLED and Product ID Register	CA0h
Revision Indicator Register	CA1h
BIOS and Jumper Status Register	CA2h
Interrupt Control Register	CA3h
Interrupt Status Register	CA4h
8254 Timer Control/Status Register	CA5h
Reserved	CA6h-CA7h
SPX Control Register	CA8h
SPX Status Register	CA9h
SPX Data Register 0	CAAh
SPX Data Register 1	CABh
SPX Data Register 2	CACh
SPX Data Register 3	CADh
Miscellaneous Control Register	CAEh
A/D, D/A Control/Status Register	CAFh
Super I/O Runtime Registers	C00h-C80h
COM0 Serial Port Default	3F8h– 3FFh
COM1 Serial Port Default	2F8h– 2FFh

PLED and Product Code Register

PLEDPC (Read/Write) CA0h

D7	D6	D5	D4	D3	D2	D1	D0
PLED	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Table 28: PLEDPC Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J29. 0 = Turns LED off 1 = Turns LED on
D6-D0	PC(6:0)	**Product Code** — These bits are hard-coded to represent the product type. The VL-EBX-41 is uniquely identified by the code 0000101. **PC6 PC5 PC4 PC3 PC2 PC1 PC0 Product Code** 0 0 0 1 1 0 0 VL-EBX-41 These bits are read-only.

PLD Revision and Type Register

REVTYP (Read-only) CA1h

D7	D6	D5	D4	D3	D2	D1	D0
PLD4	PLD3	PLD2	PLD1	PLD0	TEMP	CUSTOM	BETA

This register is used to indicate the PLD revision level and model of the Copperhead.

Table 29: Revision and Type Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	PLD(4:0)	**PLD Code Revision Level** — These bits are hard-coded and represent the PLD code revision. **PLD4 PLD3 PLD2 PLD1 PLD0 Revision** 0 0 0 1 0 Rev. 1.00A These bits are read-only.
D2	TEMP	**Temperature Rating** — This bit indicates whether the VL-EBX-41 is rated for standard or industrial temperature operation. 0 = Standard temperature operation 1 = Industrial temperature operation This bit is read-only.
D1	CUSTOM	**PLD Class** — This bit indicates whether the PLD code is standard or customized. 0 = Standard PLD code 1 = Custom PLD code This bit is read-only.
D0	BETA	**Production Level** — This bit indicates if the PLD code is at the beta or production level. 0 = Production level PLD 1 = Beta level PLD This bit is read-only.

BIOS and Jumper Status Register

BIOSJSR (Read/Write) CA2h

D7	D6	D5	D4	D3	D2	D1	D0
BIOS_JMP	BIOS_OR	BIOS_SEL	Reserved	Reserved	Reserved	Reserved	GPI_JMP

Table 30: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	BIOS_JMP	**System BIOS Selector Jumper Status** — Indicates the status of the system BIOS selector jumper at V6[1-2]. 0 = Jumper installed – Primary system BIOS selected 1 = No jumper installed – Secondary system BIOS selected This bit is read-only.
D6	BIOS_OR	**BIOS Jumper Override** — Overrides the system BIOS selector jumper and selects the BIOS with BIOS_SEL. 0 = No BIOS override 1 = BIOS override
D5	BIOS_SEL	**BIOS Select** — Selects the system BIOS when BIOS_OR is set. 0 = Primary BIOS selected 1 = Secondary BIOS selected
D4-D1	Reserved	These bits are reserved. Only write 0 to these bits and ignore all read values.
D0	GPI_JMP	General Purpose Jumper Status – Indicates the status of the general purpose jumper at V6[3-4].

Appendix A – References

CPU	
Intel 3rd Generation Intel® Core™ Quad or Dual-Core Processor	Mobile 3rd Generation Intel® Core™ Processor Family Datasheet Vol. 1, Vol. 2, Update
Chipset	
Intel QM77 Platform Controller Hub	Mobile Intel® QM77 Express Chipset (Intel® BD82QM77 PCH)
Ethernet Controller	
Intel 82574IT Ethernet Controller	Intel 8257IT Datasheet
PCIe/104 Interface	PCI/104-Express & PCIe/104 Express Specification
SUMIT Interface	SUMIT Specification

Appendix B – Custom Programming

B

PLD Interrupts

The PLD can generate interrupts for the internal 8254 timers and the external SPI interrupt (which includes the DIO device interrupt). The SPI interrupt settings are discussed in the section on "SPX Expansion Bus." This section covers the interrupt settings for the 8254 timers.

INTERRUPT CONTROL REGISTER

This register enables interrupts.

IRQCTRL (Read/Write) CA3h

D7	D6	D5	D4	D3	D2	D1	D0
IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	reserved	IMSK_TC5	IMSK_TC4	IMSK_TC3

Table 31: Interrupt Control Register Bit Assignments

Bit	Mnemonic	Description
D7	IRQEN	IRQ Enable — Enables or disables an interrupt. 0 = Disable interrupt 1 = Enable interrupt
D6-D5	IRQSEL(2:0)	Specifies the interrupt mapping (this setting is ignored when IRQEN = 0 … interrupts are disabled): "000" IRQ3 (default) "001" IRQ4 "010" IRQ5 "011" IRQ10 "100" IRQ6 "101" IRQ7 "110" IRQ9 "111" IRQ11
D4	Reserved	These bits are reserved. Only write 0 to these bits and ignore all read values.
D2	IMASK_TC5	Mask for the 8254 Timer #5 output (terminal count) Interrupt. 0 = Disable interrupt 1 = Enable interrupt
D1	IMASK_TC4	Mask for the 8254 Timer #4 output (terminal count) Interrupt. 0 = Disable interrupt 1 = Enable interrupt
D0	IMASK_TC3	Mask for the 8254 Timer #3 output (terminal count) Interrupt. 0 = Disable interrupt 1 = Enable interrupt

Note: IRQ3, IRQ4, IRQ5, IRQ10 are also defined for the SPX interface interrupts. If one of these interrupts is selected for the SPX interface and also enabled here for the timer interrupts, then the interrupt sources are combined (i.e., logically OR'd).

INTERRUPT STATUS REGISTER

This register is used for reading the status of interrupts generated by the PLD.

IRQSTAT (Read-Status/Write-Clear) CA4h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	ISTAT_TC5	ISTAT_TC4	ISTAT_TC3

Table 32: Interrupt Status Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	Reserved	These bits are reserved. Only write 0 to these bits and ignore all read values.
D2	ISTAT _TC5	Status for the 8254 Timer #5 output (terminal count) Interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transitioned from a 0 to a 1 level This bit is read-status and a write-1-to-clear.
D1	ISTAT _TC4	Status for the 8254 Timer #4 output (terminal count) Interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transitioned from a 0 to a 1 level This bit is read-status and a write-1-to-clear.
D0	ISTAT _TC3	Status for the 8254 Timer #3 output (terminal count) Interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transitioned from a 0 to a 1 level This bit is read-status and a write-1-to-clear.

The interrupt status register is valid whether the interrupt mask is set or not for the interrupt (that is, it can be used for polled status). An interrupt status is acknowledged (cleared to a 0) by writing a '1' to the status bit.

The PLD implements an 8254 timer (consisting of three individual timers). The outputs of these timers can generate interrupts when they transition from a 0 level to a 1 level (edge sensitive).

8254 Timer Control Register

This register is used to set modes related to the inputs on the 8254 Timers.

TIMCNTRL (Read/Write) CA5h

D7	D6	D5	D4	D3	D2	D1	D0
TIM5GATE	TIM4GATE	TIM3GATE	TM4MODE	TM4SEL	TM3SEL	Reserved	Reserved

Table 33: 8254 Timer Control Register Bit Assignments

Bit	Mnemonic	Description
D7	TIM5GATE	Sets the level on the Gate input for the 8254 Timer #5. 0 = GCTC5 Gate is disabled (set to a logic 0) 1 = GCTC5 Gate is enabled (set to a logic 1)
D6	TIM4GATE	Sets the level on the Gate input for the 8254 Timer #4. 0 = GCTC4 Gate is disabled (set to a logic 0) 1 = GCTC4 Gate is enabled (set to a logic 1)
D5	TIM3GATE	Sets the level on the Gate input for the 8254 Timer #3. 0 = GCTC3 Gate is disabled (set to a logic 0) 1 = GCTC3 Gate is enabled (set to a logic 1)
D4	TM4MODE	Configure how the 8254 Timer #4 and #5 are used. 0 – Timer #4 is cascaded with Timer #5 for a 32-bit timer 1 – Timer #4 operates in normal 16-bit mode
D3	TM4SEL	Configure the clock source for 8254 Timer #4. 0 – Timer #4 input clock is 4.167 MHz internal clock (PCI clock divided by 8) 1 – Timer #4 input clock is from User I/O connector Input ICTC4
D2	TM3SEL	Configure the clock source for 8254 Timer #3. 0 – Timer #3 input clock is 4.167 MHz internal clock (PCI clock divided by 8) 1 – Timer #3 input clock is from User I/O connector Input ICTC3
D1-D0	Reserved	These bits are reserved. Only write 0 to these bits and ignore all read values.

An 8254 timer is implemented in the PLD. It contains three independent 16-bit timers. It is fully software compatible with the Intel 8254, except that only binary counting modes are implemented (the BCD control bit is implemented but ignored). See the Intel 82C54 Programmable Interval Timer Datasheet for register definitions and programming information.

There is an option to cascade two of the timers together in a 32-bit mode. The timers are identified as Timer 3, 4, and 5. When Timers 4 and 5 are cascaded, Timer 4 is the LS 16-bits and Timer 5 is the MS 16-bits. In this 32-bit cascade mode the timer output of Timer 4 feeds the clock input of Timer 5. In this mode Timer 4 would normally be set so that it generates a clock after counting the full 16-bit range, but there is no requirement to do this.

The 32-bit cascade mode is set in TM4MODE in the Timer Control Register. There are also internal or external clock selections for the timers in this register using the external clocks ICTC3 and ICTC4 signals on the connector at J19. The internal clock is the PCI clock divided by 8 (33.33 MHz / 8 = 4.167 MHz). ICTC3 can only be used with Timer 3. ICTC4 can only be used with Timer 4. The clock for Timer 5 is always the internal clock except in the 32-bit cascade mode when the output from Timer 4 is the clock for Timer 5.

The timer outputs can generate interrupts. When a timer output transitions from a 0 to a 1 then an interrupt status bit is set and can generate an interrupt. This bit sticks until cleared.

By default there are two external timer input clocks (ICTC3, ICTC4) and two timer outputs (OCTC3, OCTC4) on connector J19. To use all three of the 16-bit timers, timers 4 and 5 are configured in 32-bit mode by default. Custom options are available that can expand the external controls to allow for three clock inputs and four, timer outputs as well as three timer gate inputs for all three 16-bit timers by using some of the digital I/O signal pins on J19.

Miscellaneous Control Register

This register is used to configure the control of the mSATA/PCIe Minicard slot multiplexer and for controlling the SPI access.

MISCCON (Read/Write) CAEh

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	MUXSEL2	MUXSEL1	MUXSEL0	Reserved	Reserved	Reserved	ADIOMODE

Table 34: mSATA/PCIe Mux Control Register Bit Assignments

Bit	Mnemonic	Description
D7	Reserved	These bits are reserved. Only write 0 to these bits and ignore all read values.
D6-D4	MUXSEL(2:0)	mSATA/PCIe Minicard Mux Controls (these are typically only configured in the BIOS setup): "000" Use only J8 Pin 43. This is based on a newer mSATA module detection method recommended by Intel due to conflicts with J8 Pin 51. Reliable for all PCIe Minicards but some mSATA modules do not ground this so using setting "010" is recommended. "001" Use only J8 Pin 51. This is only reliable for mSATA modules which drive this signal High and is not recommended. "010" Use either J8 Pin 43 or J8 Pin 51 to detect mSATA modules. This works on the majority of modules and is the recommended setting. Note: This is the BIOS default setting. "011" Force the multiplexer to always be used as a PCIe Minicard. "100" Force the multiplexer to always be used as an mSATA module. "101" Undefined "110" Undefined "111" Undefined
D3-D1	Reserved	These bits are reserved. Only write 0 to this bit and ignore read values.
D0	ADIOMODE	Selects how the 3 bits in the SS field of the SPICONTROL register are decoded (see decodings in the SPICONTROL register documentation): 0 Use standard decodes (primarily used if accessing more than 2 SPX Expansion interface devices or on products with 8 analog inputs and 4 analog outputs or on products that do not use the SUMIT SPI interfaces). This is the power-on-reset default setting. 1 Use alternate decodes (primarily used on products with 16 analog inputs and 8 analog outputs or for accessing the SUMIT SPI interfaces).

A/D and D/A Control/Status Register

This register is used to control A/D and D/A conversion.

ADCONSTAT (Read/Write) CAFh

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	DACLDA1	DACLDA0	ADCBUSY1	ADCBUSY0	ADCONVST1	ADCONVST0

Table 35: A/D, D/A Control/Status Register Bit Assignments

Bit	Mnemonic	Description
D7-D6	Reserved	These bits are reserved. Only write 0 to these bits and ignore all read values.
D5	DACLDA1	This is a write-only (pulsed) bit. When a '1' is written it will strobe the LDAC signal on the LTC2634 D/A Converter for channels 4-8. Writing a '0' is ignored. LDAC is only used to update all 4 channels in one operation.
D4	DACLDA0	This is a write-only (pulsed) bit. When a '1' is written it will strobe the LDAC signal on the LTC2634 D/A Converter for channels 1-4. Writing a '0' is ignored. LDAC is only used to update all 4 channels in one operation.
D3	ADCBUSY1	This read-only status bit returns the conversion status for the LTC1857 A/D for channels 9-16 0 – A/D is idle. 1 – A/D is busy doing a conversion.
D2	ADCBUSY0	This read-only status bit returns the conversion status for the LTC1857 A/D for channels 1-8 0 – A/D is idle. 1 – A/D is busy doing a conversion.
D1	ADCONVST1	This is a write-only (pulsed) bit. When a '1' is written it will start a conversion on the LTC1857 A/D converter for channels 9-16. Writing a '0' is ignored.
D0	ADCONVST0	This is a write-only (pulsed) bit. When a '1' is written it will start a conversion on the LTC1857 A/D converter for channels 1-8. Writing a '0' is ignored.