Reference Manual

DOC. REV. 3/17/2009

EPM-5 (Puma)

AMD GX Based SBC with Ethernet, Video, and PC/104-*Plus* interface

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MEPM5

Product Release Notes

Rev 7 Release – Production release.

- See KnowledgeBase article VT1597 for changes made to Rev. 7.00.

Rev 6 Release – Production release.

- For the latest BIOS and PLD updates, go to the EPM-5 support page.
- See KnowledgeBase article VT1568 for changes made to Rev. 6.00.

Rev 5 Release – Production release.

- Heat sink added to CPU to improve thermal margins.
- BIOS upgraded to version 5.3.103. Results in lower power draw in sleep state (suspend-to-RAM).
- Converted jumper block V3 into two separate blocks, V3 and V5.
- Removed Ethernet EMI capacitors to allow auto MDI/MDIX operation.
- [R5.01] New PLD code enables true 16-bit I/O transfers on ISA bus. See KnowledgeBase article VT1477 for the update instructions.
- [R5.01] BIOS upgraded to version 5.3.104: Fixes Ultra DMA IDE modes in Linux, frees COM port I/O resources.
- [R5.07] BIOS revision improves LVDS panel dot clock rate at high resolution and PCI IRQ line routing. PLD revision implements GNT-REQ synchronization with the PCI clock and IOCHRDY on the ISA bus.

Rev 4 Release – Production release.

- ACPI pushbutton control jumper.
- ISA IRQ5 removed.
- RoHS compliance.

Rev 3 Release – Charlie release.

- USB 2.0.
- Audio interface.
- ACPI power management: standby, suspend to RAM support.

Rev 2 Release – Beta release.

Rev 1 Release – Pre-production only. No customer releases.

Support Page

The **EPM-5 support page**, at **http://www.VersaLogic.com/private/pumasupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for EPM-5 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

Contents

1 Introduction

Description

FEATURES AND CONSTRUCTION

The EPM-5 is a feature-packed single board computer (SBC) designed for OEM control projects requiring fast processing and designed-in reliability and longevity (product lifespan). Its features include:

- AMD GX 500 microcontroller
- 256 MB soldered on system DDR SDRAM
- CompactFlash site
- 10/100 Ethernet interface
- Flat Panel Display support
- PC/104 (ISA) and PC/104-*Plus* (PCI) expansion
- ATA-5 IDE controller
- Four USB 2.0 ports for keyboard, mouse, floppy, and other devices
- TVS devices for ESD protection
- Parallel port
- Audio
- CPU temperature sensor
- One RS-232 COM port and two RS422/485 COM ports
- Vcc sensing reset circuit
- PC/104-compliant 3.55” x 3.95” footprint
- Field upgradeable BIOS with OEM enhancements
- Latching I/O connectors
- ACPI standby mode (suspend to RAM)
- Customizing available
- Low-power fanless version

The EPM-5 is a PC/104-*Plus*-compliant single board computer with an AMD GX 500 processor. The board is compatible with popular operating systems such as Windows, QNX, VxWorks and Linux.

The EPM-5 features high reliability design and construction, including latching I/O connectors, voltage sensing reset circuits, and self-resetting fuses on the 5V supply to the USB ports.

EPM-5 boards are subjected to 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service and product longevity for this exceptional SBC.

A full complement of standard I/O ports is included on the board. Additional I/O expansion is available through the high-speed PC/104-*Plus* (PCI) and PC/104 (ISA) connectors. The EPM-5 is equipped with a multifunction utility cable, CBL/CBR-5010 (breakout board), that provides standard I/O interfaces, including three COM ports, four USB ports, two LEDs, and a pushbutton reset, among others.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 3.55" x 3.775" (PC/104 standard) with 0.20" connector overhangs in designated connector areas

Storage Temperature: -40° C to 85° C

Operating Temperature:

0° C to +60° C free air, no airflow, standard version
-40° C to +85° C free air, extended temperature version

Power Requirements: *(with 256 MB soldered on system DDR SDRAM, keyboard and mouse, Running Windows XP)*

EPM-5c, g AMD CPU 5V ± 5% @ 1.0 A (5.0 W) typ.
EPM-5h AMD CPU 5V ± 5% @ 1.0 A (5.0 W) typ.
+3.3V or ± 12V may be required by some expansion modules

System Reset:

V_{cc} sensing, resets below 4.70V typ.

DRAM:

256 MB soldered-on DDR SDRAM

Video Interface:

Up to 1280 x 1024 (24 bits)
Standard RGB analog output (VESA DDC not supported)
LVDS output for TFT FPDs

IDE Interface:

One-channel, 44-pin, 2mm connector. Supports up to and including UDMA5.
Supports two Parallel ATA IDE devices (hard drive, CD-ROM, CF, etc.)

Compact Flash:

Shares IDE channel, master or slave

Ethernet Interface:

Intel 82551ER based 10/100 Fast Ethernet Controller

COM1 Interface:

RS-232, 16C550 compatible, 115 kbps max.

COM3–4 Interface:

RS-422/485, 16C550 compatible, 460 kbps max.

LPT Interface:

Bi-directional/EPP/ECP compatible

BIOS: General Software Embedded BIOS© 2000 with OEM enhancements
Field-upgradeable with Flash BIOS Update Utility

Bus Speed:

PC/104-*Plus* (PCI): 33MHz
PC/104 (ISA): 8MHz

Compatibility:

PC/104 – Partial compliance (See PC/104 expansion bus)
Embedded-PCI (PC/104-*Plus*) – full compliance, 3.3V signaling

Weight:

EPM-5g – 0.115 kg (0.253 lbs)
EPM-5h – 0.125 kb (0.275 lbs)

Specifications are subject to change without notice.

EPM-5 Block Diagrams

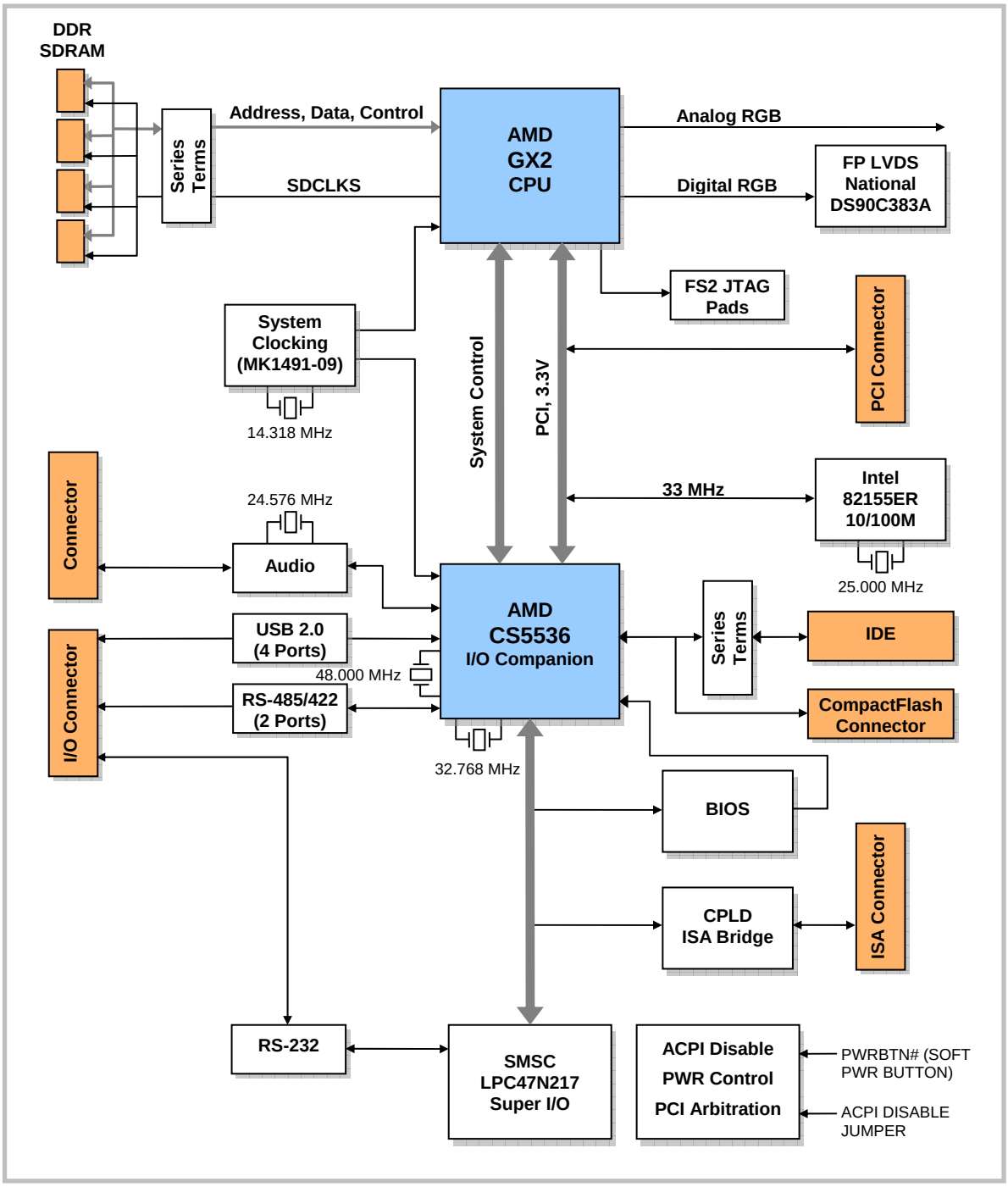


Figure 1. System Block Diagram

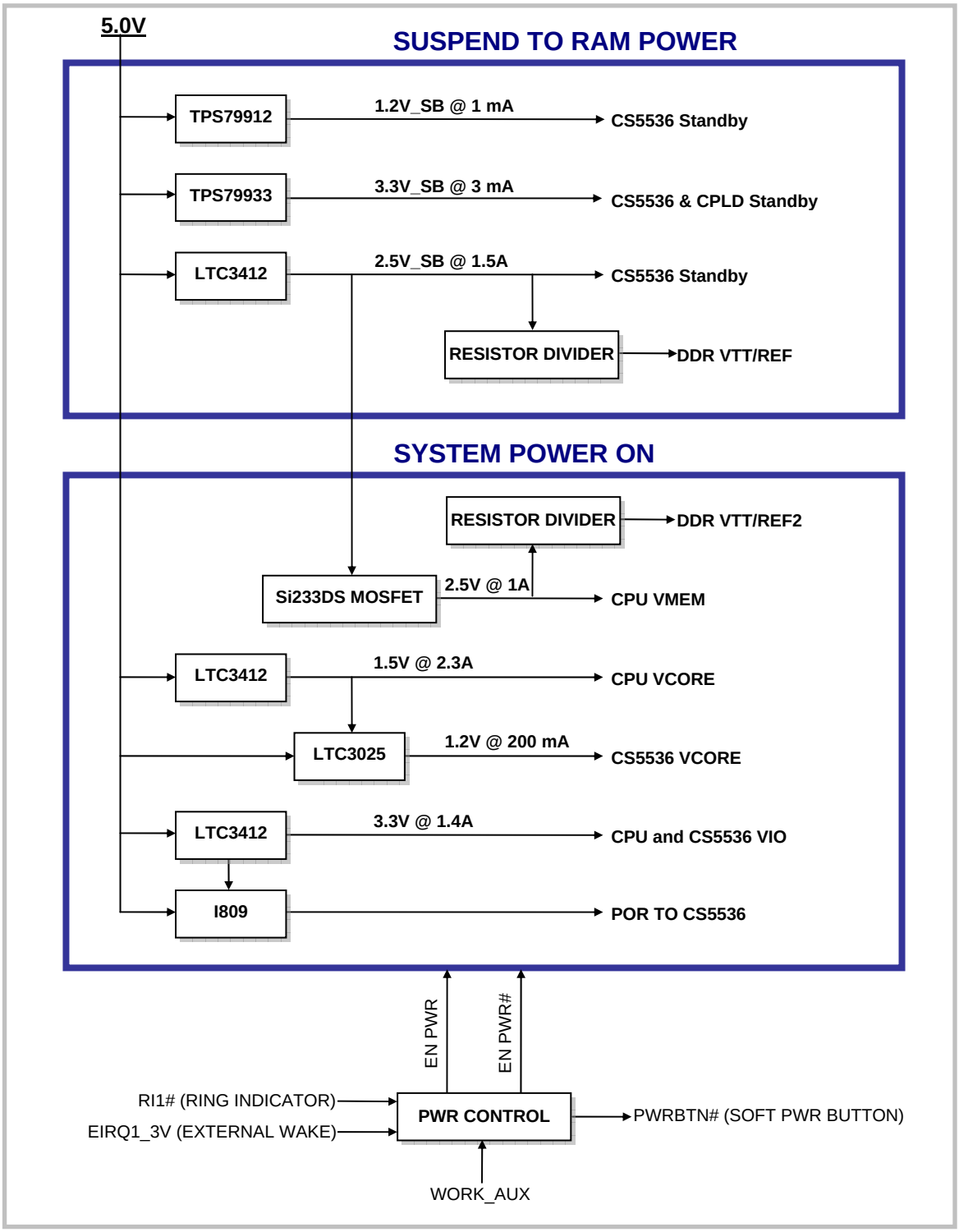


Figure 2. Power Control Block Diagram

RoHS Compliance

The EPM-5, Revision 4.xx and above, is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

ROHS COMPLIANT CABLES

Adapter cables for the EPM-5 are available in RoHS compliant and RoHS noncompliant versions. Compliance or noncompliance is indicated by the part number prefix. "CBR" indicates RoHS compliance. "CBL" indicates RoHS noncompliance. For applications that require RoHS compliance, use only the RoHS compliant ("CBR" version) cables.

Warnings

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EPM-5.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner.

HANDLING CARE

Warning! Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling (while changing the CompactFlash module), resulting in CMOS resetting to factory defaults.

Technical Support

If you are unable to solve a problem after reading this manual please visit the EPM-5 Product Support web page at **http://www.VersaLogic.com/private/pumasupport.asp**. If you have further questions, contact VersaLogic technical support at (541) 485-8575. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

EPM-5 Support Website

http://www.VersaLogic.com/private/pumasupport.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contacted if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning.

Configuration and Setup 2

Initial Configuration

The following components are recommended for a typical development system.

- EPM-5 Computer
- ATX Power Supply
- SVGA Video Monitor
- Standard I/O Utility Cable (CBL/CBR-5010)
- USB Keyboard
- USB Floppy Disk Drive
- IDE Hard Drive (optional)
- IDE CD ROM Drive (optional)

The following VersaLogic cables are recommended.

- CBL/CBR-1201 – Video adapter cable
- CBL/CBR-5009A – Utility I/O cable
- CBL/CBR-5010B – Breakout board
- CBL/CBR-4406 – IDE data cable
- CBL/CBR-4405 – IDE adapter board, if you are using drives with 40-pin connectors
- CBL/CBR-1008 – Power adapter cable

Note: Adapter cables for the EPM-5 are available in RoHS compliant and RoHS noncompliant versions (see "RoHS Compliance"). Compliance or noncompliance is indicated by the part number prefix. "CBR" indicates RoHS compliance. "CBL" indicates RoHS noncompliance. For applications that require RoHS compliance, use only the RoHS compliant ("CBR" version) cables.

You will also need a Windows (or other OS) installation CD.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The EPM-5 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the EPM-5 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damaged that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the EPM-5 and their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

Figure 3 shows a typical start-up configuration (using RoHS compatible cables).

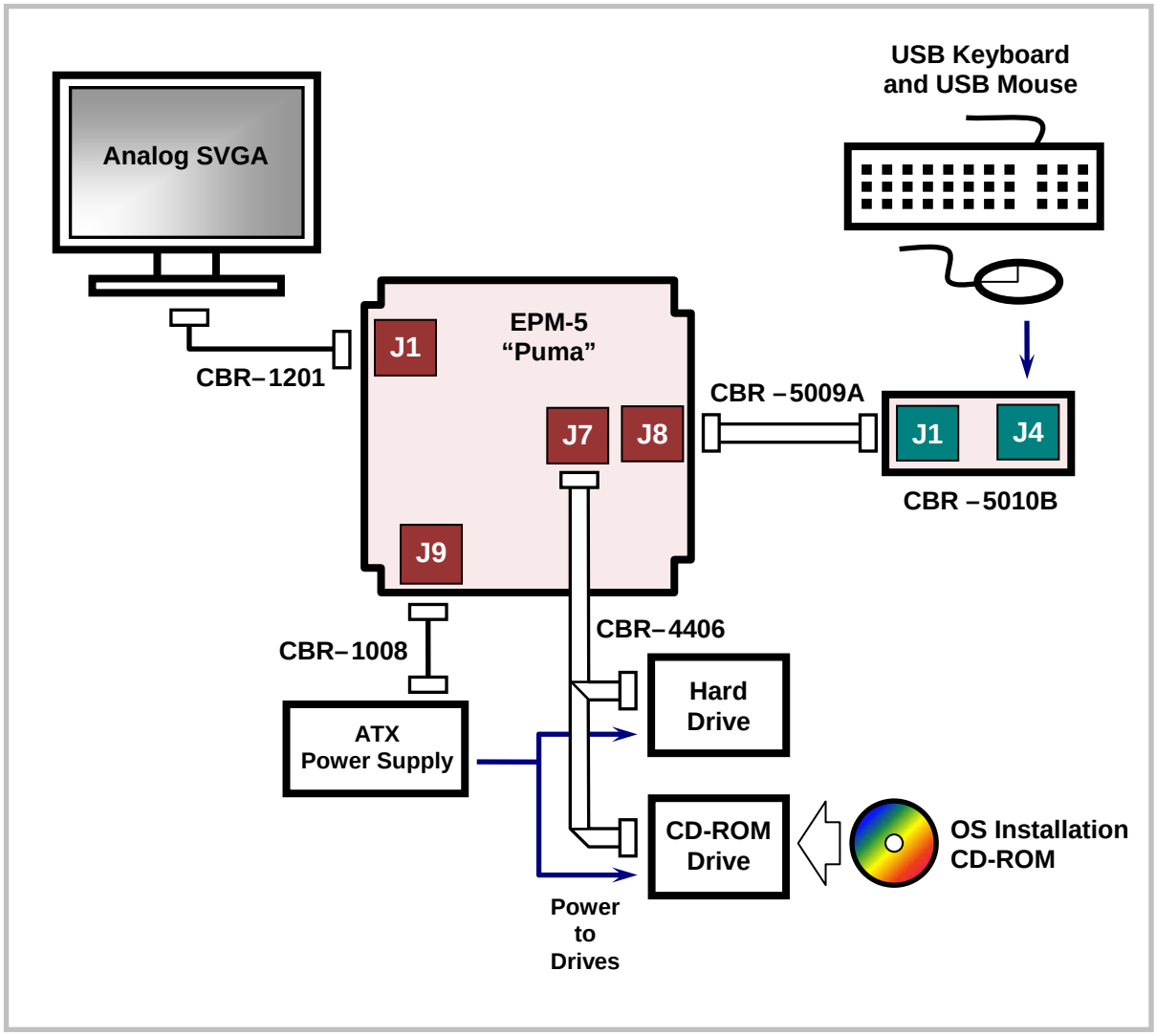


Figure 3. Typical Start-up Configuration

1. Attach Power

- Plug the power adapter cable CBL/CBR-1008 into socket J9. Attach the motherboard connector of the ATX power supply to the adapter.

2. Attach Cables and Peripherals

- Plug the video adapter cable CBL/CBR-1201 into socket J1. Attach the video monitor interface cable to the video adapter.
- Plug the breakout cable CBL-5009A into socket J8. If necessary, attach the breakout board CBL-5010B to the cable. (The cable and board are shipped attached.)
- Plug a USB keyboard and USB floppy drive into socket J4 of the breakout board.
- Plug the hard drive data cable CBL/CBR-4406 into socket J7. Attach a hard drive and CD-ROM drive to the connectors on the cable. If the hard drive is 3.5", use the 2mm to 0.1" adapter CBL/CBR-4405 to attach the IDE cable.
- Attach an ATX power cable to any 3.5" drive (hard drive or CD-ROM drive).

- Set the hard drive jumper for master device operation and the CD-ROM drive jumper for slave device operation.

3. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the EPM-5 and peripheral devices.

4. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

5. Change CMOS Setup Settings

- Enter CMOS Setup by pressing Delete during the early boot cycle.
- Select Basic Configuration and set or verify the following settings:

```
DRIVE ASSIGNMENT ORDER | Drive C: Ide 0/Pri Master

ATA DRV ASSIGNMENT | Ide 0: 3 = AUTOCONFIG, LBA
ATA DRV ASSIGNMENT | Ide 1: 5 = IDE CDROM

BOOT ORDER | Boot 1st: CDROM
BOOT ORDER | Boot 2nd: Drive C:
```

- Before saving the CMOS Setup settings, insert the Windows (or other OS) installation disk in the CD-ROM drive so it will be accessed when the system reboots.
- Press ESC and select the option to save the new parameters to CMOS RAM. The system will reboot.

6. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

  Note: If you intend to operate the EPM-5 under Windows XP or Windows XP Embedded, be sure to use Service Pack 2 (SP2) for full support of the latest CS5536 I/O hub and its USB 2.0 features.

CMOS Setup

The default CMOS Setup parameters for the EPM-5 are shown below. See VersaLogic KnowledgeBase article VT1458 – EPM-5 CMOS Setup Reference for more information about these parameters.

Basic CMOS Configuration

```
+--------------------------------------------------------------------------+
|                System BIOS Setup - Basic CMOS Configuration              |
|           (C) 2005 General Software, Inc. All rights reserved            |
+--------------------------+-------------------+-----------------------------+
| DRIVE ASSIGNMENT ORDER:  | Date:>Jun 15, 2006 | Typematic Delay  : 250 ms  |
| Drive A: (None)          | Time: 00 : 00 : 00 | Typematic Rate   : 30 cps  |
| Drive B: (None)          | NumLock:  Disabled | Seek at Boot     : None    |
| Drive C: Ide 0/Pri Master +-------------------+ Show "Hit Del"   : Enabled |
| Drive D: (None)          | BOOT ORDER:        | Config Box       : Enabled |
| Drive E: (None)          | Boot 1st: Drive C: | F1 Error Wait    : Enabled |
| Drive F: (None)          | Boot 2nd: (None)   | Parity Checking  : (Unused)|
| Drive G: (None)          | Boot 3rd: (None)   | Memory Test Tick : Enabled |
| Drive H: (None)          | Boot 4th: (None)   | Debug Breakpoints: (Unused)|
| Drive I: (None)          | Boot 5th: (None)   | Debugger Hex Case: Upper   |
| Drive J: (None)          | Boot 6th: (None)   | Memory Test : StdLo  FastHi|
| Drive K: (None)          +-------------------+-----------------+-----------+
| Boot Method: Boot Sector | ATA DRV ASSIGNMENT:  Sect  Hds  Cyls | Memory    |
+--------------------------+ Ide 0: 3 = AUTOCONFIG, LBA           |  Base:    |
| FLOPPY DRIVE TYPES:      | Ide 1: 3 = AUTOCONFIG, LBA           |   632KB   |
| Floppy 0: Not installed  | Ide 2: 3 = AUTOCONFIG, LBA           |  Ext:     |
| Floppy 1: Not installed  | Ide 3: 3 = AUTOCONFIG, LBA           |   235MB   |
+--------------------------+--------------------------------------+-----------+
```

Features Configuration

```
+--------------------------------------------------------------------------+
|                System BIOS Setup - Features Configuration                |
|           (C) 2005 General Software, Inc. All rights reserved            |
+-------------------------------------+------------------------------------+
| ACPI 1.0                 :>Enabled  | System Management Mode   : Enabled |
| Advanced Power Management: Enabled  | Splash Screen            : Disabled|
| System Management BIOS   : Enabled  | Firmbase Instrumentation : Disabled|
| Primary IDE UDMA         : Enabled  | Secondary IDE UDMA       : Disabled|
| Console Redirection      : Auto     | Firmbase Debug Console   : None    |
| UsbMassStorage           : Enabled  | AtaMassStorage           : Disabled|
| Usb20                    : Disabled | Shell                    : Disabled|
+-------------------------------------+------------------------------------+
```

Custom Configuration

```
+--------------------------------------------------------------------------+
|                System BIOS Setup - Custom Configuration                  |
|           (C) 2005 General Software, Inc. All rights reserved            |
+-------------------------------------+------------------------------------+
| PCI INT A Assignment  :>IRQ 5       | ISA IRQ 3             : Disabled   |
| PCI INT B Assignment  : IRQ 5       | ISA IRQ 4             : Disabled   |
| PCI INT C Assignment  : IRQ 5       | ISA IRQ 10            : Disabled   |
| PCI INT D Assignment  : IRQ 11      | COM1 (3F8) RS-232     : IRQ4       |
| Video buffer size     : 16 MB       | COM3 (3E8) RS-422/485 : Disabled   |
| Video device mode     : Disabled    | COM4 (2E8) RS-422/485 : Disabled   |
| Video refresh rate    : 60 Hz       | LPT1 (378) Enable/IRQ : No IRQ     |
| Video data width      : 8 bit       | Parallel Port Mode    : Printer    |
| Video panel type      : TFT         | BIOS Extension        : Disabled   |
| Primary video device  : Auto        | Write Protect BIOS    : Disabled   |
| CPU Temperature Thresh: 100*C       | IDE cable type        : 40-Wire    |
| CPU Over Temp IRQ     : No IRQ      | Periodic SMM IRQ      : Enabled    |
+-------------------------------------+------------------------------------+
```

Plug-n-Play Configuration

```
+---------------------------------------------------------------------------+
|               System BIOS Setup - Plug-n-Play Configuration               |
|           (C) 2005 General Software, Inc. All rights reserved             |
+-------------------------------------+-------------------------------------+
| Enable PnP Support       :>Enabled  | Enable PnP O/S          : Enabled   |
|                                     |                                     |
| Assign IRQ0 to PnP       : Disabled | Assign IRQ8 to PnP      : Disabled  |
| Assign IRQ1 to PnP       : Enabled  | Assign IRQ9 to PnP      : Disabled  |
| Assign IRQ2 to PnP       : Enabled  | Assign IRQ10 to PnP     : Disabled  |
| Assign IRQ3 to PnP       : Enabled  | Assign IRQ11 to PnP     : Enabled   |
| Assign IRQ4 to PnP       : Disabled | Assign IRQ12 to PnP     : Enabled   |
| Assign IRQ5 to PnP       : Enabled  | Assign IRQ13 to PnP     : Enabled   |
| Assign IRQ6 to PnP       : Disabled | Assign IRQ14 to PnP     : Enabled   |
| Assign IRQ7 to PnP       : Disabled | Assign IRQ15 to PnP     : Enabled   |
|                                     |                                     |
| Assign DMA0 to PnP       : Disabled | Assign DMA4 to PnP      : Enabled   |
| Assign DMA1 to PnP       : Disabled | Assign DMA5 to PnP      : Enabled   |
| Assign DMA2 to PnP       : Disabled | Assign DMA6 to PnP      : Disabled  |
| Assign DMA3 to PnP       : Enabled  | Assign DMA7 to PnP      : Enabled   |
+-------------------------------------+-------------------------------------+
```

Shadow Configuration

```
+---------------------------------------------------------------------------+
|               System BIOS Setup - Shadow/Cache Configuration              |
|           (C) 2005 General Software, Inc. All rights reserved             |
+-------------------------------------+-------------------------------------+
| Shadowing               :>Chipset   | Shadow 16KB ROM at C000 : Enabled   |
| Shadow 16KB ROM at C400 : Enabled   | Shadow 16KB ROM at C800 : Disabled  |
| Shadow 16KB ROM at CC00 : Disabled  | Shadow 16KB ROM at D000 : Disabled  |
| Shadow 16KB ROM at D400 : Disabled  | Shadow 16KB ROM at D800 : Disabled  |
| Shadow 16KB ROM at DC00 : Enabled   | Shadow 16KB ROM at E000 : Enabled   |
| Shadow 16KB ROM at E400 : Enabled   | Shadow 16KB ROM at E800 : Enabled   |
| Shadow 16KB ROM at EC00 : Enabled   | Shadow 64KB ROM at F000 : Enabled   |
+-------------------------------------+-------------------------------------+
```

Note: Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above**.**

Operating System Installation

The standard PC architecture used on the EPM-5 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EPM-5 Product Support web page at **http://www.VersaLogic.com/private/pumasupport.asp.**

Dimensions and Mounting

The EPM-5 complies with all PC/104-*Plus* standards. Dimensions are given below to help with pre-production planning and layout.

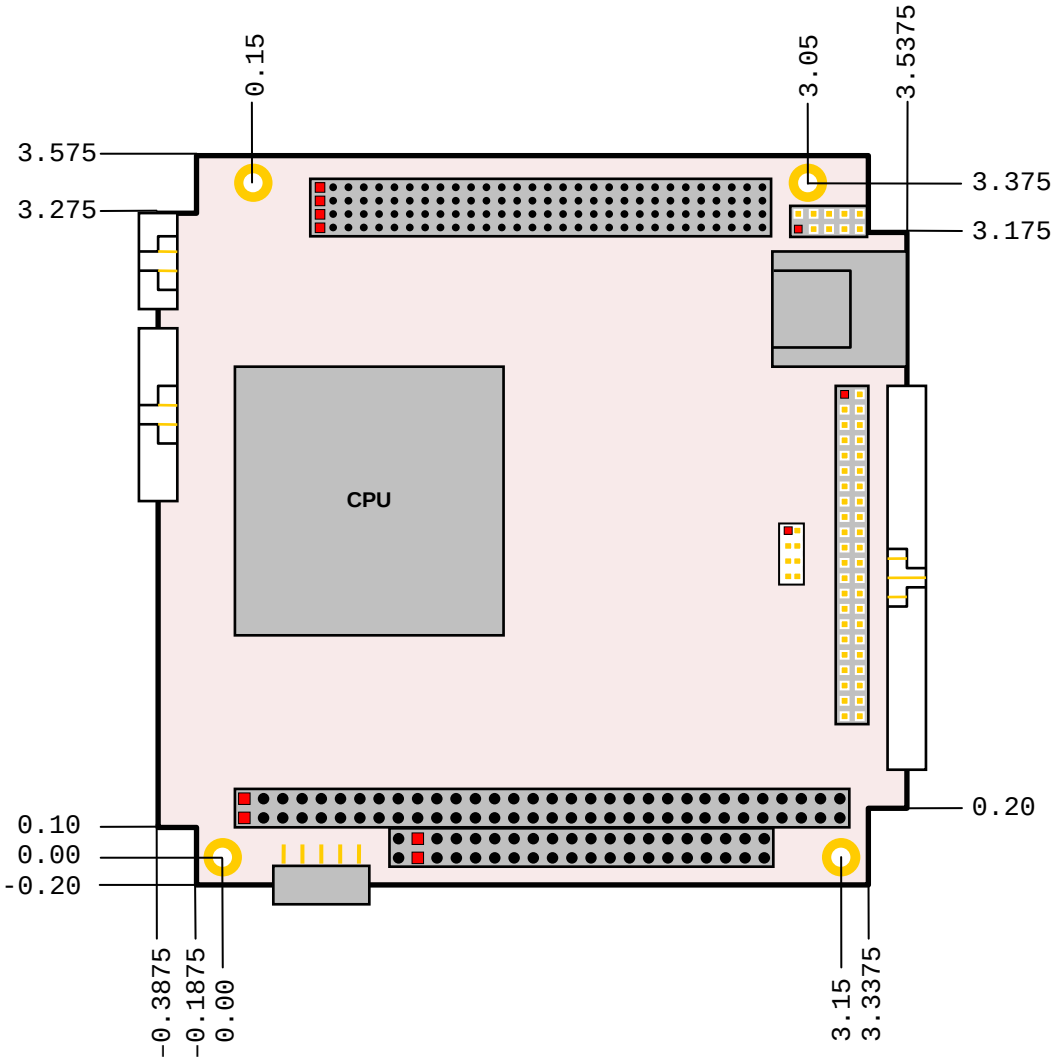


Figure 4.EPM-5 Dimensions and Mounting Holes

(Not to scale. All dimensions in inches.)

SIDE PROFILE

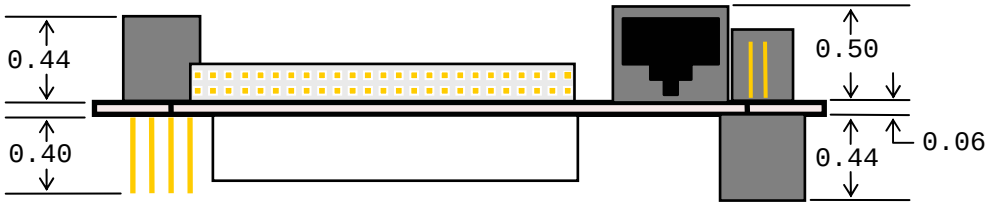


Figure 5. EPM-5 Side Profile
(Not to scale. All dimensions in inches.)

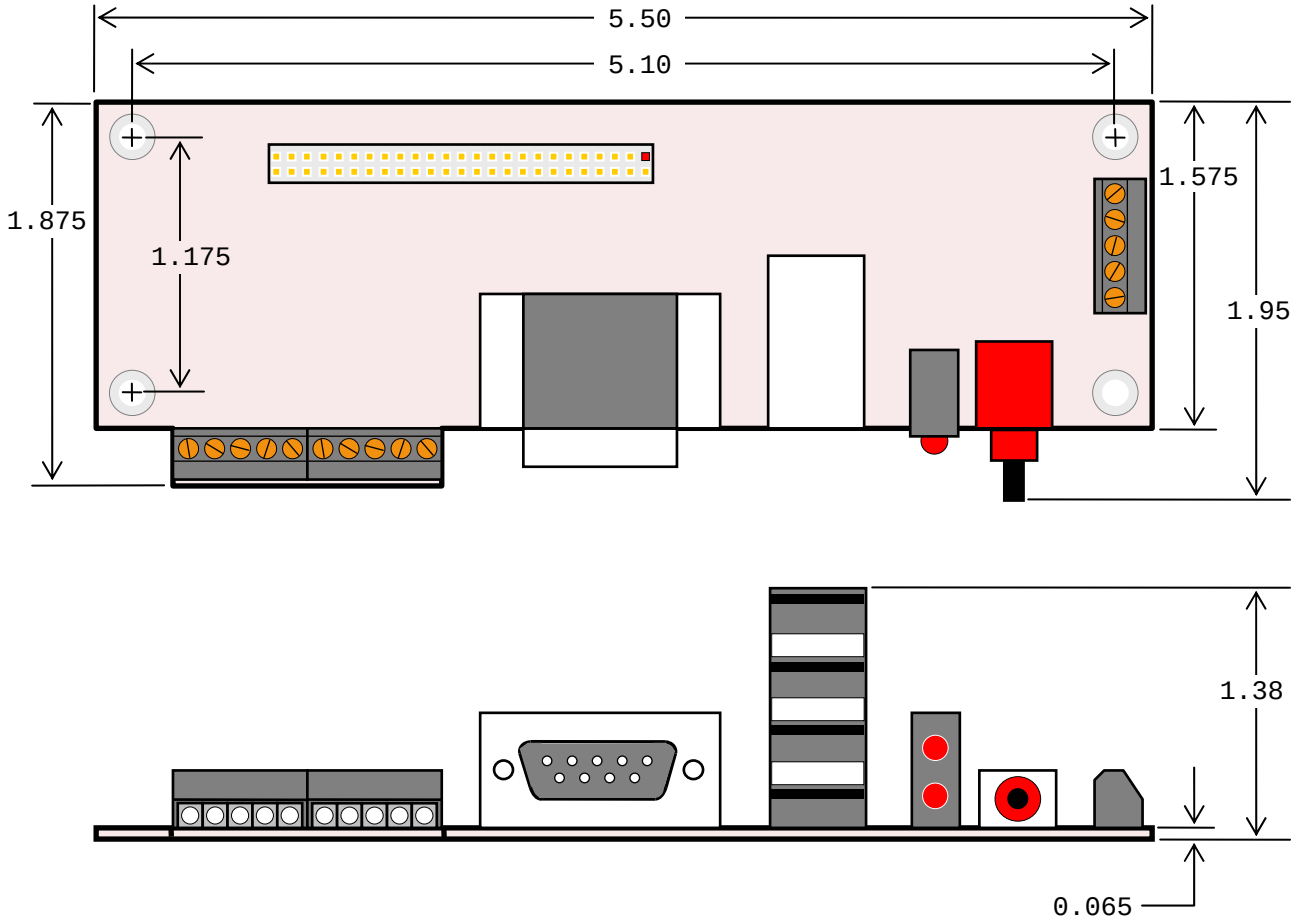


Figure 6. CBL/CBR-5010 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The EPM-5 uses pass-through PC/104 and PC/104-*Plus* connectors so that expansion modules can be added to the top or bottom of the stack. PC/104 (ISA) modules must not be positioned between the EPM-5 and any PC/104-*Plus* (PCI) modules on the stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Standoffs are secured to the top circuit board using four pan head screws. See page 13 for dimensional details. Standoffs and screws are available as part number VL-HDW-101.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack. Use caution when using the extractor tool not to damage any board components.

STACK ARRANGEMENT EXAMPLE

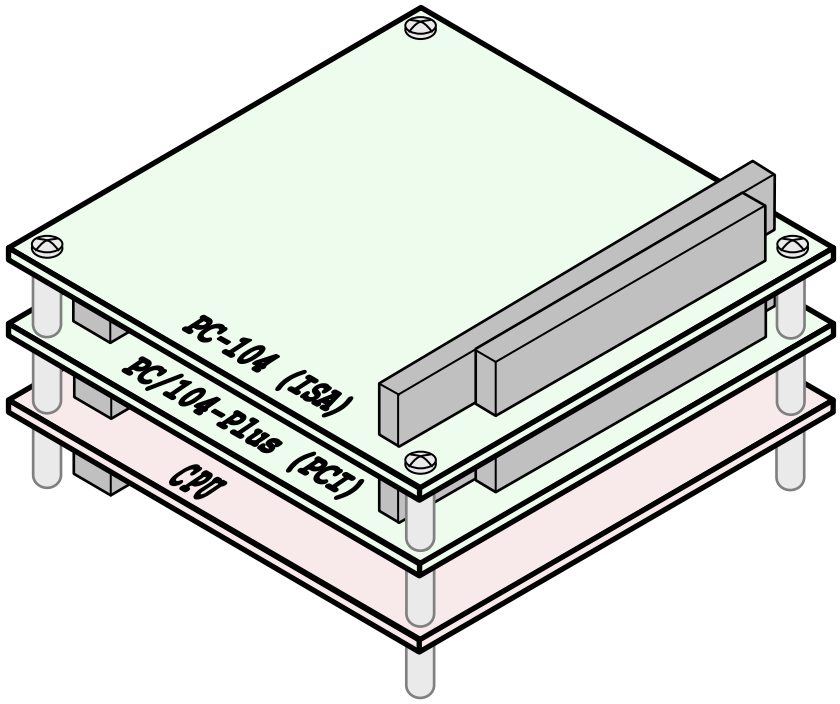


Figure 7. Stack Arrangement Example

External Connectors

EPM-5 Connector Locations – Top

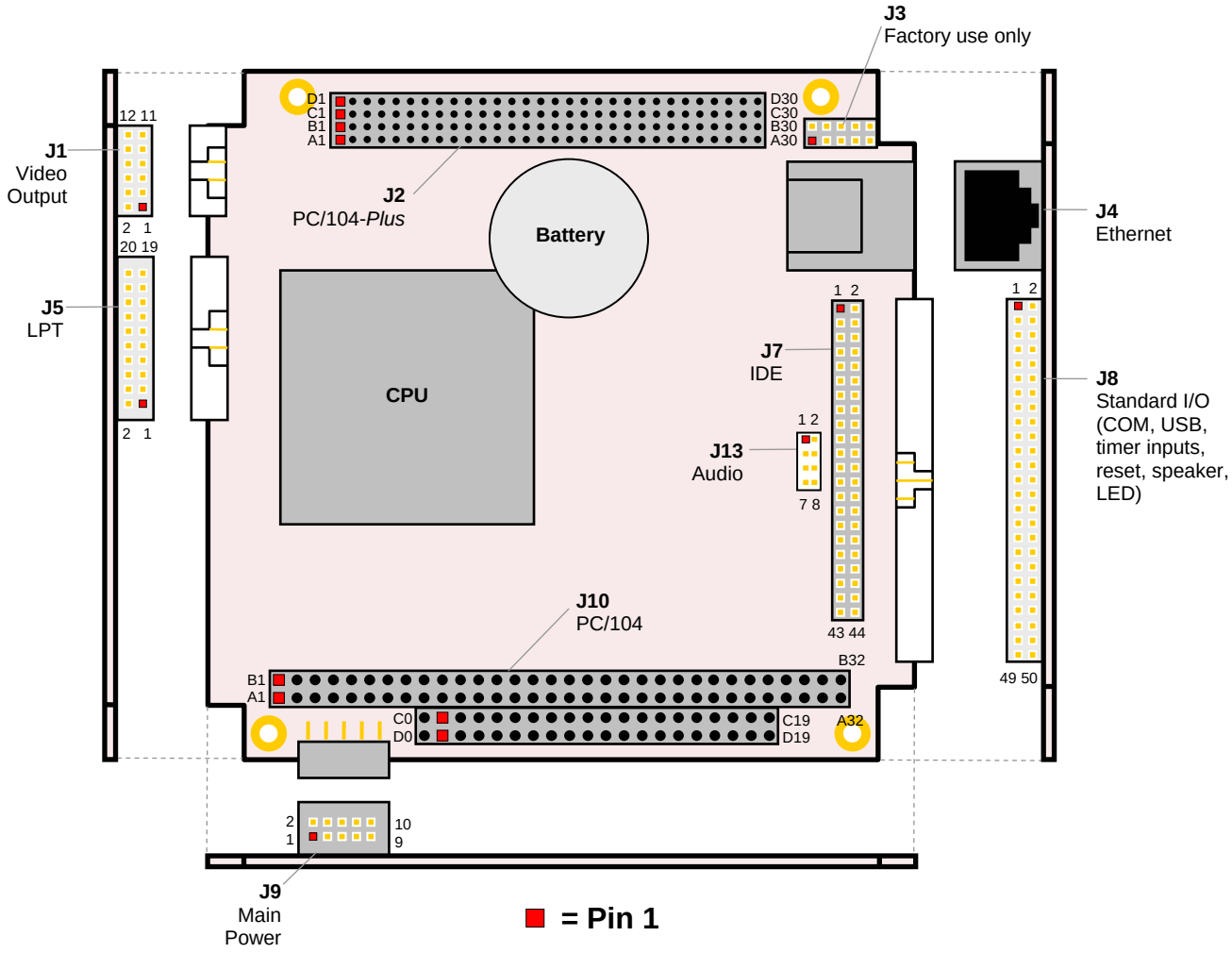


Figure 8. Connector Locations (Top)

(Not to scale.)

EPM-5 CONNECTOR LOCATIONS – BOTTOM

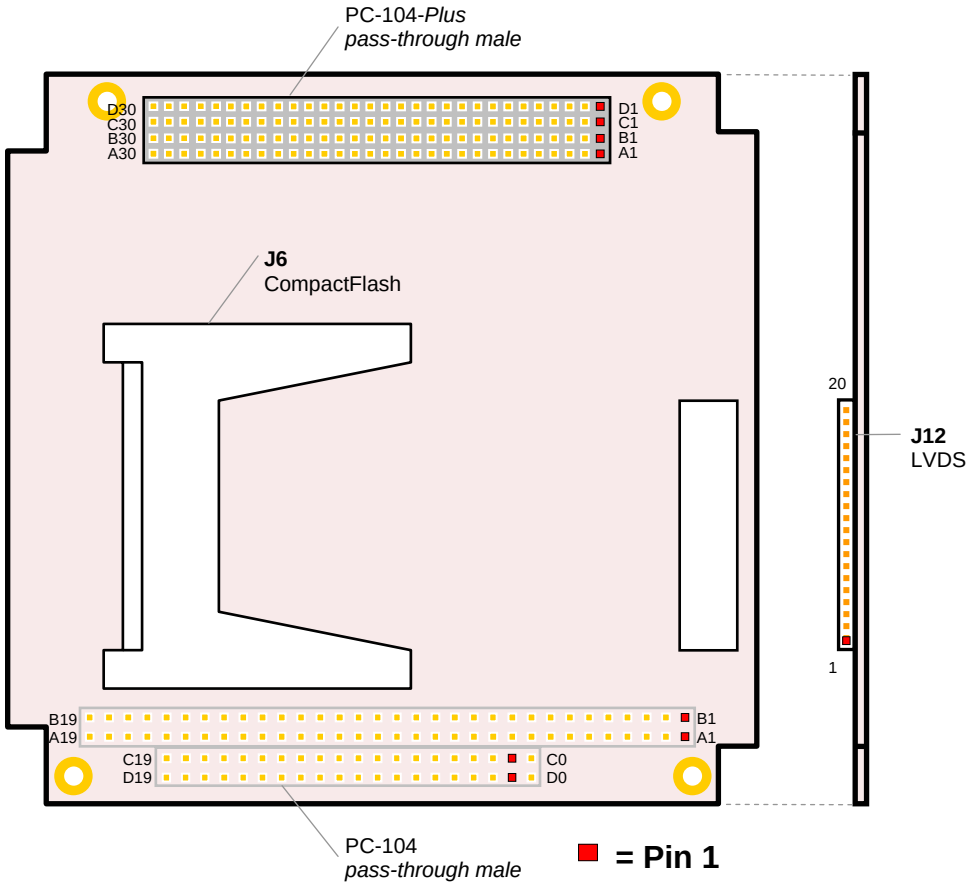


Figure 9. Connector Locations (Bottom)

(Not to scale.)

EPM-5 CONNECTOR FUNCTIONS AND INTERFACE CABLES

Table 1 provides information about the function, mating connectors, and transition cables for EPM-5 connectors. Page numbers indicate where a detailed pinout or further information is available.

Note: Adapter cables for the EPM-5 are available in RoHS compliant and RoHS noncompliant versions (see "RoHS Compliance"). Compliance or noncompliance is indicated by the part number prefix. "CBR" indicates RoHS compliance. "CBL" indicates RoHS noncompliance. For applications that require RoHS compliance, use only the RoHS compliant ("CBR" version) cables.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Pin 1 Location[1] x coord.	Pin 1 Location[1] y coord.	Page
J1	Video Output	FCI 89361-712 or FCI 89947-712	CBL-1201 or CBR-1201	1' 12-pin 2mm latching / 15-pin HD D-Sub VGA	-0.191	2.795	32
J2	PC/104-*Plus*	AMP 1375799-1	—	—	0.450	3.139	15
J3	PLD Reprogram-ming Port	—	—	—	2.795	3.125	—
J4	Ethernet	RJ-45	—	—	3.000	2.545	36
J5	LPT port	FCI 89947-720	CBL-2003 or CBR-2003	1' 20-pin 2mm latching IDC / 25-pin F D-Sub	-0.191	1.825	31
J6	CompactFlash	Type I or Type II CompactFlash	—	—	2.996	0.743	—
J7	IDE Hard Drive Channel 1	FCI 89947-144	CBL-4406 or CBR-4406[2]	1' 44-pin 2mm latching / two 44-pin 2mm	3.153	2.227	27
J8	COM ports, USB ports, DB-9, timer inputs, push-button reset, PC speaker, LED	FCI 89361-350LF	CBL-5009A or CBR-5009A	50-pin standard I/O cable to breakout board CBL/CBR-5010	3.340	2.270	29
J9	Main Power Input	Berg 69176-010 (housing) + Berg 47715-000 (pins)	CBL-1008 or CBR-1008	Interface from standard ATX power supply	0.275	-0.075	22
J10	PC/104	AMP 1375795-2	—	—	0.050	0.200	15
J11	Process JTAG DBUG	2mm	—	—	1.275	3.515	—
J12	LVDS	Molex 51146-2000 (housing) Molex 50641-8041 (pins)	CBL-2010 or CBR-2010; CBL-2011 or CBR-2011	18-bit TFT FPD using 20-pin Hirose conn. or 18-bit TFT FPD using 20-pin JAE conn.	-0.050	1.640	33
J13	Audio	FCI 89947-708LF or FCI 89361-708LF	CBL-0803 or CBR-0803	12" latching 8-pin 2mm to two 3.5mm stereo audio	2.769	1.580	37

1. The PCB Origin is the mounting hole to the lower left, as shown in Figures 8.
2. CBL/CBR-4405 44-pin to 40-pin adapter required to connect to 3.5-inch IDE drives with 40-pin connectors.

CONNECTOR LOCATIONS – CBL/CBR-5010

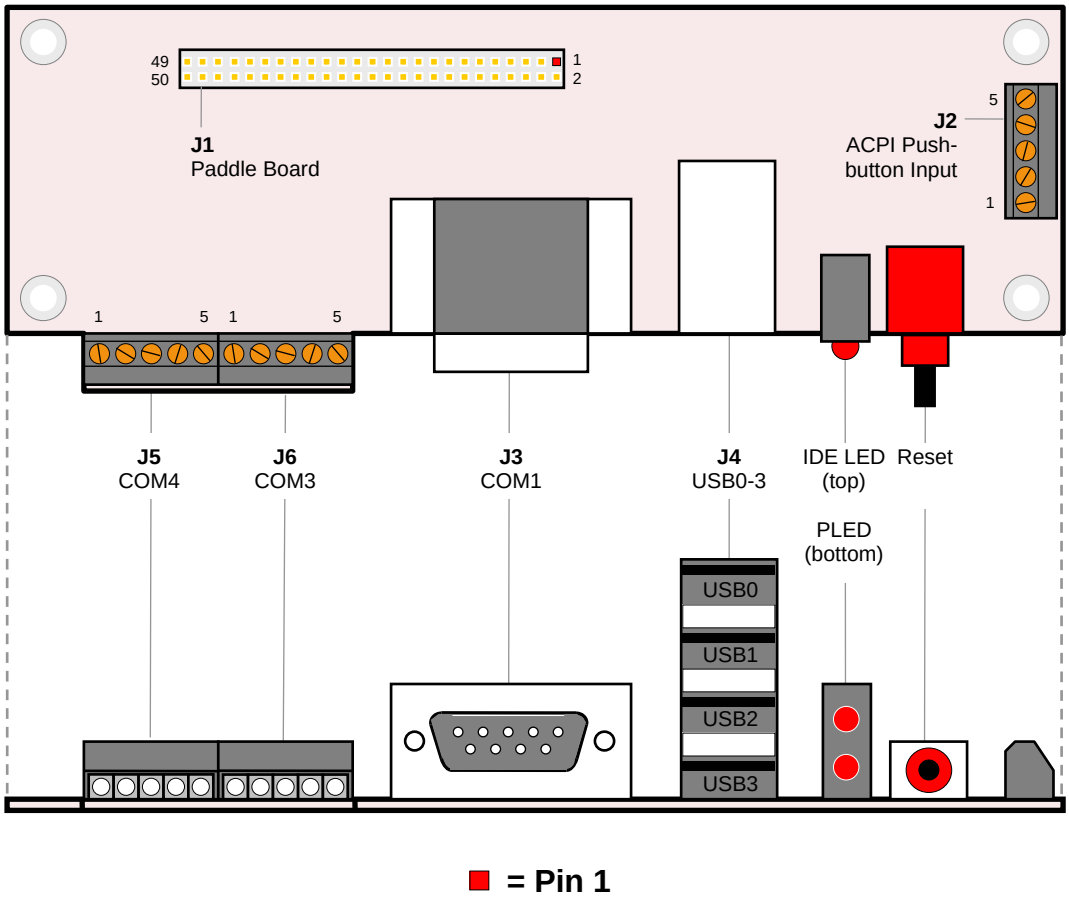


Figure 10. CBL/CBR-5010 Connector Locations

(Not to scale.)

CBL/CBR-5010 CONNECTOR FUNCTIONS AND MATING CONNECTORS

Table 2: CBL/CBR-5010 Connector Functions and Interface Cables

Connector	Function	PCB Connector	Description
J1	High Density Connector	FCI 98414-F06-50ULF	2mm, 50-pin, keyed, latching header
J2	ACPI Pushbutton Input	Conta-Clip 10250.4	5-pin screw terminal
J3	COM1	Kycon K42-E9P/P-A4N	DB-9 male
J4	USB 0-3	USB Type A	USB Type A
J5	COM4	Conta-Clip 10250.4	5-pin screw terminal
J6	COM3	Conta-Clip 10250.4	5-pin screw terminal

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION

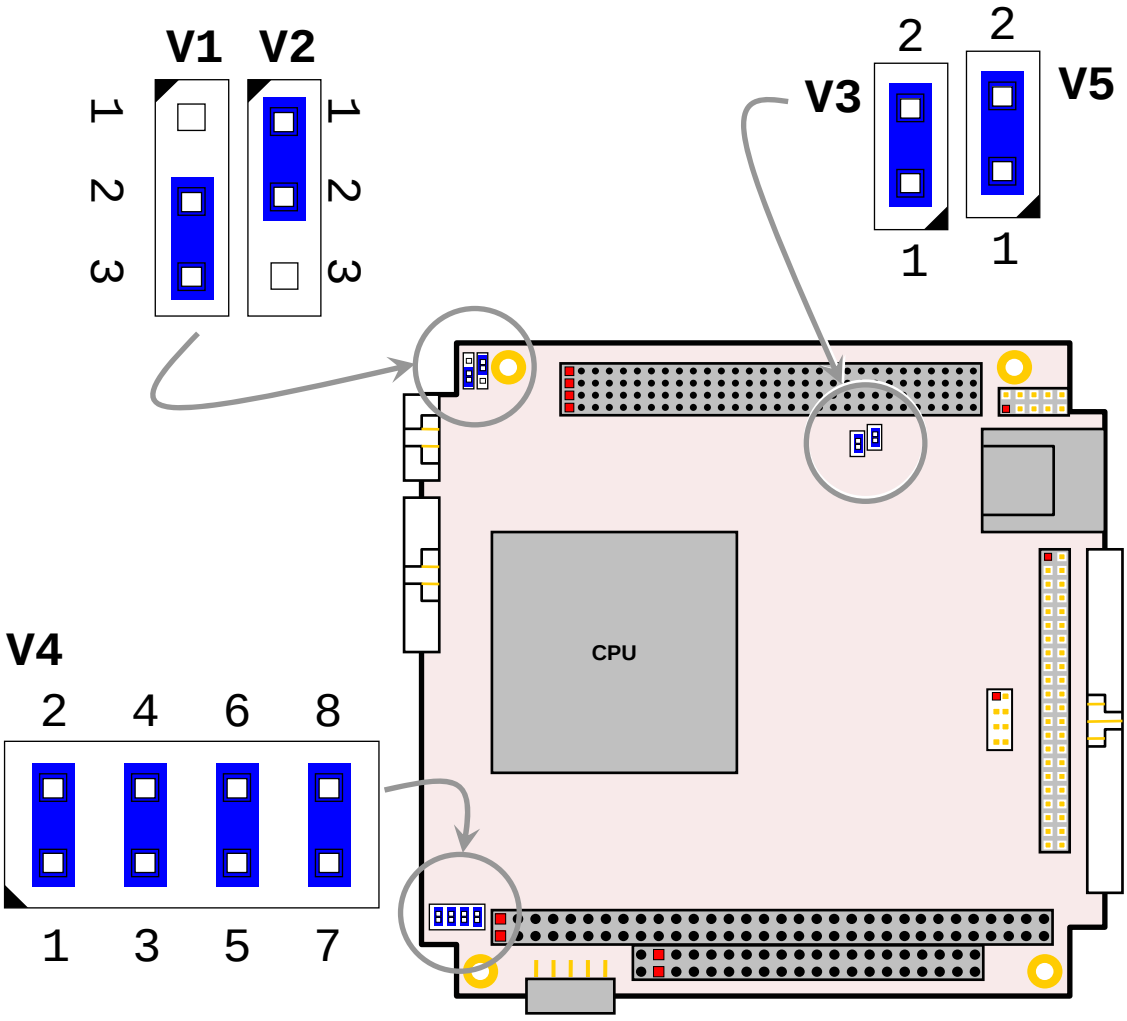
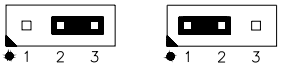
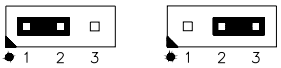


Figure 11. Jumper Block Locations

JUMPER SUMMARY

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1	**Video Display Jumper** Analog Video LVDS  	Analog Video	—
V2	**Battery Power Jumper** Standard Operation Erase CMOS  ***Warning:*** *Use care when handling the EPM-5 not to short the V2 pins accidentally, which may cause CMOS to revert to factory settings.*	Standard Operation	24
V3[1-2]	**COM3 RS-422/485 Termination** In – Line A and B terminated with 127 Ohms Out – No termination **Note:** Places terminating resistor across COM3 RS-485 TXRX+/TXRX- or RS-422 RX+/RX- differential pair.	In	27
V5[1-2]	**COM4 RS-422/485 Termination** In – Line A and B terminated with 127 Ohms Out – No termination **Note:** Places terminating resistor across COM4 RS-485 TXRX+/TXRX- or RS-422 RX+/RX- differential pair.	In	27
V4[1-2]	**SDMASTER** In – Compact Flash Master Device Out – Compact Flash Slave Device	In	–
V4[3-4]	**Video BIOS Selector** In – Primary Video BIOS selected Out – Secondary Video BIOS selected ***Note:*** *The secondary Video BIOS is field-upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/pumasupport.asp for further information*	In	32
V4[5-6]	**System BIOS Selector** In – Runtime system BIOS selected Out – Master system BIOS selected ***Note:*** *The Runtime System BIOS is field upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/pumasupport.asp for further information.*	In	–
V4[7-8]	**ACPI Pushbutton Enable** In – ACPI pushbutton disabled. Out – ACPI pushbutton enabled.	In	25

Power Supply

POWER CONNECTORS

Main power is applied to the EPM-5 through a 10-pin polarized connector, with mating connector Berg 69176-010 (Housing) + Berg 47715-000 (Pins). See the table below for connector pinout and page 16 for location information.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5VDC pins and all ground pins to prevent excess voltage drop. Some manufacturers include a pin-1 indicator on the crimp housing that corresponds to pin-10 of the pinout shown in Figure 12.

Table 4: Main Power Connector Pinout

J9 Pin	Signal Name	Description
1	GND	Ground
2	+5VDC	Power Input
3	GND	Ground
4	+12VDC	Power Input
5	GND	Ground
6	-12VDC	Power Input
7	+3.3VDC	Power Input
8	+5VDC	Power Input
9	GND	Ground
10	+5VDC	Power Input

Figure 12 shows the VersaLogic standard pin numbering for this type of 10-pin power connector and the corresponding mating connector.

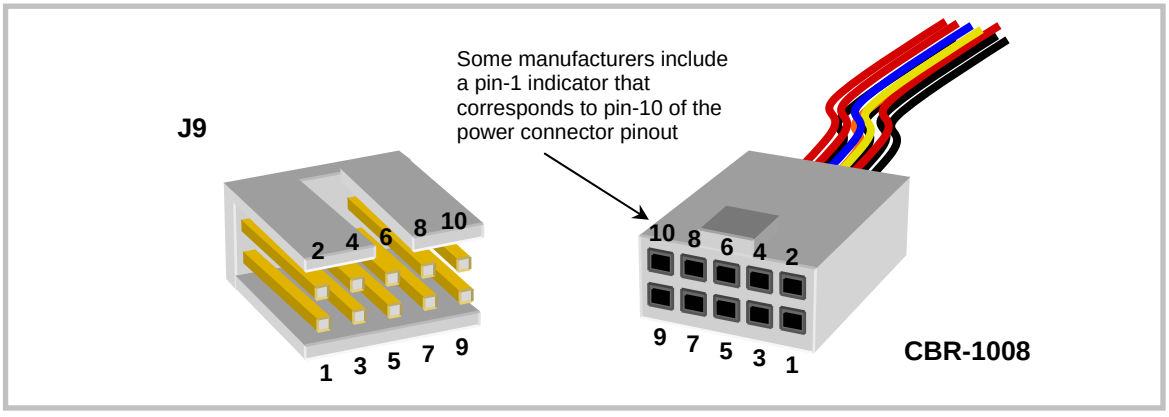


Figure 12. J9 and CBR-1008 Pin Numbering

Note: The +3.3VDC, +12VDC and -12VDC inputs are required only for expansion modules that require these voltages.

POWER REQUIREMENTS

The EPM-5 requires only +5 volts (±5%) for proper operation. The voltage required for the RS-232 ports is generated with an on-board DC/DC converter. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the EPM-5 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 3.0V, contact the factory for a replacement (part number T-HB3/0-1). The life expectancy under normal use is approximately 10 years.

CPU

The Geode GX 500 microcontroller has a 32-bit, low-voltage AMD x86 microprocessor at its core. The maximum clock rate is 366 MHz actual, with 500 MHz performance. The CPU on the extended temperature “h” version is clocked down to 333 MHz actual. The GX 500 features 32 kb of level 1 cache, DDR SDRAM support, and an integrated display controller. The CPU has a typical power consumption of 1.1W.

System RAM

MEMORY

The EPM-5 has 256MB of soldered-on DDR SDRAM board with the following characteristics:

- Storage Capacity 256 MB
- Voltage 2.5V
- Type Unbuffered PC2100 (DDR266) or PC2700 (DDR333)

CMOS RAM

CLEARING CMOS RAM

You can move the V2 jumper to position [2-3] for a minimum of three seconds to erase the contents of the CMOS RAM and the Real-Time Clock. When clearing CMOS RAM: 1) Power off the EPM-5. 2) Install the jumper on V2[2-3] and leave it for four seconds. 3) Move the jumper to back to V2[1-2]. 4) Power on the EPM-5.

CMOS Setup Defaults

The EPM-5 permits users to modify CMOS Setup defaults. This allows the system to boot up with user-defined settings from cleared or corrupted CMOS RAM, battery failure or battery-less operation. All CMOS setup defaults can be changed, except the time and date. CMOS Setup defaults can be updated with the BIOS Update Utility. See the General BIOS Information page for details.

Warning! If CMOS Setup default settings make the system unbootable and prevent the user from entering CMOS Setup, the EPM-5 needs to be serviced by the factory.

DEFAULT CMOS RAM SETUP VALUES

After CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

Real Time Clock

The EPM-5 features a year 2000-compliant, battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the Delete key during the early boot cycle) can be used to set the time and date of the real time clock.

ACPI Power Management

The EPM-5 supports the Advanced Configuration and Power Interface (ACPI) "S3 Sleeping State," also known as "standby" or "suspend to RAM" mode. Wakeup is accomplished via a TTL-level input or pushbutton (or relay attached to the pushbutton interface). Power consumption in standby mode is under 1 watt. Wakeup typically occurs in 1 to 6 seconds.

Standby mode functionality has been tested under Windows XP and Windows XP Embedded.

Also see the Power Management Control Block Diagram on page 4.

THE S3 SLEEPING STATE

The ACPI Specification defines the S3 sleeping state as a low wake latency sleeping state where all system context is lost except system memory. CPU, cache, and chipset context are lost in this state. The hardware maintains memory context and restores some CPU configuration context. Control starts from the processor's reset vector after the wake event.

Since the state of the operating system and all applications (including open documents) is sustained in main memory, the system can resume work exactly where it left off. The contents of main memory when the computer wakes from standby are the same as when it was put into standby.

SETUP

To set up the EPM-5 to use ACPI power management:

1. Verify that the CMOS Setup ACPI 1.0 setting is set to Enabled. This is the default setting.
2. If you plan to use a pushbutton or relay for wakeup, remove the jumper from jumper block V4[7-8]. Removing this jumper enables the ACPI pushbutton interface.
3. If you plan to use a pushbutton or relay for wakeup, attach the switch contacts to pins 3 and 4 of connector J2 on the CBL/CBR-5010 utility board. Pin 3 is ground, and pin 4 is the pushbutton input. (If you are not using CBL/CBR-5010, the pushbutton input is pin 40 of connector J8 on the EPM-5 motherboard.)
4. Install the most current drivers for all system devices. If a driver is not installed correctly, an exclamation point will appear before the device name in Device Manager. Incorrectly installed or older drivers may prevent the system from entering standby mode.

ENTERING STANDBY MODE

Standby mode can be entered through the operating system (by configuring the standby settings in Power Options Properties) or programmatically, through a function call or the execution of a shutdown utility. The Microsoft Windows utility DUMPPO.EXE can be used to set up and fine tune ACPI power states.

SetSystemPowerState Function

The “Power Management Reference” in the MSDN Library (http://msdn.microsoft.com/library/default.asp) contains complete information on the API available for power control under Windows. The “Power Management Functions” section provides complete information on the use of the API.

The function used to set the system power state is SetSystemPowerState. This function suspends the system by shutting power down. Depending on the *ForceFlag* parameter, the function either suspends operation immediately or requests permission from all applications and device drivers before doing so.

```
BOOL SetSystemPowerState(
  BOOL fSuspend,
  BOOL fForce
);
```

Parameters:

fSuspend

[in] If this parameter is TRUE, the system is suspended. If the parameter is FALSE, the system hibernates. This parameter is ignored in Windows Me/98/95.

fForce

[in] If this parameter is TRUE, the function broadcasts a PBT_APMSUSPEND event to each application and driver, then immediately suspends operation. If the parameter is FALSE, the function broadcasts a PBT_APMQUERYSUSPEND event to each application to request permission to suspend operation.

WAKEUP

A pushbutton or relay can be attached to connector J2 on the CBL/CBR-5010 utility board. Pin 3 is ground, and pin 4 (or pin 40 of motherboard utility connector J8) is the pushbutton input. A 3.3V or 5V TTL signal can also drive pin 4. This circuit on the EPM-5 motherboard has a 10k pull-up resistor.

Serial Ports

The EPM-5 features three on-board 16550-based serial channels located at standard PC I/O addresses. Connector J8 provides interfaces to the COM ports. See Table 6 on page 18 for COM port signal and pinout information.

COM1 is an RS-232 (115.2K baud) serial port. COM3 and COM4 can be operated in RS-422 or RS-485 modes. Additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 460K baud.

Interrupt assignment for each COM port is handled in CMOS Setup, and each port can be independently enabled or disabled.

Note: If a COM port is disabled in CMOS Setup, its I/O address space is available to the PC/104 (ISA) bus.

All serial ports are protected against ESD damage. This protection exceeds the 15KV human body model.

COM Port Configuration

There is no configuration jumper for COM1 because it operates only in RS-232 mode.

Jumper block V3 and V5 are for termination of the RS-422/485 differential pairs. See the Jumper Summary on page 21 for details on termination configuration.

COM3 and COM4 RS-485 Mode Line Driver Control

The TxD+/TxD– differential line driver can be turned on and off by manipulating the RS-485/422 Transmit/Receive Control Register. Refer to page 44 for more information.

The following code example shows how the BIOS initializes COM3 and COM4 to RS-422 mode:

```
; set up 485/422 register in pld
mov     dx, 1dah    ; IO port in PLD
mov     al, 33h     ; initialize RS-422/485 line drivers to RS-422 mode
out     dx, al
```

IDE Hard Drive / CD-ROM Interfaces

The IDE interface is available to connect up to two IDE devices, such as hard disks, CD-ROM drives, or CompactFlash. Connector J7 is the primary IDE controller with a 44-pin 2 mm latching connector. Use CMOS setup to specify the drive parameters of the drive. If you use the on-board CompactFlash device, only one other IDE device can be connected to the IDE controller.

Cable length must be 18" or less to maintain proper signal integrity.

This interface supplies power to 2.5" IDE drives. If you are connecting a 3.5" drive to the interface (using the CBL/CBR-4405 44-pin to 40-pin IDE adapter), you must supply external power to the drive. The power cable attached to a 3.5" drive must be properly grounded so that motor current is not returned via the grounds in the data cable.

Table 5: J7 IDE Hard Drive Connector Pinout

Pin	Signal Name	Function
1	Reset-	Reset signal from CPU
2	Ground	Ground
3	DD7	Data bus bit 7
4	DD8	Data bus bit 8
5	DD6	Data bus bit 6
6	DD9	Data bus bit 9
7	DD5	Data bus bit 5
8	DD10	Data bus bit 10
9	DD4	Data bus bit 4
10	DD11	Data bus bit 11
11	DD3	Data bus bit 3
12	DD12	Data bus bit 12
13	DD2	Data bus bit 2
14	DD13	Data bus bit 13
15	DD1	Data bus bit 1
16	DD14	Data bus bit 14
17	DD0	Data bus bit 0
18	DD15	Data bus bit 15
19	Ground	Ground
20	NC	Key
21	PDMARQ	DMA request
22	Ground	Ground

Pin	Signal Name	Function
23	DIOW	I/O write
24	Ground	Ground
25	DIOR	I/O read
26	Ground	Ground
27	IORDY	I/O ready
28	CSEL	Cable select
29	DMACK-	DMA acknowledge
30	Ground	Ground
31	INTRQ	Interrupt request
32	NC	No connection
33	DA1	Device address bit 1
34	CBLID-	Cable type identifier
35	DA0	Device address bit 0
36	DA2	Device address bit 2
37	CS0	Chip select 0
38	CS1	Chip select 1
39	DASP-	LED
40	Ground	Ground
41	Power	+5.0 V
42	Power	+5.0 V
43	Ground	Ground
44	NC	No connection

J8 Utility Connector

The J8 50-pin utility connector incorporates the COM ports, USB ports, LEDs, speaker, and the reset button. Table 6 illustrates the function of each pin and the pinout assignments to connectors on the CBL/CBR-5010 breakout board.

Table 6: J8 Utility Connector Pinout

J8 Pin	External Connector	Pin	Signal	
1	**COM1**	1	Data Carrier Detect	
2	**J3**	6	Data Set Ready	
3		2	Receive Data	
4		7	Request to Send	
5		3	Transmit Data	
6		8	Clear to Send	
7		4	Data Terminal Ready	
8		9	Ring Indicator	
9		5	Ground	
10		–	Ground	
	COM3		**RS-422**	**RS-485**
11	**J6**	5	TxD+	(note)
12		4	TxD–	(note)
13		1	Ground	Ground
14		3	RxD+	TxD/RxD+
15		2	RxD–	TxD/RxD–
16		–	Ground	Ground
	COM4		**RS-422**	**RS-485**
17	**J5**	5	TxD+	(note)
18		4	TxD–	(note)
19		1	Ground	Ground
20		3	RxD+	TxD/RxD+
21		2	RxD–	TxD/RxD–
22		–	Ground	Ground
23	**USB0**	T4	Ground	
24	**J4**	T1	+5V (Protected)	
25		T3	Channel 0 Data +	
26		T2	Channel 0 Data -	

J8 Pin	External Connector	Pin	Signal
27	**USB1**	TM4	Ground
28	**J4**	TM1	+5V (Protected)
29		TM3	Channel 1 Data +
30		TM2	Channel 1 Data -
31	**USB2**	BM4	Ground
32	**J4**	BM1	+5V (Protected)
33		BM3	Channel 2 Data +
34		BM2	Channel 2 Data -
35	**USB3**	B4	Ground
36	**J4**	B1	+5V (Protected)
37		B3	Channel 3 Data +
38		B2	Channel 3 Data -
39	**ACPI Push-**	3	Ground
40	**button J2**	4	EIRQ1
41		–	reserved
42		–	reserved
43	**PROG LED**	1	+5V (Protected)
44	**D1**	3	Programmable LED
45	**IDE LED**	2	+5V (Protected)
46	**D1**	4	IDE LED
47	**Speaker**	–	+5V (Protected)
48	**S1**	SP1	Speaker Drive
49	**PBRESET**	1	Ground
50	**J2**	2	Pushbutton Reset

Note: Do not connect to these pins in RS-485 mode.

USB INTERFACE

Connector J8 includes interfaces for four USB ports. The USB interface on the EPM-5 is UHCI (Universal Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible, which provides a common industry software/hardware interface. There are four USB connectors on the CBL/CBR-5010 breakout board.

BIOS Configuration

The USB controller can be enabled or disabled in the CMOS setup. The USB controller uses PCI interrupt “INTD#”. The CMOS setup screen is used to select the IRQ line routed to each PCI interrupt line.

PROGRAMMABLE LED

Connector J8 includes an output signal for a software controlled LED. Connect the cathode of the LED to J8 pin 44; connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the CBL/CBR-5010 breakout board.

To turn the LED on and off, set or clear bit D7 in I/O port 1D0h. When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn the LED on and off. Refer to page 41 for further information:

LED On

```
MOV    DX,1D0H
IN     AL,DX
OR     AL,80H
OUT    DX,AL
```

LED Off

```
MOV    DX,1D0H
IN     AL,DX
AND    AL,7FH
OUT    DX,AL
```

Note: The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code. The BIOS also flashes the LED in sync with “Beep Codes” when an error occurs.

IDE LED

Connector J8 includes an output signal for an IDE Activity LED. Connect the cathode of the LED to J8 pin 46, and connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. An IDE LED is provided on the CBL/CBR-5010 board.

INTERNAL SPEAKER

Connector J8 includes a speaker output signal at pin 48. The CBL/CBR-5010 breakout board provides a Piezo electric speaker.

PUSH-BUTTON RESET

Connector J8 includes an input for a push-button reset switch. Shorting J9 pin 50 to ground causes the EPM-5 to reboot. This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Parallel Port

The EPM-5 includes a standard bi-directional/EPP/ECP compatible LPT port which resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via CMOS Setup. The LPT mode is also set via CMOS Setup.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 7: LPT1 Parallel Port Pinout

J5 Pin	Centronics Signal	Signal Direction
1	Strobe	Out
2	Auto feed	Out
3	Data bit 1	In/Out
4	Printer error	In
5	Data bit 2	In/Out
6	Reset	Out
7	Data bit 3	In/Out
8	Select input	Out
9	Data bit 4	In/Out
10	Data bit 5	In/Out
11	Data bit 6	In/Out
12	Data bit 7	In/Out
13	Data bit 8	In/Out
14	Ground	—
15	Acknowledge	In
16	Ground	—
17	Port Busy	In
18	Ground	—
19	Paper End	In
20	Select	In

Video Interface

An on-board video controller integrated into the chipset provides high performance video output for the EPM-5. (The EPM-5 can also be operated without video card attached. See “Console Redirection.”)

CONFIGURATION

The EPM-5 uses a shared-memory architecture. This allows the video controller to use 16 Mega-bytes of system DRAM for video RAM.

The EPM-5 supports two types of video output, SVGA and LVDS Flat Panel Display.

VIDEO BIOS SELECTION

Jumper V4[3-4] can be removed to allow the system to boot off of the Secondary Video BIOS. Unlike the Primary Video BIOS, the Secondary Video BIOS can be reprogrammed in the field.

SVGA OUTPUT CONNECTOR

See the *Connector Location Diagram* on page 16 for connector location information. An adapter cable, part number CBL/CBR-1201, is available to translate J1 into a standard 15-pin D-Sub SVGA connector.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 8: Video Output Pinout

J1 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	CRED	Red video	1
3	GND	Ground	7
4	CGRN	Green video	2
5	GND	Ground	8
6	CBLU	Blue video	3
7	GND	Ground	5
8	CHSYNC	Horizontal Sync	13
9	GND	Ground	10
10	CVSYNC	Vertical Sync	14
11	–	pulled high	–
12	–	pulled high	–

LVDS Flat Panel Display Connector

The integrated LVDS Flat Panel Display in the EPM-5 is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the 4 differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 85 MHz.

The 3.3V power provided to pins 19 and 20 of J12 is protected by a 1 Amp fuse.

See the *Connector Location Diagram* on page 16 for connector location information.

Table 9: LVDS Flat Panel Display Pinout

J12 Pin	Signal Name	Function
1	GND	Ground
2	NC	No Connection
3	LVDSA3	Diff. Data 3 (+)
4	LVDSA3#	Diff. Data 3 (–)
5	GND	Ground
6	LVFSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (–)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (–)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (–)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (–)
17	GND	Ground
18	GND	Ground
19	+3.3V	Protected Power Supply
20	+3.3V	Protected Power Supply

COMPATIBLE LVDS PANEL DISPLAYS

The following list of flat panel displays is reported to work properly with the integrated graphics video controller chip used on the EPM-5.

Table 10: Compatible Flat Panel Displays

Manufacture	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4”	800 x 600 18-bit	LVDS	TFT
Sharp	LQ121S1LG411	12.1”	800 x 600 18-bit	LVDS	TFT
eVision Displays*	xxx141X01 series	14.1”	1024 x 768 18-bit	LVDS	TFT

* Compatible with DOS or Windows Generic VGA driver, but not the GX Windows driver.

CONSOLE REDIRECTION

The EPM-5 can be operated without using the onboard video output by redirecting the console to COM1. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

In the Features Configuration screen, there is an option to control console redirection. This option can be set to Auto or Redirect. When set to Auto, the console will not be redirected to COM1. When set to Redirect, the console will be directed to COM1.

Notes on console redirection:

- When console redirection is enabled, you can access CMOS Setup by typing Ctrl-C.
- The decision to redirect the console is made early in BIOS execution, and cannot be changed later.
- The redirected console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control.
- The default console redirection setting is "Auto". The defaults can be reloaded without entering BIOS setup by discharging CMOS contents (consult the reference manual for instructions).

Null Modem

The following diagram illustrates a typical DB9 to DB9 RS-232 null modem adapter.

```
System 1    <-->  System 2
Name  Pin         Pin   Name
-------------------------------------
TX    3     <-->  2     RX
RX    2     <-->  3     TX
RTS   7     <-->  1     DCD
CTS   8
DSR   6     <-->  4     DTR
DCD   1     <-->  7     RTS
                  8     CTS
DTR   4     <-->  6     DSR
```

Pins 7 and 8 are shorted together on each connector. Unlisted pins have no connection.

Ethernet Interface

The EPM-5 features an on-board Ethernet controller. This controller is the Intel 82551ER Fast Ethernet controller. While this controller is not NE2000-compatible, it is widely supported. Drivers are readily available to support a variety of operating systems. See VersaLogic website for latest OS support.

BIOS Configuration

The Ethernet interface (J4) uses PCI interrupt "INTA#". The CMOS setup screen is used to select the IRQ line routed to each PCI interrupt line.

Status LED

The EPM-5 includes an on-board, two-colored LED to provide an indication of the Ethernet status as follows:

Green LED (Link)

- ON — Active Ethernet cable plugged in
- OFF — Active cable not plugged in or cable not plugged into active hub

Yellow LED (Activity)

- ON — Activity detected on cable
- OFF — No Activity detected on cable

Ethernet Connector

A board-mounted RJ-45 connector is provided to make connection with a Category 5 Ethernet cable. The 82551ER Ethernet controller autodetects 10BaseT/100Base-TX connection speed. The interface uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Audio

The audio interface on the EPM-5 is implemented using the Analog Devices AD1981B Audio Codec. This interface is AC ’97 2.3 compatible. Drivers are available for most Windows-based operating systems. To obtain the most current versions, consult the EPM-5 product support page at http://www.VersaLogic.com/private/pumasupport.asp**.**

J13 provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

SOFTWARE CONFIGURATION

The audio interface uses PCI interrupt “INTB#”. CMOS Setup is used to select the IRQ line routed to INTB#.

The audio controller can be disabled within CMOS Setup.

Table 11: J13 Audio Connector

Pin	Signal Name	Function
1	LINE_OUTR	Line-Out Right
2	Ground	Ground
3	LINE_OUTL	Line-Out Left
4	Ground	Ground
5	LINE_INR	Line-In Right
6	Ground	Ground
7	LINE_INL	Line-In Left
8	Ground	Ground

CPU Temperature Monitor

A thermometer circuit constantly monitors the die temperature of the CPU. This circuit can be used to detect over-temperature conditions, which can result from fan or heat sink failure or excessive ambient temperatures, and under-temperature conditions.

The CMOS setup is used to set the temperature detection threshold. A status bit in the Special Control Register bit D5 of I/O port 1D0h, can be read to determine if the die temperature is above or below the threshold.

Contact the factory for information on clearing the status bit or reading and writing to the thermometer circuit. See page 41 for additional information.

PC/104 Expansion Bus

EPM-5 has limited support of the PC/104 bus. Most PC/104 cards will work, but be sure to check the requirements of your PC/104 card against the list below.

PC/104 I/O Support

The following I/O ranges are supported:

- 100h – 1CFh
- 1D3h – 1D9h
- 1DBh – 1EFh
- 200h – 36Fh (2E8h–2EF excluded if COM4 is enabled)
- 3E8h – 3EF (range excluded if COM3 is enabled)
- 3F7h – 47Fh (3F8h–3FF excluded if COM1 is enabled)
- 490h – 4CFh
- 4D2h – 777h
- 77Ch – AFFh

Note: Rev 5.01 boards and later support 16-bit I/O transfers. On Rev 5.00 and earlier boards, all 16-bit I/O reads and writes were converted into two 8-bit cycles (low byte, then high byte) on the PC/104 bus. The PLD code that enables 16-bit transfers can be installed on Rev 5.00 boards. See KnowledgeBase article VT1477 PLD and BIOS 5.3.104 Update Instructions. Later PLD updates are also available. To access them, search the VersaTech KnowledgeBase on the keywords "EPM-5 PLD."

PC/104 Memory Support

Memory ranges supported:

- CC000h-DBFFFh, 8-bit transfers only

IRQ Support

The following IRQs are available on the PC/104 bus:

- IRQ 3, IRQ 4, IRQ 10

Each of the three IRQs must be enabled in CMOS Setup before they can be used on the ISA bus. Because ISA IRQ sharing is not supported, make sure that any IRQ channel used for an ISA device is not used elsewhere. For example, if ISA IRQ 4 is enabled, you must use a different IRQ for COM1.

DMA Support

The current revision of the board does not support PC/104 DMA.

6 System Resources and Maps

Memory Map

The lower 1 MB memory map of the EPM-5 is arranged as shown in the following table.

Various blocks of memory space between C0000h and FFFFFh can be shadowed. The CMOS setup is used to enable or disable this feature.

Table 12: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS
DC000h	DFFFFh	Reserved
D0000h	DBFFFh	PC/104
C0000h	CFFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	System RAM

I/O Map

The following table lists the common I/O devices in the EPM-5 I/O map. User I/O devices should be added using care to avoid the devices already in the map as shown in the following table.

Table 13: On-Board I/O Devices

I/O Device	Standard I/O Addresses
Special Control Register	1D0h
Jumper and Status Register	1D2h
RS-485/422 Tx/Rx Control Register	1DAh
Reserved	1E0h
Primary Hard Drive Controller	1F0h – 1F7h
COM4 Serial Port	2E8h – 2EFh
LPT1 Parallel Port	378h – 37Fh
COM3 Serial Port	3E8h – 3EFh
COM1 Serial Port	3F8h – 3FFh

** User selectable via CMOS setup*

Note: The I/O ports occupied by on-board devices are freed up when the device is disabled in the CMOS setup.

Interrupt Configuration

The EPM-5 has the standard complement of PC type interrupts. Three non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines can be allocated as needed to PCI devices. There are no interrupt configuration jumpers. All configuration is handled through CMOS Setup.

Table 14: EPM-5 IRQ Settings

● = default setting ○ = allowed setting

Source	IRQ															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer 0	●															
Keyboard		●														
Slave PIC			●													
COM1				○	●	○		○		○	○	○				
COM3				○	○	○		○		○	○	○				
COM4				○	○	○		○		○	○	○				
Floppy							●									
RTC									●							
Mouse													●			
Math Chip														●		
Pri. IDE															●	
LPT1				○	○	○		○		○	○	○				
CPU Temp				○	○	○		○		○	○	○				
ISA IRQ3				○												
ISA IRQ4					○											
ISA IRQ10											○					
PCI INTA#						●				○	○	○				
PCI INTB#						●				○	○	○				
PCI INTC#						●				○	○	○				
PCI INTD#						○				○	○	●				

Table 15: PCI Interrupt Settings

● = default setting ○ = allowed setting

Source	PCI Interrupt			
	INTA#	INTB#	INTC#	INTD#
Ethernet	●			
Audio		●		
USB				●

Notes:

- If your design needs to use interrupt lines on the PC/104 bus, IRQ10 is recommended. (IRQ3 and IRQ4 are normally used by COM ports on the main board.) On boards prior to Rev. 5.00, PC/104 IRQ3 (B25) was bonded to PC/104 IRQ7 (B21), and PC/104 IRQ4 (B24) to PC/104 IRQ11 (D4).
- Though the EPM-5 is not equipped with a standard keyboard (IRQ1), floppy disk (IRQ6), or mouse (IRQ12), the BIOS infrastructure makes it appear they exist for DOS and older operating systems. Though these devices use USB interrupts, legacy IRQs are created via software.
- ACPI uses IRQ9. IRQ9 should not be assigned to other devices if ACPI is enabled.
- The BIOS has no devices to assign to IRQ15.

Special Control Register

SCR (READ/WRITE) 1D0h

D7	D6	D5	D4	D3	D2	D1	D0
PLED	Reserved	OVERTEMP	Reserved	Reserved	Reserved	Reserved	Reserved

Table 16: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J4 0 = Turns LED on 1 = Turns LED off
D6	Reserved	**Reserved** — This bit has no function.
D5	OVERTEMP	**Temperature Status** — Indicates CPU temperature. 0 = CPU temperature is below value set in the CMOS setup 1 = CPU temperature is above value set in the CMOS setup ***Note:*** *This bit is a read-only bit.*
D4-D0	Reserved	**Reserved** — These bits have no function.

Revision Indicator Register

REVIND (READ ONLY) 1D1h

D7	D6	D5	D4	D3	D2	D1	D0
PC4	PC3	PC2	PC1	PC0	EXT	REV1	REV0

This register is used to indicate the revision level of the EPM-5.

Table 17: Revision Indicator Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	PC	**Product Code** — These bits are hard-coded to represent the product type. The EPM-5 always reads as 00011. Other codes are reserved for future products. **PC4 PC3 PC2 PC1 PC0 Product Code** 0 0 1 0 0 EPM-5 ***Note:*** *These bits are read-only.*
D2	EXT	**Extended Temperature** — Indicates operating temperature range. 0 = Standard temperature range 1 = Extended temperature range
D1-D0	REV	**Revision Level** — These bits represent the EPM-5 circuit revision level. **REV1 REV0 Revision Level** 0 0 Initial product release, Rev 1, 2 and 3 0 1 Rev 4.xx 1 0 Rev 5.xx, 6.xx ***Note:*** *These bits are read-only.*

Jumper and Status Register

JSR (READ/WRITE) 1D2h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	VB-SEL	SB-SEL	Reserved	Reserved	Reserved	Reserved	Reserved

Table 18: Jumper and Status Register Bit Assignments

Bit	Mnemonic	Description
D7	Reserved	This bit has no function.
D6	VB-SEL	**Video BIOS Selection** — Indicates the status of jumper. 0 = Jumper out, Secondary Video BIOS selected. 1 = Jumper in, Primary Video BIOS selected. ***Note:*** *This is a read-only bit.*
D5	SB-SEL	**System BIOS Selection** — Indicates the status of jumper. 0 = Jumper out, Master System BIOS selected. 1 = Jumper in, Run Time System BIOS selected. ***Note:*** *This is a read-only bit.*
D4-D0	Reserved	**Reserved** — These bits have no function.

RS-485/422 Transmit/Receive Control Register

RS485/422 (WRITE ONLY) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	COM4TE485	COM4RE4XX	COM4TE422	Reserved	COM3TE485	COM3RE4XX	COM3TE422

Table 19: RS-485/422 Tx/Rx Register Bit Assignments

Bit	Mnemonic	Description
D7	Reserved	This bit has no function.
D6	COM4TE485	**COM4 RS-485 Transmit Enable** — Controls RS-485 Tx on COM4. 0 = Disable RS-485 transmitter on COM4. 1 = Enable RS-485 transmitter on COM4. ***Note:*** *This is a write-only bit.*
D5	COM4RE4XX	**COM4 RS-485/422 Receive Enable** — Controls RS-485/422 Rx on COM4. 0 = Disable RS-485/422 receiver on COM4. 1 = Enable RS-485/422 receiver on COM4. ***Note:*** *This is a write-only bit.*
D4	COM4TE422	**COM4 RS-422 Transmit Enable** — Controls RS-422 Tx on COM4. 0 = Disable RS-422 transmitter on COM4. 1 = Enable RS-422 transmitter on COM4. ***Note:*** *This is a write-only bit.*
D3	Reserved	**Reserved** — This bit has no function.
D2	COM3TE485	**COM3 RS-485 Transmit Enable** — Controls RS-485 Tx on COM3. 0 = Disable RS-485 transmitter on COM3. 1 = Enable RS-485 transmitter on COM3. ***Note:*** *This is a write-only bit.*
D1	COM3RE4XX	**COM3 RS-485/422 Receive Enable** — Controls RS-485/422 Rx on COM3. 0 = Disable RS-485/422 receiver on COM3. 1 = Enable RS-485/422 receiver on COM3. ***Note:*** *This is a write-only bit.*
D0	COM3TE422	**COM3 RS-422 Transmit Enable** — Controls RS-422 Tx on COM3. 0 = Disable RS-422 transmitter on COM3. 1 = Enable RS-422 transmitter on COM3. ***Note:*** *This is a write-only bit.*

Note: On the EPM-5 Rev 5.00 and earlier boards, this register was read/write. Customers using COM3 or COM4 in RS-422 or RS-485 modes should review their driver code to ensure the control register at 1DAh is used as a write-only register.

Appendix A – References

PC Chipset *GX 500 Chipset*	Advanced Micro Devices
Ethernet Controller *Intel 82551ER*	Intel Corporation
Video Controller	In chipset.
PC/104 Specification *PC/104 Resource Guide*	PC/104 Consortium
PC/104-*Plus* Specification *PC/104 Resource Guide*	VersaLogic Corporation
General PC Documentation *The Programmer's PC Sourcebook*	Microsoft Press
General PC Documentation *The Undocumented PC*	Powell's Books

Appendix B – Generated Frequencies

The following frequencies on the EPM-5 board can be measured for EMI/EMC testing.

Table 20: Generated Frequencies

Component	Frequencies	Notes
10/100 Ethernet	25 MHz	Y1 crystal, U7 82551ER chip.
RTC	32.768 kHz	Y2 crystal, U13A CS5536 chip.
System Clock	14.318 MHz	Y3 crystal, U34 MK1491-09F chip.
REF Clock	14.318 MHz	
IOAPC Clock	14.318 MHz	
PCI Clock	33.3 MHz	
USB	48 MHz	Y4 crystal, U13B CS5536 chip.
Audio	24.576 MHz	Y5 crystal, U44 AD1981B chip.
PCI Bus	33.3 MHz	Fixed frequency.
ISA Bus	8 MHz	
VCore Switching Register	1 MHz	Switching frequency.
Memory	111 MHz or 222 transfers per second	