EPMs-21 CMOS SETUP PARAMETERS

This article provides reference information and tips for setting CMOS Setup parameters on the EPMs-21 (Ocelot). Start CMOS Setup by pressing Delete during the early boot cycle. The Main menu appears first. You can scroll to other menus using the left and right arrow keys. The CMOS Setup menus are:

The basic idea when using CMOS Setup is to navigate to the menus containing fields you want to review, and change those fields as desired. When your settings are complete, navigate to the Exit menu, and select “Save Settings and Restart.” This causes the settings to be stored in nonvolatile memory in the system, and the system will reboot so that POST can configure itself with the new settings. After rebooting it may be desirable to reenter the Setup system as necessary to adjust settings as necessary.

Once the system boots, CMOS Setup cannot be entered; this is because the memory used by the BIOS configuration manager is deallocated by the system BIOS, so that it can be used by the OS when it boots. To reenter CMOS Setup after boot, simply reset the system or power off and power back on.

Note: The configurations and factory defaults described here are for EPMs-21 BIOS version 6.5.105, except where noted.

Main Menu

The Main menu displays the main system components and allows editing of the date and time.

```
+ ------------------------- -------------------------- + ------------------
- +
| System Summary                                       |Use TAB to switch
|
| ------------------------- -------------------------- |between month, day
|
| Phoenix[R] System BIOS                               |and year.  Use
digits|
| VersaLogic Version    6.5.105                        |and BKSP to change
|
| Core Version          EB(SF).005                     |field.
|
| PLD Version           3                              |
|
| PLD Flags             Standard                       |
|
| BIOS Build Date       10/01/13                       |
|
| System BIOS Size      128KB                          |
|
```

```
| CPM/CSPM/BPM Modules  P7C7, SCHUS15W, EPMS21           |
|
| StrongFrame[R] Technology, Firmbase[R] Technology      |
|
|                                                        |
|
| Processor (CPU)                                        |
|
| Intel[R] Atom[TM] CPU Z530  @ 1.60GHz                  |
|
| Processor Count       2                                |
|
|                                                        |
|
| System Memory (RAM)                                    |
|
| Low Memory (KB)       626                              |
|
| Extended Memory (KB)  1030912                          |
|
|                                                        |
|
| Real Time Clock (RTC)                                  |
|
| RTC Date              [05/24/2011]                     |
|
| RTC Time              [13:57:20]                       |
|
+ ------------------------ -------------------------- + ------------------
- +
```

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RTC Date
RTC Time

The real time clock (RTC) date is factory set to the date of the BIOS build. The date and time are editable.

Exit Menu

The Exit menu allows you to save or discard changes and exit, or restore default settings and exit.

```
+ ------------------------ -------------------------- + ------------------
- +
|                                                     |
|
| Save, Restore, and Exit Setup                       |Press ENTER to save
|
| ------------------------ -------------------------- |changes and reboot
|
| Save Settings and Restart           [Enter]         |system.
|
```

```
|                                                                  |
|
| Exit Setup Without Saving Changes    [Enter]                     |
|
|                                                                  |
|
| Reload Factory-Defaults and Restart  [Enter]                     |
|
|                                                                  |
|
| Reload Custom-Defaults and Restart   [Enter]                     |
|
|                                                                  |
|
+ ------------------------- --------------------------- + ------------------
- +
```

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You can exit CMOS Setup by selecting one of the options below. To select an option, position the cursor over the option and press Enter. Pressing Esc at any time in CMOS Setup is equivalent to "Exit Setup Without Saving Changes."

- **Save Settings and Restart:** Saves all changes made to CMOS settings and reboots the EPMs-21.
- **Exit Setup Without Saving Changes:** Does not save any changes made to CMOS settings and continues with POST as normal.
- **Reload Factory-Defaults and Restart:** Resets CMOS to factory defaults, even if there are custom defaults available. All changes made to CMOS settings during the current and previous CMOS Setup sessions will revert.
- **Reload Custom-Defaults and Restart:** Resets CMOS to custom defaults. All changes made to CMOS settings during the current and previous CMOS Setup sessions will revert. Custom defaults are programmed using the FBU utility.

Boot Menu

The Boot menu configures boot actions and devices.

```
+ ------------------------- --------------------------- + ------------------
- +
| System Boot Configuration                            |Select
initialization|
| ------------------------- --------------------------- |and boot priority
for|
|                                                      |all devices.
|
| Boot Device Prioritization (BBS)                     |
|
| 0 [IDE 0/Pri Master]                                 |Backspace deletes
|
```

```
| 1 [IDE 1/Pri Slave]                                    |selection. Space
|
| 2 [None]                                               |bar, + and - change
|
|                                                        |selections.
|
| Initialization Policy [Boot Devices Only]              |
|
|                                                        |
|
| IDE Drive Configuration                                |
|
| IDE 0 Type     [Autoconfig, LBA]                       |
|
| IDE 0 Mode     [UDMA mode (40-conductor cable)]        |
|
| IDE 1 Type     [Autoconfig, LBA]                       |
|
| IDE 1 Mode     [UDMA mode (40-conductor cable)]        |
|
|                                                        |
|
+ -------------------------- ---------------------------- + ------------------
- +
```

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Boot Device Prioritization (BBS)

Values: IDE/Pri Master/Slave, Enter BIOS Preeboot Screen, Enter BIOS Setup Screen, Reboot System, Enter BIOS Debugger, P2P Bridge card in PCIE SLT 0, P2P Bridge on P2P Bridge card in PCIE..., Intel (R) Boot Agent GE v1.3.27, All other devices, USB Floppy, USB Hard Drive 1-7, USB CDROM Drive, None

Lists the devices and activities to be performed in the order in which they appear in the list -- the BIOS boot specification (BBS). When the BIOS completes POST, it follows this list, attempting to process each item. Some items are drives, such as an IDE drive, or a USB hard disk, or CDROM.

The ordering of the drives in the BBS list controls the BIOS in several ways. First, it is the list of drives that is scanned and assigned BIOS unit numbers for DOS (0, 1, 2 for floppy-type devices, and 80h, 81h, 83h, and so on for hard drives). If a drive on the list is not plugged in or working properly, the BIOS moves on to the next drive, skipping the inoperative one. Second, once the drives in the list have been verified, POST attempts to boot from them in that order as well. Drives without bootable partitions might be configured, but skipped over in the boot phase, so that other drives on the list become candidates for booting the OS.

The BBS list also contains other boot actions, such as boot from network cards and PCI slots, as well as special BIOS boot actions. When deciding what boot action to do first and then next in succession, POST first scans all the drives in the list to verify they are present and operating properly, and then goes down the list and tries to perform the actions in order. During this boot phase, if the list item is a drive, an attempt is made to boot from the boot record of that drive. If

the list item is a device like a network card or PCI slot, an attempt is made to boot from that device. If the list item is a software item like “Enter BIOS Preboot Screen,” then it performs that action, and when that action completes, it moves on to the next item in the BBS list.

If detected, the names and serial numbers of drives connected to the board will appear after the connector number; for example: "IDE 0/Pri Master, WDC WD800BB-00JHC0."

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Initialization Policy

Values: All Devices, Boot Devices Only

Specifies the policy used to determine if device specific initialization code should be executed. Boot Devices Only prevents the initialization of devices not assigned a boot priority.

IDE x Type

Values: Autoconfig; Autoconfig, Physical; Autoconfig, LBA; Autoconfig, Phoenix; Not Installed

Selects the logical geometry translation method for the IDE drive.

IDE x Mode

Values: UDMA mode (40-conductor cable), UDMA mode (80-conductor cable), Fastest supported mode, PIO mode, Multi-word DMA mode

Selects the preferred transfer mode for the IDE drive. This applies only to the BIOS. The OS may use chipset specific drivers.

BACK TO BOOT

POST Menu

The POST menu configures power-on self-test settings.

```
+ ------------------------- --------------------------- + ------------------
- +
| POST Memory Tests                                     |Enable basic memory
|
| ------------------------- --------------------------- |confidence test
below|
| Low Memory Standard Test     [Enabled]                |1MB during POST.
|
| Low Memory Exhaustive Test   [Disabled]               |
|
| High Memory Standard Test    [Disabled]               |
|
| High Memory Exhaustive Test  [Disabled]               |
|
```

Click During Memory Test	[Enabled]
Clear Memory During Test	[Disabled]
POST Error Control	
Pause on POST Errors	[Disabled]
POST User Interface	
POST Display Messages	[Enabled]
POST Operator Prompt	[Enabled]
POST Display PCI Devices	[Enabled]
POST Debugging	
POST Slow Reboot Cycle	[Disabled]
POST Fast Reboot Cycle	[Disabled]
Device Initialization	
POST Floppy Seek	[Disabled]
POST Hard Disk Seek	[Enabled]

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POST Memory Tests

Enables or disables the following memory tests during POST:

- **Low Memory Standard Test:** Basic confidence test of memory below the 1 MB address boundary (conventional memory, or memory normally used by DOS).
- **Low Memory Exhaustive Test :** Exhaustive confidence test of memory below 1 MB.
- **High Memory Standard Test:** Basic confidence test of memory above the 1 MB address boundary.
- **High Memory Exhaustive Test:** Exhaustive confidence test of memory above 1 MB.
- **Click During Memory Test:** Audible click after each tested memory block.
- **Clear Memory During Test:** Sets all memory locations tested to 0. This is required only for some legacy DOS programs that might rely on cleared memory to operate properly.

Pause on POST Error

If enabled, causes POST to pause if an error is detected, allowing the user to review the error before continuing POST.

POST User Interface

Enables or disables the following POST messaging:

- **POST Display Messages:** Text messages displayed during POST. When disabled, POST is "quiet."
- **POST Operator Prompt:** Operator prompts if POST is configured to ask interactive questions of the user about whether to use specific features.
- **POST Display PCI Devices:** Display of PCI devices.

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POST Debugging

Enables or disables slow or fast reboot cycles for diagnostic purposes.

- **POST Slow Reboot Cycle:** The system reboots late in POST. Used to exercise system memory and peripherals without requiring a boot to an operating system.
- **POST Fast Reboot Cycle:** The system reboots repeatedly early in POST. Used to verify that the system can reboot quickly many times in succession. The system will continue to reboot after every boot until the CMOS is reset (using jumper V2[3-4]), as there is no way to enter Setup from this early point during POST.

Device Initialization

Enables or disables floppy drive or hard disk seek during POST for diagnostic purposes.

- **POST Floppy Seek:** Executes a head seek on each floppy drive connected to the system. Used to recalibrate the drive in some systems with older DOS operating systems.
- **POST Hard Disk Seek:** Executes a head seek on each hard drive connected to the system. This extends the standard test performed on each drive by requesting that the drive actually move the head.

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SIO Menu

The SIO menu configures super I/O devices, specifically the serial ports. Note that the default addresses assigned to the serial ports are not the only ones possible, but they do ensure compatibility with legacy software, especially early DOS programs that do not use the BIOS to access the ports.

The default addresses are chosen first to be at legacy locations for optimal compatibility, and second to optimize I/O space usage. There are really only four I/O addresses that can be called "legacy" (3F8, 2F8, 3E8, and 2E8, which correspond to device names COM1-4). Beyond that, compatibility with legacy software cannot be ensured.

Note: The EPMs-U1 submenu appears only if an EPMs-U1 device is attached to the EPMs-21. If two EPMs-U1 boards are attached, there will be two submenus. The number of serial ports in each submenu depends on the type of super I/O chip (SMSC SCH3114 or SCH3116) present on the EPMs-U1. The menu below shows the BIOS options for an SCH3116 SIO board).

```
+ ------------------------- --------------------------- + ------------------
- +
| BIOS Super I/O Configuration                          |
|
| ------------------------- --------------------------- |
|
|                                                       |
|
| SMSC SCH3114 Devices                                  |
|
| ------------------------- --------------------------- |
|
| IRQ Sharing                    [No Sharing]           |
|
|                                                       |
|
| Serial Port 1                  [Enabled]              |
|
|   Address                      [3F8h]                 |
|
|   IRQ                          [IRQ 4]                |
|
|   Mode                         [RS-232 (4-wire)]      |
|
| Serial Port 2                  [Enabled]              |
|
```

	Address	[2F8h]
	IRQ	[IRQ 3]
	Mode	[RS-232 (4-wire)]
Serial Port 3		[Disabled]
	Address	[3E8h]
	IRQ	[No IRQ]
	Mode	[RS-232 (4-wire)]
Serial Port 4		[Disabled]
	Address	[2E8h]
	IRQ	[No IRQ]
	Mode	[RS-232 (4-wire)]
EPMs-U1 Devices (SMSC SCH3116)		
-------------------------	-------------------------	
IRQ Sharing		[No Sharing]
Serial Port 1		[Disabled]
	Address	[200h]
	IRQ	[IRQ 4]
Serial Port 2		[Disabled]
	Address	[208h]
	IRQ	[IRQ 3]
Serial Port 3		[Disabled]
	Address	[210h]
	IRQ	[No IRQ]
	Mode	[RS-232 (4-wire)]
Serial Port 4		[Disabled]
	Address	[218h]

```
|   IRQ                          [No IRQ]                 |
|
|   Mode                         [RS-232 (4-wire)]        |
|
| Serial Port 5                  [Disabled]               |
|
|   Address                      [220h]                   |
|
|   IRQ                          [No IRQ]                 |
|
|   Mode                         [RS-232 (4-wire)]        |
|
| Serial Port 6                  [Disabled]               |
|
|   Address                      [228h]                   |
|
|   IRQ                          [No IRQ]                 |
|
|   Mode                         [RS-232 (4-wire)]        |
|
+ ------------------------- --------------------------- + -----------------
- +
```

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EPMs-21 Super I/O Devices

Serial Port 1-4

Enables or disables serial ports on the CPU board and sets port addresses and interrupts.

- **Address:** 3F8h, 2F8h, 3E8h, 2E8h, 238h, 338h
- **IRQ:** IRQ 3, IRQ 4, IRQ 5, IRQ 6, IRQ 7, No IRQ
- **Mode:** RS-232 (4-wire), RS-422, RS-485 (Auto flow ctl)

Normally, IRQs cannot be shared among devices on the ISA or LPC buses. However, SCH311x SIOs have the ability to assert a specific IRQ if two, or any, of its internal UARTs need to interrupt the CPU. The SCH311x driver checks every internal UART associated with that IRQ to see if it is the one that requested the interrupt.

Mode notes:

- RS-232 (4-wire): Only the TX, RX, CTS, and RTS signals are used. This will work for terminal communication, but not for a modem.
- RS-485 (Auto flow ctl): Data is only driven onto the RS-485 shared bus lines when the UART output FIFO contains data. If the FIFO is disabled, Auto Flow Control will not work.

EPMs-U1 Super I/O Devices

The EPMs-U1 Devices submenu is displayed only if one or two EPMs-U1 boards are attached to the EPMs-21. The number of configurable serial ports will depend on the model(s) of EPMs-U1 installed. See the EPMs-U1 Reference Manual for information on addressing considerations.

Serial Port 1-6

Enables or disables serial ports and sets port addresses and interrupts.

- **Address:**
  - **Serial Port 1:** 200h, 3F8h, 3E8h, 100h
  - **Serial Port 2:** 208h, 2F8h, 2E8h, 108h
  - **Serial Port 3:** 210h, 3F8h, 3E8h, 110h
  - **Serial Port 4:** 218h, 2F8h, 2E8h, 118h
  - **Serial Port 5:** 220h, 238h, 120h
  - **Serial Port 6:** 228h, 338h, 128h
- **IRQ:** IRQ 3, IRQ 4, IRQ 5, IRQ 7, No IRQ
- **Mode:** RS-232 (4-wire), RS-422, RS-485 (Manual flow control), RS-485 (Auto flow control)

Mode notes:

- RS-232 (4-wire): Only the TX, RX, CTS, and RTS signals are used. This will work for terminal communication, but not for a modem.
- RS-485 (Auto flow control): Data is only driven onto the RS-485 shared bus lines when the UART output FIFO contains data. If the FIFO is disabled, Auto Flow Control will not work.

IRQ Sharing

The IRQ Sharing parameter appears under each super I/O block of the SIO Menu.

Values: No Sharing, Paired Sharing, Full Sharing

Sets or disables IRQ sharing among the serial ports of a single super I/O chip. When you select Paired Sharing, two or three additional parameters appear depending on the model of SIO:

- **IRQ for Serial Ports 1, 2:** IRQ 3, IRQ 4, IRQ 5, IRQ 7, No IRQ
- **IRQ for Serial ports 3, 4:** IRQ 3, IRQ 4, IRQ 5, IRQ 7, No IRQ
- **IRQ for Serial ports 5, 6:** IRQ 3, IRQ 4, IRQ 5, IRQ 7, No IRQ

When you select Full Sharing, one additional parameters appears:

- **IRQ for all Serial Ports:** IRQ 3, IRQ 4, IRQ 5, IRQ 7, No IRQ

Selecting either Paired Sharing or Full Sharing removes the IRQ parameter from the individual Serial Ports.

Interrupts can be shared among serial ports on the same super I/O chip, but not shared among serial ports originating from different super I/O chips.

BACK TO SIO

Features Menu

The Features menu enables and disables system BIOS features and configures console redirection and CPU settings.

```
+ ------------------------- ---------------------------- + ------------------
- +
| BIOS Feature Configuration                              |Enable to
initialize |
| ------------------------- ---------------------------- |APICs and use them
in|
| Interrupt Processing          [Use APIC]                |an emulated PIC
mode.|
| MP Tables (non ACPI OSes)     [Enabled]                 |If you wish to use
|
| Quick Boot                    [Disabled]                |full-APIC mode,
this |
| ACPI                          [Enabled]                 |must be set AND
|
| POST Memory Manager           [Disabled]                |either ACPI or MP
|
| System Management BIOS        [Enabled]                 |must be enabled. DO
|
| Splash Screen                 [Disabled]                |NOT CHANGE AFTER OS
|
|                                                         |INSTALL.
|
| Console Redirection                                     |
|
| ------------------------- ---------------------------- |
|
| Use Console Assignments Below [On Remote User Detect]   |
|
| POST Console                  [COM1]                    |
|
| Preboot Console               [COM1]                    |
|
| Debugger Console              [COM1]                    |
|
|                                                         |
|
| Legacy Free Option                                      |
|
| ------------------------- ---------------------------- |
|
```

```
| Legacy-Free                    [Enabled]                |
|
| Plug-n-Play Header             [Enabled]                |
|
|                                                         |
|
| CPU Configuration                                       |
|
| ------------------------- ---------------------------- |
|
| P7 Geyserville/Speedstep       [Enabled]                |
|
| Intel VT                       [Disabled]               |
|
| Microcode Update               [Enabled]                |
|
| Core Multi-Processing          [Enabled]                |
|
+ ------------------------- ---------------------------- + ------------------
- +
```

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Interrupt Processing

Values: Use APIC, Use Legacy PIC

Initializes APICs and uses them in an emulated PIC mode. For full-APIC mode, this parameter must be enabled along with ACPI. Do not change this setting after an operating system has been installed.

MP Tables (non ACPI OSes)

Values: Enabled, Disabled

Enabling this feature provides operating systems with APIC and processor information according to the Multi-Processor Specification. This feature requires the use of APICs. Do not change this setting after an operating system is installed.

Note: If you plan to stack more than one VL-EPMs-E1 card on the EPMs-21, you should disable this option to ensure proper operation.

Quick Boot

Values: Enabled, Disabled

Enables or disables a time-optimized POST, causing preconfigured boot optimizations to be made when the system boots. This will reduce POST time.

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ACPI

Values: Enabled, Disabled

Advanced control and power management (ACPI) is used with ACPI-aware operating systems. Do not change this setting after installing the OS.

POST Memory Manager

Values: Enabled, Disabled

Enables or disables the POST memory manager, which is needed by the preboot execution environment (PXE) boot ROMs to allocate memory for POST-time operation in order to perform their functions. If your boot ROM supports PXE, then you should enable this option.

System Management BIOS

Values: Enabled, Disabled

Enables or disables System Management BIOS, which supports DMI agents and other PXE clients.

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Splash Screen

Values: Enabled, Disabled

Enables or disables the display of the splash screen during the boot cycle. When the splash screen is enabled, it appears on the computer display for approximately one second. To learn how to create a custom splash screen, see VT1400 How to Create a Splash Screen.

Use Console Assignments Below

Values: On Remote User Detect, Always, Never

When set to Always, the console is directed to the selected device. When set to On Remote User Detect, the console will be directed to the selected device only when there is no video device available, or when the user has specifically requested redirection by pressing Enter or Ctrl-C on the serial terminal. CMOS Setup and some operating systems such as DOS can use the redirected console for user interaction. The redirected console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control. (See "Console Redirection" in the *EPMs-21 Reference Manual*.)

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POST Console

Sets the serial port for console redirection.

Note: The Preboot Console and Debugger Console parameters are not used.

Legacy-Free

Values: Enabled, Disabled

Enables or disables support for Microsoft's Legacy-Free Specification.

Plug-N-Play Header

Values: Enabled, Disabled

When enabled this option provides a "$PnP" pointer to BIOS extensions. This allows some add-on cards to function without needing full PnP support.

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P7 Geyserville/Speedstep

Values: Enabled, Disabled

Enabling this feature sets Geyserville/Speedstep processors to full speed.

Intel VT

Values: Enabled, Disabled

Enables or disables Intel Virtualization Technology.

Microcode Update

Values: Enabled, Disabled

Enables or disables processor microcode update.

Core Multi-Processing

Values: Enabled, Disabled

When disabled, the second execution core will not be visible to software and cannot be started via an SIPI message.

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Firmbase Menu

The Firmbase menu configures Firmbase Technology (the 32-bit firmware infrastructure of the BIOS). It is recommended that you do not change settings beyond the Basic Firmbase Technology Configuration options on this menu.

```
+ ------------------------- ---------------------------- + ------------------
- +
| Features Enabled by Firmbase[R] Technology             |Enable to support
USB|
| ------------------------- ---------------------------- |keyboard and mouse
|
| Legacy USB                    [Enabled]                |
|
| USB Boot                      [Enabled]                |
|
| EHCI/USB 2.0                  [Enabled]                |
|
| Firmbase User Shell           [Enabled]                |
|
|                                                        |
|
| Basic Firmbase[R] Technology Configuration             |
|
| ------------------------- ---------------------------- |
|
| Firmbase Technology           [Enabled]                |
|
| Firmbase Debug Log            [None]                   |
|
| Firmbase System Console       [None]                   |
|
| Firmbase Shell on Serial Port [None]                   |
|
|                                                        |
|
| Firmbase[R] Technology Foreground IRQ Monitoring       |
|
| ------------------------- ----------------------------|
|
| IRQ0 (Timer)                  [Disabled]               |
|
| IRQ1 (Keyboard)               [Disabled]               |
|
| IRQ2 (Cascade)                [Disabled]               |
|
| IRQ3 (COM2/COM4)              [Disabled]               |
|
| IRQ4 (COM1/COM3)              [Disabled]               |
|
| IRQ5 (LPT2)                   [Disabled]               |
|
| IRQ6 (Floppy)                 [Disabled]               |
|
| IRQ7 (LPT1)                   [Disabled]               |
|
```

```
| IRQ8 (RTC)                    [Disabled]              |
|
| IRQ9 (PCI/SCI)                [Disabled]              |
|
| IRQ10 (PCI)                   [Disabled]              |
|
| IRQ11 (PCI)                   [Disabled]              |
|
| IRQ12 (Mouse)                 [Disabled]              |
|
| IRQ13 (NPX)                   [Disabled]              |
|
| IRQ14 (IDE)                   [Disabled]              |
|
| IRQ15 (IDE)                   [Disabled]              |
|
|                                                       |
|
+ -------------------------- ---------------------------- + ------------------
- +
```

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Legacy USB

Values: Disable, Enable

Enables or disables BIOS support for USB keyboards and USB mice.

USB Boot

Values: Enabled, Disabled

Enables BIOS access to USB mass storage devices. The Enabled setting is required for booting from USB hard drives or CD-ROM drives. It is not required for the OS access to USB mass storage devices.

EHCI/USB 2.0

Values: Enabled, Disabled

The BIOS is capable of booting from a USB device, or of mounting one as a drive letter. If EHCI/USB 2.0 is enabled, this access will take advantage of the USB 2.0 (EHCI) controller. Otherwise, the USB 1.1 (OHCI) controller will be used. In either case, the EHCI controller is available for the OS to use.

Firmbase User Shell

Values: Enabled, Disabled

Enables or disables the Firmbase shell.

Firmbase Technology

Values: Enabled, Disabled

Enables or disables Firmbase Technology, an operating environment running in the CPU's System Management Mode (SMM). Enable to provide SMM support for legacy USB, USB booting, and some other features. Disabling this is for troubleshooting only, as Windows and Linux boot is likely to fail.

Firmbase Debug Log

Values: None, COM1, COM2, COM3, COM4

Specifies the device used to display diagnostic messages for Firmbase.

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Firmbase System Console

Values: None, COM1, COM2, COM3, COM4

Specifies the device used by the Firmbase system process to display sign-on banners of all Firmbase applications loaded during system initialization.

Firmbase Shell on Serial Port

Values: None, COM1, COM2, COM3, COM4

Specifies a serial port that can be used by the Firmbase User Shell.

Firmbase Technology Foreground IRQ Monitoring

Values: Enabled, Disabled

Enables or disables foreground IRQ monitoring for specific interrupts. If a monitored IRQ is pending while Firmbase is running, then control will be quickly returned to the foreground OS where the IRQ can be serviced. This can help some latency-sensitive applications.

BACK TO FIRMBASE

Misc Menu (BIOS Rev. 6.5.101 and Earlier)

The Misc menu only appears in BIOS revision 6.5.101 and earlier. It configures miscellaneous features such as system cache and keyboard control.

```
+ ------------------------ -------------------------- + -----------------
- +
| Cache Control                                       |Enable to allow CPU
|
```

```
| ------------------------- ---------------------------- |caching to operate.
|
| System Cache                    [Enabled]                |
|
|                                                          |
|
| Keyboard Control                                         |
|
| ------------------------- ---------------------------- |
|
| Keyboard Numlock LED            [Disabled]               |
|
| Typematic Rate                  [30/sec]                 |
|
| Typematic Delay                 [250ms]                  |
|
|                                                          |
|
| Miscellaneous BIOS Configuration                         |
|
| ------------------------- ---------------------------- |
|
| Lowercase Hex Displays          [Disabled]               |
|
|                                                          |
|
|
|                                                          |
|
+ ------------------------- ---------------------------- + ------------------
- +
```

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System Cache

Values: Enabled, Disabled

Enables or disables the operation of L2 cache.

Keyboard NumLock LED

Values: Enabled, Disabled

Enables or disables NumLock. Set this option to Disabled to turn off the NumLock key when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. Some operating systems, such as DOS, honor this initial setting and use it for run-time operations. Other operating systems, such as Windows, assume complete control of the NumLock state, and do not honor this setting.

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Typematic Rate

Values: 30/sec, 20/sec, 10/sec, 8/sec, 6/sec, 5/sec, 4/sec, 3/sec, 2/sec

Sets the rate at which a keyboard key will automatically repeat when held down, expressed in characters per second. Some operating systems, such as DOS, honor this initial setting and use it for run-time operations. Other operating systems, such as Windows, assume complete control of the Typematic Rate, and do not honor this setting.

Typematic Delay

Values: 250ms, 500ms, 750ms, 1 sec

Sets the amount of time a keyboard key must be held down before it begins automatically repeating. Some operating systems, such as DOS, honor this initial setting and use it for run-time operations. Other operating systems, such as Windows, assume complete control of the Typematic Delay, and do not honor this setting.

Lowercase Hex Displays

Values: Enabled, Disabled

Enables or disables the display of lowercase characters in hexadecimal numbers in the debugger.

BACK TO MISC

Video Menu

The Chipset menu configures chipset settings, particularly video device settings.

```
+ ------------------------- ---------------------------- + ------------------
- +
|                                                       |Select video boot
|
| Display Device Configuration                          |display.
|
| ------------------------- ---------------------------- |
|
| Video Boot Display            [Default]                |
|
| LCD Flat Panel Type           [800x600 LVDS Color      |
|
| Panel]                                                 |
|
| Panel Fitting                 [Default]                |
|
| Spread Spectrum               [Disabled]               |
|
|                                                       |
|
+ ------------------------- ---------------------------- + ------------------
- +
```

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Video Boot Device

Values: Default, CRT, TV, EFP, LFP

Selects the video boot device.

LCD Flat Panel Type

Values: 640x480 LVDS Color Panel, 800x600 LVDS Color Panel, 1024x768 LVDS Color Panel, 640x480 8.4 NEC, 800x480 9 NEC, 1024x600 5.61 TMD, 1024x600 4.8 Samsung, 1024x768 15 Samsung, 1280x768 7.2 Sharp, 1280x800 15.4 Samsung, 1280x1024 LVDS Color Panel, 1280x800 LVDS Color Panel, 1366x768 11.1 TMD

Selects the flat panel type.

Panel Fitting

Values: Default, Center All, Stretch Text, Stretch Graphics

Selects the display expansion/centering setting.

Spread Spectrum

Values: Enabled, Disabled

Enables or disables the LVDS spread spectrum setting.

Note: If you are using the VL-CBR-2014 LVDS to VGA Adapter Card, enabling this option causes video noise to occur.

BACK TO VIDEO

Chipset Menu

The Chipset menu configures chipset settings, particularly video device settings.

```
+ ------------------------ -------------------------- + -----------------
- +
|                                                     |Enable Wake-On-RTC.
|
| RTC Alarm Configuration                             |
|
| ------------------------ -------------------------- |
|
| Wake-On-RTC                  [Disabled]             |
|
|   RTC Alarm                  [00:00:00]             |
|
```

```
|                                                                  |
|
| Intel SCH US15W Configuration                                    |
|
| ------------------------- --------------------------- |
|
| Video Frame Buffer Size       [8MB]                      |
|
| IGD MSI                       [Disabled]                 |
|
| Route USB P2 to USB Client    (Enabled]                  |
|
|                                                                  |
|
+ ------------------------- --------------------------- + ------------------
- +
```

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Wake-On-RTC

Values: Enabled, Disabled

Enables or disables Wake-On-RTC.

RTC Alarm

Sets the hours, minutes and seconds for Wake-On-RTC.

Video Frame Buffer Size

Values: 1MB, 4MB, 8MB

Selects the size of the frame buffer for on-board video.

IGD MSI

Values: Enabled, Disabled

Enables or disables IGD message signaled interrupts.

Route USP P2 to USB Client

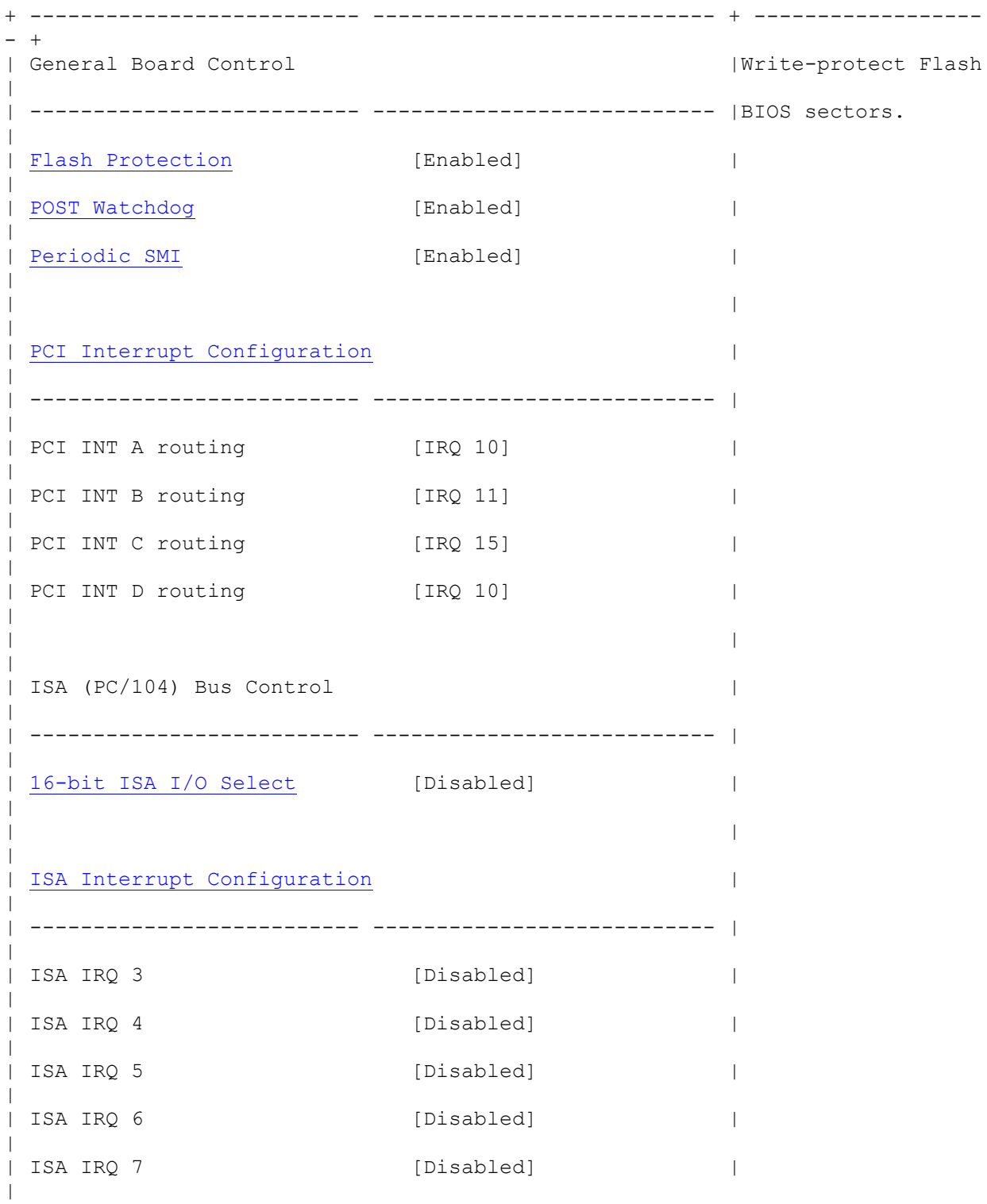
Values: Enabled, Disabled

Controls whether USB port 2 is routed to the client or host USB controller.

BACK TO CHIPSET

Board Menu

The Board menu configures PCI interrupts, enables and disables ISA interrupts, and configures hardware monitoring interrupts.



ISA IRQ 9	[Disabled]
ISA IRQ 10	[Disabled]
ISA IRQ 11	[Disabled]
ISA IRQ 12	[Disabled]
ISA IRQ 15	[Disabled]
ISA I/O Range Forwarding	
-------------------------	-------------------------
080 to 080	[Enabled]
100 to 1CF	[Disabled]
200 to 2E7	[Disabled]
2E8 to 2EF	[Disabled]
2F0 to 2F7	[Disabled]
2F8 to 2FF	[Disabled]
300 to 377	[Disabled]
378 to 3E7	[Disabled]
3E8 to 3EF	[Disabled]
3F0 to 3F7	[Disabled]
3F8 to 3FF	[Disabled]
400 to AFF	[Disabled]

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Flash Protection

Values: Enabled, Disabled

Enables or disables write protection of the flash BIOS sectors. You must disable Flash Protection in order to reprogram or update the BIOS.

POST Watchdog

Values: Enabled, Disabled

Enables or disables the watchdog timer during POST. When enabled and POST progress halts unexpectedly, the watchdog will timeout and reboot the board, giving it another chance to be successful. (When disabled, a POST hang condition will just hang the board.)

Periodic SMI

Values: Enabled, Disabled

Enables or disables the periodic System Management Interrupt. Enabling this option gives periodic CPU time slices to Firmbase after POST completes. Firmbase primarily allows USB keyboards and mass storage devices to behave as legacy PS/2 and IDE devices for operating systems such as DOS, which don't natively support USB. Disabling this option can improve reliability of serial port traffic running at 115200 baud or greater. It should also be disabled for real-time applications with latency sensitivity in the 1 millisecond range.

PCI Interrupt Configuration

Values: IRQ 10, IRQ 11, IRQ 15

Sets PCI interrupts. All four PCI interrupts can be shared without conflict, but in certain high performance hardware configurations, the assignment of separate IRQs can reduce IRQ latency. Make sure there are no conflicts with the ISA IRQ settings.

16-bit ISA I/O Select

Values: Enabled, Disabled

"Restrictions apply to 16-bit I/O. The IOCSIG pin must be asserted, all transactions are word-aligned (even addressed), and all transactions are 16-bit only."

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ISA Interrupt Configuration

Values: Enabled, Disabled

Enables or disables ISA interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12 and 15 for access by ISA (PC/104) devices. These must not conflict with the PCI IRQ settings.

ISA I/O Range Forwarding

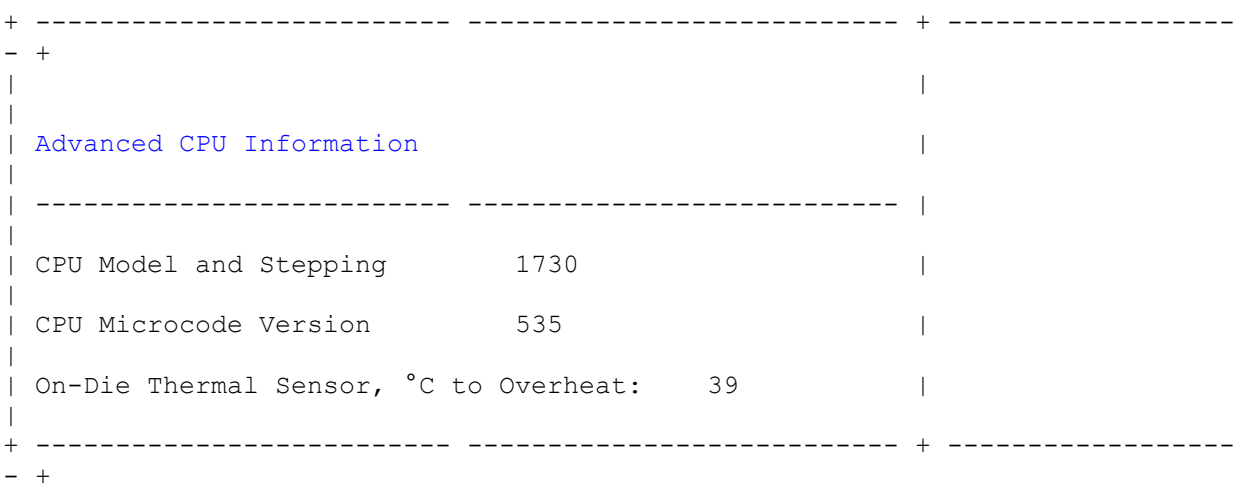
Values: Enabled, Disabled

Enables or disables ISA I/O forwarding of specific I/O ranges.

BACK TO BOARD

AdvancedCPU

The AdvancedCPU menu displays temperature and other CPU information.



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