EBX-11 SPI Controller Redesign

The serial peripheral interface (SPI) controller has been redesigned on the EBX-11 Rev. 6.00 to improve its flexibility and ease of programming. Customers who use the EBX-11 Rev. 5.xx or earlier SPI interface have two options when migrating to the Rev. 6.00 board:

- Update software to take advantage of the Rev. 6.00 SPI interface.
- Load the 5.xx PLD code onto 6.xx boards and continue using the old register interface.

Revision 5.xx boards may be updated with the 6.00 PLD code, available on the EBX-11 support site.

Overview:

The redesign of the SPI controller is extensive. Control registers are reorganized, with some features added and others eliminated. An extra data register has been added, as well as a data streaming mode for use in SPI applications that require more control over the SPI hardware lines.

The use of interrupts is different with the new controller. In order to use interrupts, the slave device must be able and configured to issue a hardware interrupt.

There are only two control registers instead of three. Most of the control functionality has been retained, with some functionality added. In the previous SPI implementation, the three control registers contained a number of unused bits, which have been eliminated.

Summary of Changes:

SPI Control Registers

Removed Functionality:

- The DONE bit has been removed. This bit was somewhat redundant with the BUSY bit, which has been retained.
- The ability to generate an IRQ upon completion of each SPI transaction has been removed. This feature proved to be impractical in use.

Added Functionality:

- A manual slave select mode has been added. In the previous implementation, writing data to the most significant data byte triggered the SPI transaction, and the SPI controller automatically asserted the configured slave select. This is still the default behavior, but in the new implementation the slave select can be controlled by software: manually asserted and held low while any number of data bytes is sent. Then the slave select must be commanded high to complete the transaction. Any SPI device can be operated in this manner.
- The shift direction of the data registers can now be controlled. The data can be right-shifted toward the least significant bit or left-shifted toward the most significant bit.

- An interrupt state flag has been added, which directly indicates whether an SPI device hardware interrupt is asserted or deasserted. This allows a software poll-able SPI device interrupt status when an IRQ is not available or desired.

Changed Functionality:

- Interrupt channel selection is now accomplished with two bits instead of four. Same IRQs selectable, but there is also an IRQ enable bit to "claim" the IRQ for SPI operation. The selected IRQ is still shared with the PC/104 bus and must be configured in CMOS for ISA IRQx. Only SPI devices that can initiate a hardware interrupt are now supported. This currently includes the on-board digital I/O, SPX-2, and SPX-3. The on-board digital I/O chips must be configured for open drain and mirrored interrupts in order for any SPI device to use hardware interrupts. In previous versions this was done by the BIOS during POST.

SPI Data Registers

- There are now four data registers (32 bits) instead of three (24 bits). Common BYTE, WORD, and DWORD I/O programming functions can be utilized to access the SPI registers.
- The I/O address of the most significant data byte is now 1DDh instead of 1DCh.

SPI Register Comparison:

The following table shows the functions of I/O ports 1D8h through 1DDh in the Rev. 5.xx and 6.xx of the SPI controllers.

I/O Port	*Rev. 5xx and earlier boards*	*Rev. 6.xx and later boards*
1D8h	SPI Control	SPI Control
1D9h	SPI Control	SPI Control and Status
1DAh	Data - LSB	Data - LSB
1DBh	Data	Data
1DCh	Data - MSB	Data
1DDh	SPI Control	Data - MSB

The address of the most significant data byte is important. By default, a write to the MSB automatically triggers an SPI transaction. In EBX-11 Ver. 5.xx, the I/O port address of the MSB was 1DCh, and in Ver. 6.xx, it is 1DDh. Automatic mode is still the default. (See the description of the new manual slave select mode.)

The following tables provide a bit-by-bit comparison of the differences between the legacy and new SPI controller implementations. See the EBX-11 Reference Manual for a complete description of both register sets.

Legend:

shaded background	function and position of bits has not changed

colored text	function has been retained but bits have moved
black text without shading	function is unique to a version
reserved	bit unused

I/O Port 1D8h

	7	6	5	4	3	2	1	0
Rev. 6.00 and later	clock idle	clock phase	frame length	frame length	manual mode	slave select	slave select	slave select
Rev. 5.xx and earlier	interrupt enable	busy	clock polarity	clock frequency	clock frequency	chip select	chip select	chip select

I/O Port 1D9h

	7	6	5	4	3	2	1	0
Rev. 6.00 and later	IRQ select	IRQ select	clock frequency	clock frequency	interrupt enable	data shift direction	interrupt state	busy
Rev. 5.xx and earlier	reserved	reserved	frame length	frame length	reserved	done	clock idle	reserved

I/O Port 1DAh

	7	6	5	4	3	2	1	0
Rev. 6.00 and later	data7	data6	data5	data4	data3	data2	data1	data0
Rev. 5.xx and earlier	data7	data6	data5	data4	data3	data2	data1	data0

I/O Port 1DBh

	7	6	5	4	3	2	1	0
Rev. 6.00 and later	data15	data14	data13	data12	data11	data10	data9	data8
Rev. 5.xx and earlier	data15	data14	data13	data12	data11	data10	data9	data8

I/O Port 1DCh

	7	6	5	4	3	2	1	0
Rev. 6.00 and later	data23	data22	data21	data20	data19	data18	data17	data16
Rev. 5.xx and earlier	data23	data22	data21	data20	data19	data18	data17	data16

I/O Port 1DDh

	7	6	5	4	3	2	1	0
Rev. 6.00 and later	data31	data30	data29	data28	data27	data26	data25	data24
Rev. 5.xx and earlier	reserved	reserved	reserved	reserved	IRQ select	IRQ select	IRQ select	IRQ select

###