

July 06, 2007

## Product Advisory #5147 EBX-11

This is a formal notification that a product supplied by VersaLogic Corporation is being revised. Our records indicate that your company has purchased this product.

Please read this notice thoroughly to determine what impact this change may have on you in regards to your currently owned product or future purchases from VersaLogic.

### Affected Product

Part Number	Description	Old Revision Level	New Revision Level
EBX-11g	Python SBC	4.01	5.00

### Changes Made to Product

The following changes have been made to the EBX-11 (Python):

- The PLD has been modified to enable true 16-bit ISA transfers.
- Wire modifications that were made to Rev. 4 boards have been designed into the Rev. 5 PCB.
- The COM3 and COM4 RxD+/- signals have been corrected: On Rev. 4.01 and earlier boards, the RxD+/- signals were transposed and nonconforming to the serial port pinouts of other VersaLogic boards. This has been corrected with Rev. 5.00. See the EBX-11 Reference Manual for details. Applications using EBX-11 connector J4, or CBR-5009 connectors J5 or J6, may have to be rewired for Rev. 5.00 and later boards.
- The Digital I/O, PWM, and TACH input signals have been corrected: On Rev. 4.01 and earlier boards, the digital I/O 0-11, PWM, and TACH input signal configuration was nonstandard. This has been corrected with Rev. 5.00. See the EBX-11 Reference Manual for details. Applications using EBX-11 connector J5, or connectors on CBR-4004, may have to be rewired for Rev. 5.00 and later boards.
- The SPI transceivers and Digital I/O chips are now powered with 3.3V instead of 5.0V for SPX™ compliance.
- The USB interface at J13 has been changed from a 10-pin 2mm header to two USB Type-A connectors.
- Connector J17 has been moved to 1.260" from the bottom edge of the board for SPX™ compliance.



- SPI signal names have been changed in the schematic and reference manual to comply with industry standards. The standard signal names are: SSx# (Slave Select), MISO (Master In Slave Out), MOSI (Master Out Slave In), and SCLK (Serial Clock).
- A number of pull-up resistors have been added.
- A number of changes have been made to the board silkscreen.

### **Customer Impact**

<b>Fielded Units</b>	<b>Future Shipments</b>
There is no impact to fielded units. Due to PCB layout changes, fielded units are not upgradeable.	New revision units will begin shipping in July 2007.

There is no impact to customers with existing products in the field; however, applications that use certain interfaces may require rewiring, as described below:

- Applications that use the COM3, COM4, Digital I/O 0-11, PWM output, or TACH input interfaces must be rewired to accommodate the corrected signaling.
- Applications that use the USB interface at connector J13 must be re-cabled with USB Type-A connectors.

### **Additional Information**

For additional information or assistance related to this change, please contact VersaLogic Customer Support at [Support@VersaLogic.com](mailto:Support@VersaLogic.com) or call (541) 485-8575.