Reference Manual

VL-AIN-1a
VL-AIN-1b

Integrating Analog Input
Card for the STD Bus

STD

VERSALOGIC
CORPORATION

VL-AIN-1a
VL-AIN-1b

Integrating Analog Input Card
for the STD Bus

Model VL-AIN-1a & VL-AIN-1b

Cards for the STD Bus

REFERENCE MANUAL

VL-AIN-1a Rev. 0.00
VL-AIN-1b Rev. 0.00
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MAIN1

Model STD AIN-1
Analog Input Card for the STD BUS
Part Number 2370

REFERENCE MANUAL

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OVERVIEW

The STD AIN-1 board, part number 2370, is an eight channel integrating analog input board compatible with the STD BUS. It provides precision measurements of up to eight single-ended or differential voltage sources, or current loop inputs.

Operating Description

The AIN-1 board uses an integrating conversion technique to perform the analog to digital (A/D) conversion. This method differs from the popular successive approximation technique, used on many A/D boards, in that no "sample and hold" circuit is involved.

Rather than taking only an instantaneous "sample" of the input signal to measure, the integrating method measures the actual input signal during the conversion cycle. This makes for much higher accuracy in reading changing (moving) input signals, and virtually eliminates errors caused by reading or "sampling" a noise pulse on the input signal. The integrating conversion method is much more noise tolerant, and requires less conditioning of the input signals to maintain stable, accurate readings.

The trade-off for these advantages is a slower conversion time. A conversion time of 45ms (90ms if a polarity change occurs) can be prohibitively slow when a system processor needs to read many channels per second. To overcome this problem, without losing the advantages of integrating conversion, the AIN-1 card uses an on-board processor. This processor constantly scans the active input channels and does conversions on them whether or not the system processor needs the data. Current readings for each channel are constantly taken and updated in the on-board RAM memory. When the system processor needs data from one of the input channels, the AIN-1 board can supply the reading immediately, without waiting for a conversion to take place.

The result is a board with the advantages of an integrating A/D converter, but a reading time of only 60us or less.

In addition, the AIN-1 board features two voltage input ranges (±5V and ±10V), 1 part in 4000 (12 bit) resolution, and accommodation of both voltage and current loop inputs.

STD BUS COMPATIBILITY

The STD AIN-1 board is compatible with both 8085/Z80 and 65/6800 type systems (65/6800 systems must include I/O addressing). It requires only +5V (regulated) power for operation.

When inserting the AIN-1 board into an STD BUS card cage, be certain that the card ejector (pin 1 edge of the card) is aligned in the same direction as other cards in the system (usually upward). The AIN-1 board has a key slot cut between pins 25 and 27. It is recommended that a matching key be installed in the STD BUS motherboard connector to prevent the card from being installed upside down.

The STD AIN-1 board should be inserted or removed from the STD BUS card cage only when the power to the bus is turned off.

STD BUS Pinout

Connections from the AIN-1 board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the AIN-1 board.

COMPONENT SIDE				SOLDER SIDE			
PIN	SIGNAL	FLOW	DESCRIPTION	PIN	SIGNAL	FLOW	DESCRIPTION
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	-	-5V or bat. backup	6	-5V	-	-5V power
7	D3	I/O	Data bus	8	D7	I/O	Data bus
9	D2	I/O	Data bus	10	D6	I/O	Data bus
11	D1	I/O	Data bus	12	D5	I/O	Data bus
13	DO	I/O	Data bus	14	D4	I/O	Data bus
15	A7	In	Address bus	16	A15	-	Address bus
17	A6	In	Address bus	18	A14	-	Address bus
19	A5	In	Address bus	20	A13	-	Address bus
21	A4	In	Address bus	22	A12	-	Address bus
23	A3	In	Address bus	24	A11	-	Address bus
25	A2	In	Address bus	26	A10	-	Address bus
27	A1	In	Address bus	28	A9	-	Address bus
29	AO	In	Address bus	30	A8	-	Address bus
31	WR*	In	Write strobe	32	RD*	In	Read strobe
33	IORQ*	In	I/O addr. select	34	MEMRQ*	-	Memory addr. select
35	IOEXP*	In	I/O expansion	36	MEMEX*	-	Memory expansion
37	REFRESH*	-	Refresh timing	38	MCSYNC*	-	Machine cycle sync.
39	STATUS1*	-	CPU status	40	STATUSO*	-	CPU status
41	BUSAK*	-	Bus acknowledge	42	BUSRQ*	-	Bus request
43	INTAK*	-	Interrupt acknowl.	44	INTRQ*	-	Interrupt request
45	WAITRQ*	Out	Wait request	46	NMIRQ*	-	Non-maskable interrupt
47	SYSRESET*	In	System reset	48	PBRESET*	-	Push button reset
49	CLOCK*	-	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	-	Priority chain out	52	PCI	-	Priority chain in
53	AUXGND	-	±12 volt ground	54	AUXGND	-	±12 volt ground
55	AUX+V	-	+12 volt input	56	AUX-V	-	-12 volt input

HARDWARE CONFIGURATION

Before input signals are connected to the AIN-1 board, it must be configured properly for the types of signals that it will receive. These options are discussed below.

Input Mode

The AIN-1 board can accommodate three types of voltage inputs, differential, single-ended, and pseudo-differential. It should be noted however that the types of inputs connected to the board must all be of the same type. Typical connections for the three input modes are shown in the following diagram. Since ground loops (current flowing between various equipment ground lines) can affect analog measurements, careful attention should be paid to the ground connections in these diagrams. In particular, the STD BUS power supply logic ground line should never be connected to earth ground when operating in the differential or pseudo-differential modes.

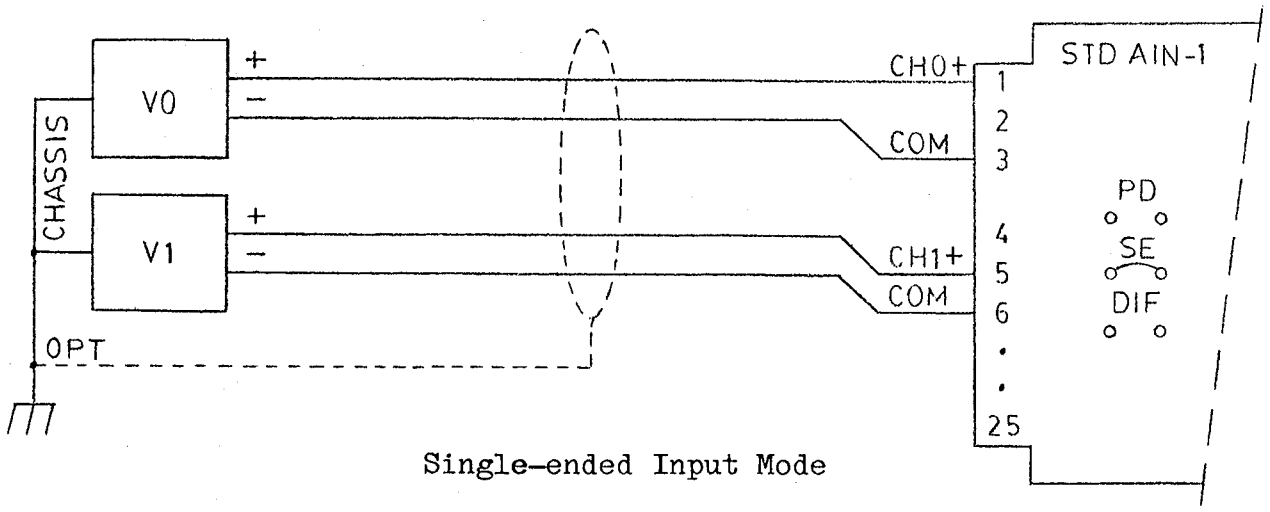
The differential mode is used for signals that are not referenced to a common or ground point, but simply have a voltage difference between the two input wires (usually a twisted pair). It is desirable to use the differential mode in electrically noisy environments since it reduces the effects of electromagnetically induced noise and ground currents. It is especially useful in canceling the "common mode" noise generated on input lines over longer distances. The differential mode is selected by jumpering the "DIF" pads.

The single-ended mode is used for signals that are referenced to a common system ground. It is normally used only for very short distance runs (typically less than 10'). This mode is selected by jumpering the "SE" pads.

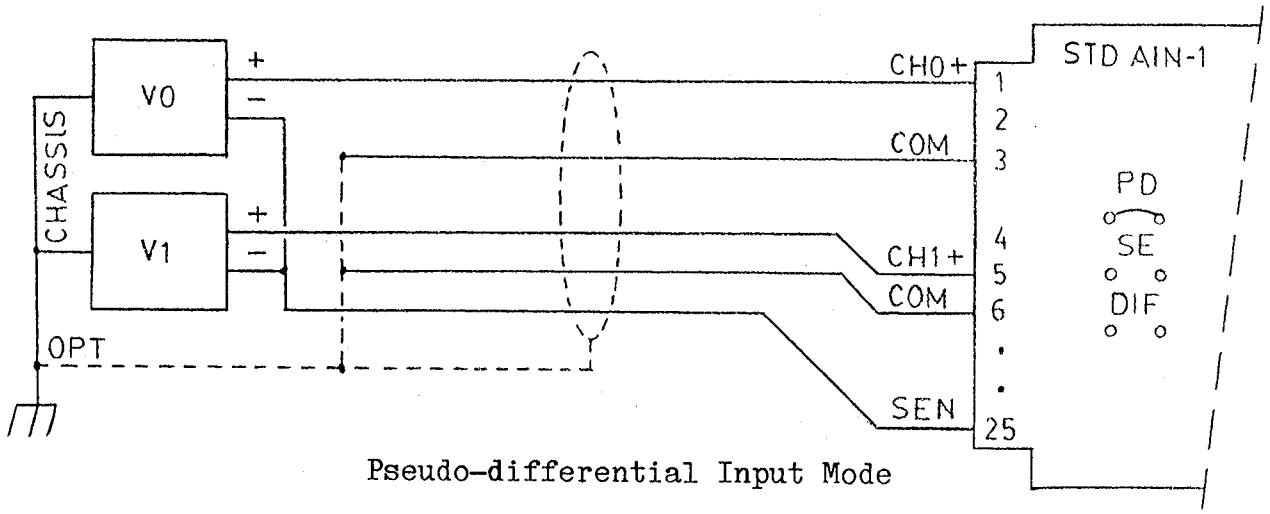
The pseudo-differential mode is used for signals that are not referenced to ground, but are all connected to a single common return line. This mode can provide most of the advantages of full differential input while requiring fewer total wires. The pseudo-differential mode is selected by jumpering the "PD" pads.

See Jumper Options for further information on the location of the input mode jumpers.

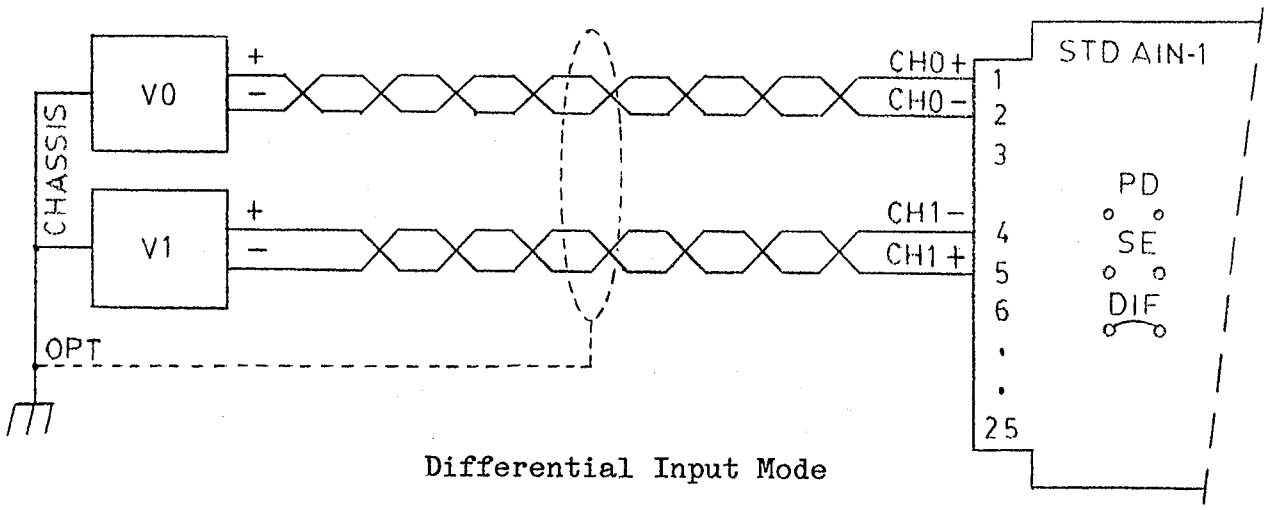
AIN-1 INPUT CONNECTION DIAGRAMS



Single-ended Input Mode



Pseudo-differential Input Mode



Differential Input Mode

Input Range

The AIN-1 board can be operated in either of two voltage input ranges. The voltage range selected applies to all of the board's eight input channels. The "RNG" jumper selects between the ±5 volt input range (jumper in), and the ±10 volt input range (jumper open).

For input signals of less than 5 volts, selecting the lower voltage range will provide twice the resolution for each measurement (2.5mv versus 5mv in the ±10V range) without affecting stability or conversion time. See Jumper Options for more information.

Current Loop Inputs

In addition to voltage inputs, the AIN-1 board can optionally accept up to eight 4-20 ma current loop inputs. The current loop mode is selected by installing a 200 ohm .1% precision resistor in location CL0 thru CL7 for current loop inputs on channels 0 thru 7 respectively. A set of eight resistors are available for this purpose as VersaLogic part number 2670.

When using the board with current loop inputs, it must be jumpered for differential voltage input (jumper DIF). The range jumper (RNG) should normally be installed (±5V range) to provide the greatest resolution possible.

INPUT CONNECTION

Analog input signals are connected to the AIN-1 board using a standard 26 pin socket connector which mates with the on-board header. Standard cable assemblies are available for this purpose from VersaLogic (refer to the VersaLogic STD BUS Series Price List for more information).

When connecting a 26 pin socket to the board, it must be oriented correctly. The "pin 1" end of the connector (red stripe or marking on the cable) should be installed nearest to the card ejector on the AIN-1 board.

Input Connector Pinout

The pinout of the input connector is shown below. Connector pin 1 is nearest to the card ejector and farthest from the board edge. Pin 2 is nearest to the card ejector and nearest to the card edge (all even numbered pins are in the same row).

Note that each of the eight channels (0 thru 7) has a "+" and a "-" connection. The "+" terminal is used in all input modes, while the "-" terminal is used only in the differential and current loop input modes. Refer to the Hardware Configuration section for more information on input modes and input connections.

Connector P1

Pin	Signal
1	CH0+
2	CH0-
3	AGND
4	CH1-
5	CH1+
6	AGND
7	CH2+
8	CH2-
9	AGND
10	CH3-
11	CH3+
12	AGND
13	CH4+
14	CH4-
15	AGND
16	CH5-
17	CH5+
18	AGND
19	CH6+
20	CH6-
21	AGND
22	CH7-
23	CH7+
24	AGND
25	SENSE
26	(No Connection)

Note: AGND = Analog ground.

ADDRESS SELECTION

The AIN-1 board is an I/O mapped board which occupies two I/O port locations. An on-board ten position switch (labeled "Address") is used to select the starting address of the board. The table below shows the ten possible address selections and the resulting locations of the two I/O ports.

Switch Setting	Location (Hex)	Location (Decimal)
0	00-01	00-01
1	10-11	16-17
2	20-21	32-33
3	30-31	48-49
4	40-41	64-65
5	50-51	80-81
6	60-61	96-97
7	70-71	112-113
8	80-81	128-129
9	90-91	144-145

Addressing of the AIN-1 board is also controlled by the "A1", "A2", "A3", and "IOX" jumpers. The "A1", "A2", and "A3" jumpers allow the board to be located at 70 additional port locations if necessary. The "IOX" jumper allows the AIN-1 board to be located in the extended (or "secondary") I/O map rather than the normal one. These pads should only be jumpered for special applications. See Jumper Options for more information.

SOFTWARE INTERFACE

The AIN-1 board is operated thru two system I/O ports. Two data ports are used to read 16 bits of the requested data from the board, while a single command port is used to request data for a specific analog channel, and control other aspects of the AIN-1 board's operation.

I/O Port Locations

Once the board's starting address is selected (see Switch Settings), the locations of the AIN-1's two I/O ports can be determined. The relative locations of the command port (for writing to the board), and the data ports (for reading data from the board) are listed below.

Port Name	Port Address
Command Port	Board address + 0
Low Byte Data Port	Board address + 0
High Byte Data Port	Board address + 1

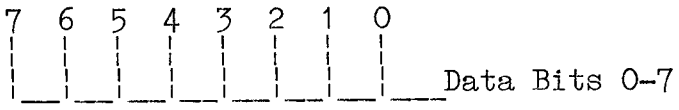
Command Port

The "command port" on the AIN-1 board is used primarily to request input data from a specific channel. It can also be used to initiate the built-in self test routine, or limit the number of channels that are scanned and converted (discussed later in this section).

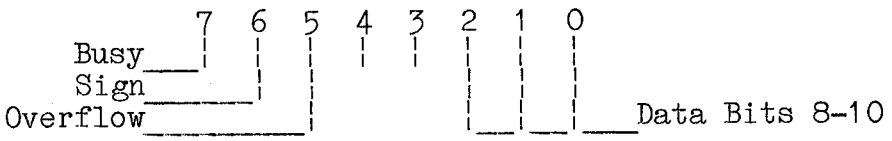
To request data from one of the eight input channels (numbered 0 thru 7), the command "x" is written to the command port, where x is the desired channel number. Writing a "4" to the command port will allow data from channel 4 to be read from the board, etc.

Data Ports

The two on-board data ports are used to read 16 bits of data and status information from the AIN-1 board. The function of each bit is shown below.



Low Byte Data Port



High Byte Data Port

Because each reading taken by the AIN-1 board involves more than eight bits of data, two data ports must be read to assemble all the information. When reading these two ports the high data byte port must always be read first as it contains the busy bit (i.e. "ready" bit) that signals when valid data has (or has not) been loaded into the data port registers.

As you can see from the above diagram, the low data port contains bits 0 thru 7 of the requested reading. The high data port contains the upper three bits (8-10) in bits 0-2 respectively. The other bits in the high data port are used for:

Busy - Bit 7 is set high (busy) when a data request is made by writing to the command port. When the request has been filled, and valid data has been loaded into the high and low data ports, the busy bit is reset to a zero.

Sign - Bit 6 is set high whenever the reading is a negative (less than zero) number.

Overflow - Bit 5 is set high whenever an overflow or underflow occurs on the channel being measured. This occurs when the input voltage is less than -5V or greater than +5V when the board is set on the 5 volt range, or less than -10V or greater than +10V when the board is set on the 10 volt range. When an underflow occurs both the overflow and sign bits will be set high.

Data Format

The AIN-1 provides data in a signed binary format. The eleven significant bits provide readings from 0 thru 1999 (0 thru 7CF hex) which represent zero thru the full scale voltage that the board is jumpered for (either 5 or 10 volts). The sign bit will be set when the reading represents a voltage of a negative polarity.

Since the board provides 2000 steps or "counts" between zero and the full scale voltage, the resolution will be doubled when the board is set on the 5 volt range. Each count represents .005 volts in the 10 volt range, and .0025 volts in the 5 volt range. Some examples are shown below.

Input Voltage =	5V range Reading =	10V range Reading
0.005	2	1
0.010	4	2
0.100	40	20
0.500	200	100
1.000	400	200
2.000	800	400
3.000	1200	600
4.000	1600	800
4.9975	1999	998
5.000	-	1000
6.000	-	1200
7.000	-	1400
8.000	-	1600
9.000	-	1800
9.995	-	1999

Usually the readings from the AIN-1 board need to relate more to a particular type of input sensor than to a voltage reading. In this case the reading can be converted (divided by some factor) directly into the desired units of temperature, pressure, or some other measure, without concern for the equivalent voltage level of the signal.

When an actual voltage level reading is desired, input from the AIN-1 can be converted as shown below. The conversion with two implied decimal places is useful for languages that allow integer numbers only (i.e. 481 = 4.81 volts).

5V scale: Actual Voltage = AIN-1 reading / 400
Voltage w/two implied decimal places = AIN-1 reading / 4

10V scale: Actual Voltage = AIN-1 reading / 200
Voltage w/two implied decimal places = AIN-1 reading / 2

For channels that are used as current loop inputs (current loop resistors installed in some positions CL0-CL7), the input readings will reflect voltage drop present across the 200 ohm current loop resistor. The table below shows the voltage drop and AIN-1 readings that result from various input currents.

If desired, these input readings can be converted to actual current values as follows: Actual Current = AIN-1 reading / 80.

Current =	Voltage =	Reading(5V range)
4ma	0.8V	320
5	1.0	400
10	2.0	800
15	3.0	1200
20	4.0	1600
25	5.0	1999

BOARD OPERATION

Active Channels Control

Normally the AIN-1 board will scan and maintain measurements on all eight input channels. Since each channel requires a fixed period of time (45ms*) to convert to a digital reading, the time between updates for each channel is a function of how many channels must be converted. With all eight channels being scanned, the data for each channel is updated every 360ms (45ms X 8 channels) or 2.7 times each second.

In applications where readings are needed more often, the AIN-1 board can be programmed to scan fewer channels. This is done by writing an "Fx" to the command port, where x is the highest channel to be scanned. For example, writing an "F4" to the command port would cause only channels 0 thru 4 to be active. With these five active channels, data for each channel would be updated every 225ms (45ms X 5) or 4.4 times each second.

If an update time faster than approximately 2.7 times per second is not required for your application then no maximum channel number needs to be set. The AIN-1 board will always default to reading all eight channels. This parameter is reset (to eight active channels) when system reset occurs.

*Note: A conversion time of 90ms can occur when converting a signal which has a polarity opposite from the previous one (going from positive to negative signals, etc.).

Self Test

The AIN-1 board includes a built-in self test routine which can be used to verify the integrity of the on-board hardware (RAM, ROM, CPU, etc.). This test, which can be performed at any time, is initiated by writing a hex "FF" (decimal 255) to the command port.

This command resets the maximum channel number to 7, and runs the internal self test routine. The busy bit (on the high data port) will remain set until the test is completed.

When the busy bit is reset to zero, the data ports will contain the following hex data:

High data port	Low data port	Meaning
00	10, 11, etc.	Board is OK, software version (1.0, 1.1, etc.) is on low data port.
7F	01	Board is bad, CPU chip defective.
7F	02	Board is bad, ROM chip defective.

Polled / Wait Modes

After data has been requested from the AIN-1 board (using the command port), there is a short delay while the data is moved into the high and low data ports for reading by the system CPU. This time varies, depending on what the on-board CPU is doing, but is never greater than 60us.

As supplied, the AIN-1 board is jumpered for polled operation. This means that the system CPU must check the busy bit (on the high data port) until it goes low to indicate that the requested data has been moved into the data ports (see note below).

Alternately, the on-board WT (wait) jumper can be installed. This will cause the system wait line (WAITRQ*) to be activated when the AIN-1 board is read and the requested data is not yet ready. The wait line will be released, allowing the program to continue, when the data has been moved into the ports and is available for reading. If this option is used it is never necessary to check the busy bit. In the wait mode the high data port should be read first since the wait line will be activated when the high port is read. The wait mode of operation is not compatible with 6800 series processors.

NOTE: In the polled mode the busy bit does not have to be read constantly; the system can do some other task and come back for the data from the AIN-1 board as desired. Once the data is available at the data ports it will remain there (and can be reread if needed) until another data request has been written to the command port.

Software Examples

Operation of the AIN-1 board is straightforward once a short subroutine has been written to facilitate reading the desired channel, checking the sign and overflow bits, and scaling the number if required.

The examples below assume that the board has been addressed at hex port 30 (decimal 48) in the polled mode (no wait jumper), on the 10 volt range (no RNG jumper).

C4 BASIC - The C4 BASIC language from VersaLogic includes the AIN statement specifically for the AIN-1 board. It is used as follows:

```
100 REM reads channel 4 (at hex port 30) and scale to an actual voltage
110 V=AIN(&30,4) / 2

200 REM a subroutine to read any channel X and return a value in V
210 V=AIN(&30,X) : RETURN
```

Microsoft BASIC - The popular Microsoft BASIC language is available for a number of machines and is used below to demonstrate a typical AIN-1 interface routine in BASIC.

```
100 X=4 : GOSUB 500 : REM read channel 4
 .
 .
500 REM a subroutine to read any channel X and return a value in V
510 OUT(48,X) : S=1 : REM select channel and setup sign flag
520 V = INP(49) : REM get high data byte
530 IF V > 127 THEN GOTO 520 : REM wait 'till data ready
540 IF V > 63  THEN S=-1 : V=V-64 : REM check sign bit
550 IF V > 31  THEN V=9999999 * S : RETURN : REM Overflow/underflow
560 V = (V*256 + INP(48))*S : combine high and low data ports and sign
570 V = V / 200  : REM scale it if desired
580 RETURN
```

USE WITH ANALOG DEVICES 3B SERIES INPUT CONDITIONERS

The AIN-1 board is designed to measure relatively high level voltages and is not compatible with the millivolt outputs of thermocouples, RTDs, strain gauges, etc. These signals can be measured with the AIN-1 card after they have been amplified or "conditioned" to a standard high signal level.

One product that is ideal for this purpose is the Analog Devices 3B Series Signal Conditioning I/O Subsystem. The 3B Series Subsystem consists of a universally mountable backplane that accepts a family of plug-in modules for input and output analog signal conditioning. A variety of modules are available which are optimized for specific sensors and can include isolation, input protection, current loop interface, etc. All the modules use the same pin-out and can be "mixed and matched" on the same backplane.

The AIN-1 board is directly compatible with the 3B Series, and connects to it with a single 26 pin cable. For additional flexibility, the VersaLogic AOUT-1 board is also pin compatible with the 3B Series. In applications requiring both specialized inputs and outputs, both the AIN-1 and AOUT-1 boards may be connected to the same 3B Series backplane with a single daisy-chained cable.

To use the AIN-1 board with the 3B Series it should be jumpered for pseudo-differential input (PD pads jumpered) and ±10V range (RNG pads open). Once connected to the 3B backplane, modules used on channels 0 thru 7 may be read with the AIN-1 board. Note: The 26 pin cable connects the AIN-1 analog ground line to the 3B Series earth ground line. No further grounding connections should be made between the two units.

CALIBRATION

The AIN-1 board is supplied precalibrated and ready to operate. It is a good practice, depending on the accuracy requirements of the application, to recalibrate the board every 12 to 18 months to compensate for any component aging that has occurred. The two on-board adjustments, ZERO and SPAN, are found near the 26 pin connector at the edge of the board.

The calibration procedure requires some way to read the board and continually display the reading(s). A routine to perform this function, written in C4 BASIC, is listed below.

```
10 REM The AIN-1 address switch should be set to "1" for this test
100 For X = 0 to 7 : Print #6,AIN(&10,X), :Next X
120 Print : PAUSE 500 : GOTO 100
```

The calibration procedure is as follows:

1. Zero Adjustment
   A. Disconnect all input lines from the board.
   B. Adjust the "ZERO" pot for a "0" reading on all channels.

2. Span Adjustment
   A. Apply +9.995 volts to any channel.
   B. Adjust the "SPAN" pot for a reading of 1999 (7CF hex) on the connected channel.

JUMPER OPTIONS

The jumper options for the AIN-1 board are as follows.

Name - Description

DIF - Jumper for differential input mode operation.
SE - Jumper for single-ended input mode operation.
PD - Jumper for pseudo-differential input mode operation.
The input mode jumpers are located between U1, U2, and U3.

RNG - Range. Sets the maximum voltage input range for the board. The pads should be jumpered for a ±5V input range, or open for a ±10V input range. The RNG pads are located just below the P1 connector.

WT - Wait. Enables the hardware wait line (WAITRQ*) during data setup time when the board is accessed. Jumpering this option will hold the system processor while the AIN-1 fills the data buffers with the requested data (60us max.). If this option is used it is not necessary to read the AIN-1 boards "ready" flag. This mode is not compatible with 6800 series processors. See Software Interface: Polled / Wait Modes for more information.

A1, A2, A3 - Allows the board to be addressed to locations in addition to the ten provided by the "Address" rotary switch. The board will be selected when address lines A1-A3 are low (open) or high (jumpered). For special addressing requirements contact the factory for assistance.

IOX - Allows the board to be used in systems that include extended I/O addressing. The board may be located in either the normal (IOX open) or extended (IOX jumpered) I/O maps. Most systems will required this jumper to be open.

CL0-CL7 - Locations for optional current loop resistors on channels 0 thru 7. See the Hardware Configuration section for more information.

SPECIFICATIONS

Input Channels: Eight.

Input type: Single-ended, differential, pseudo-differential, and current loop* (jumper selectable).

Input Range: ±5 volts, ±10 volts, 4-20ma* (jumper selectable).

Input Impedance: 1 Meg. ohm.

Output Format: Signed binary.

System I/O Locations Required: Two.

Resolution: ±2000 counts (12 bits). 5mv on ±10V range, 2.5mv on ±5V range.

Access (Channel Read) Time: 60us max.

Conversion Time: 45ms/channel.**

Linearity: ±1 count.

Common Mode Voltage: ±10 volts.

Maximum Input Voltage: ±15 volts.

Common Mode Rejection: 60dB.

Temperature Coefficient:
- Span: ±50 ppm/·C of full scale.
- Zero: ±25 uV/·C.

Interface Modes: Polled or wait line synchronized.

Size: 4.5" X 6.5" X .5".

Operating Temperature: 0 to 50·C.

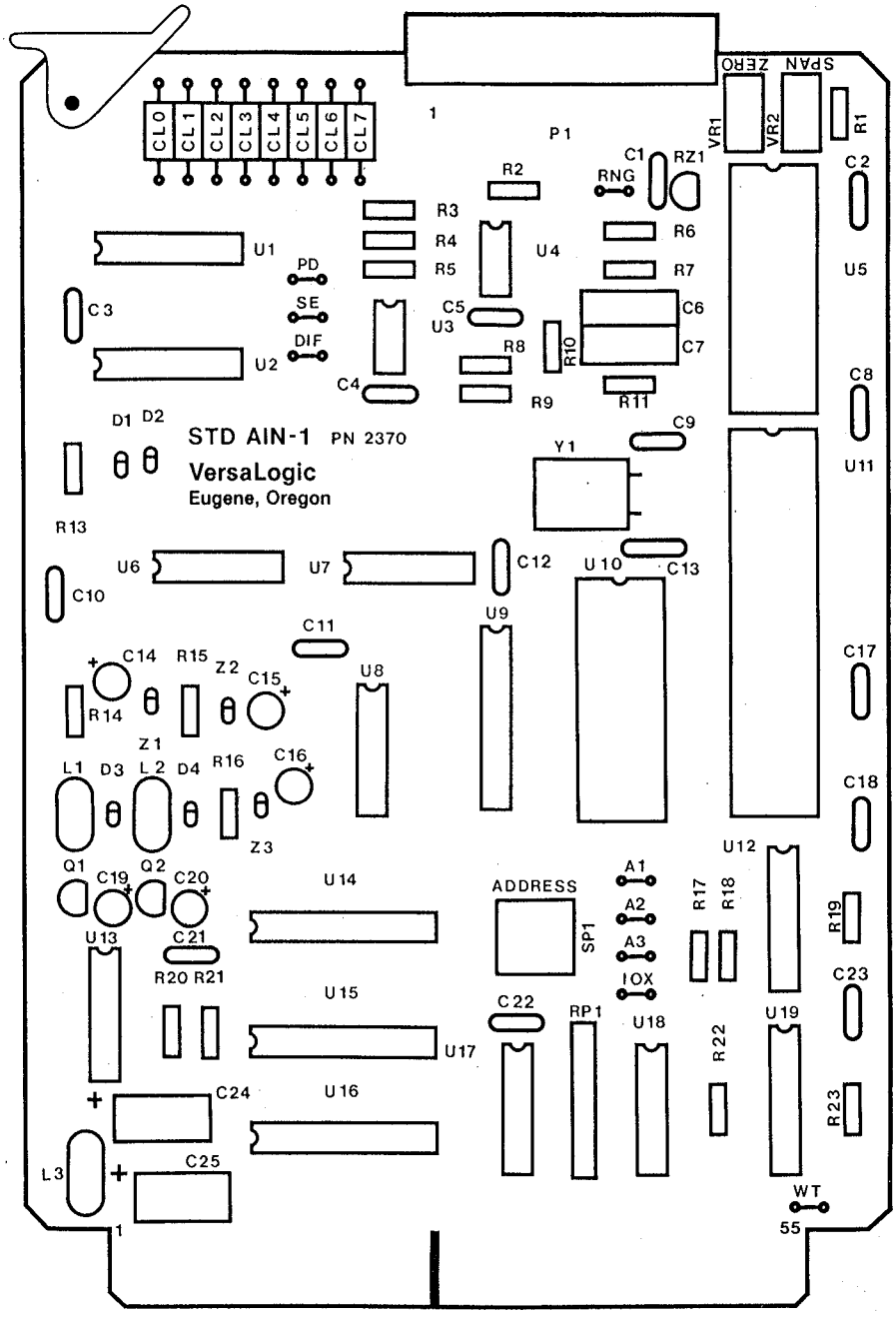
Power Requirements: +5V (±5%) at 425ma typical.

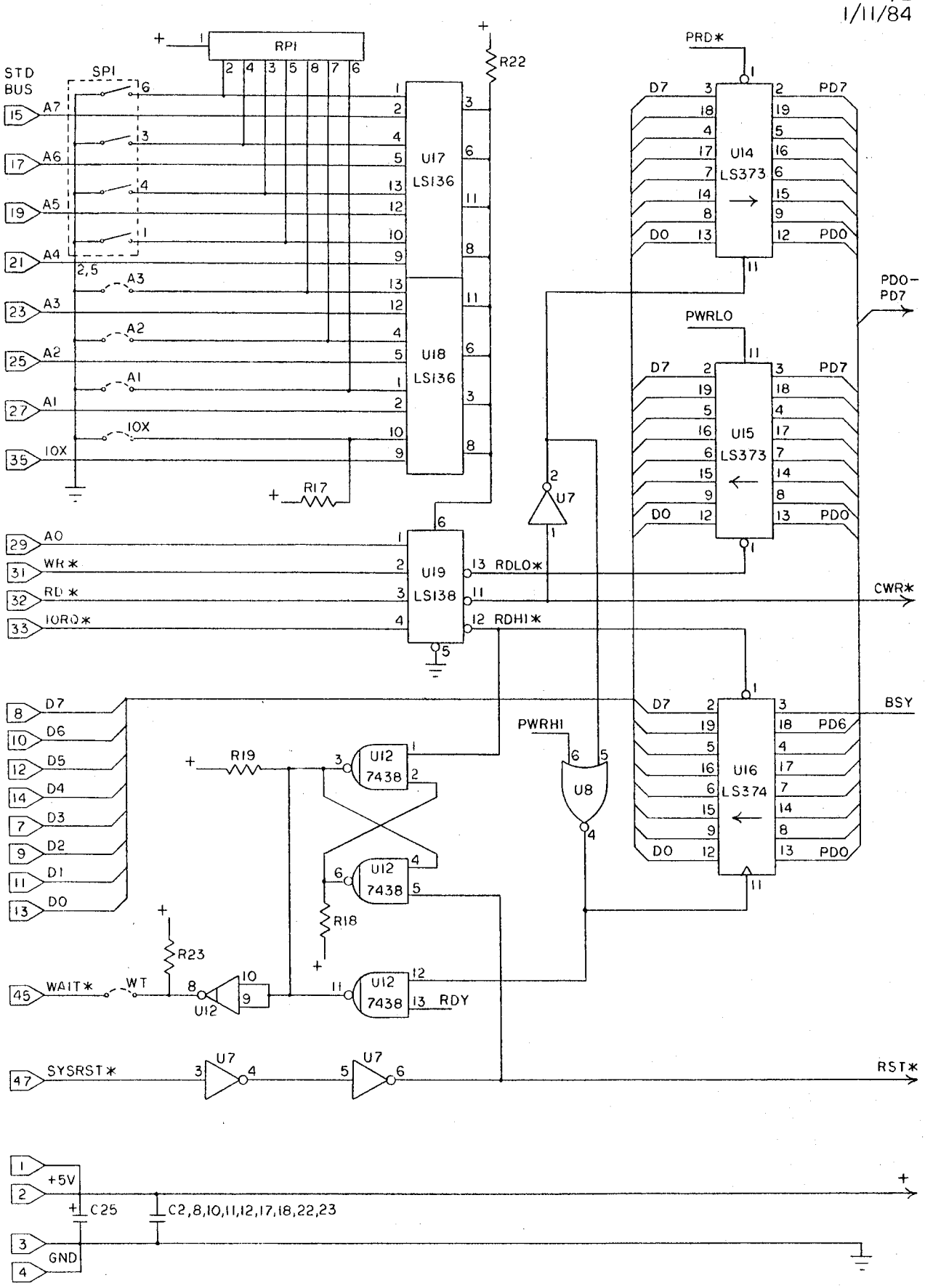
Connectors:
- STD BUS: 56 pin .125" card edge.
- Analog Input: 26 pin (dual 13) .1" header.

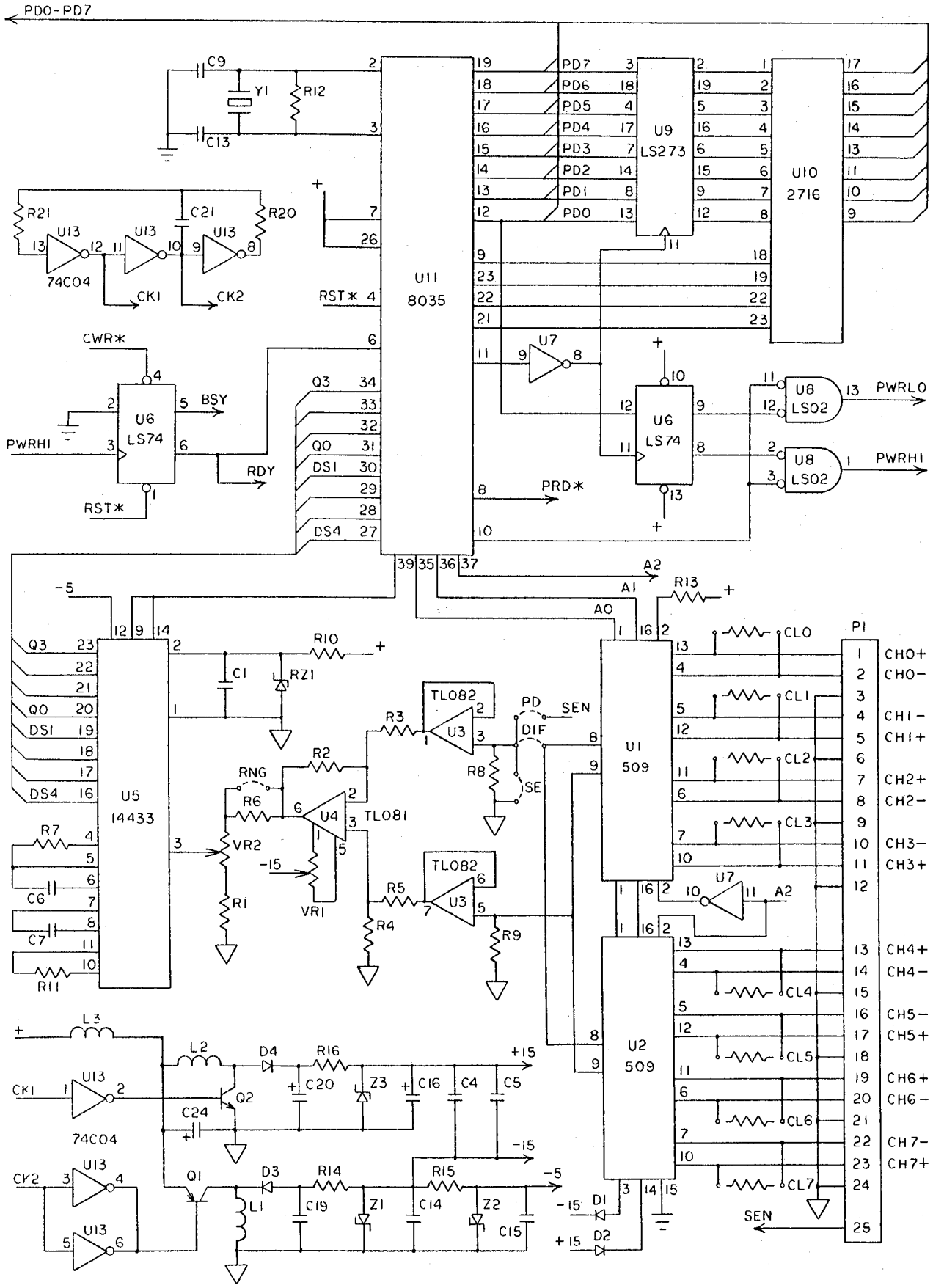
Construction: Epoxy glass PC board with solder mask and gold plated connector fingers.

Notes:
* Current loop operation requires precision resistor kit, #2670.

** 90ms if polarity change occurs. Conversion time not required for unused channels.


CL0
CL1
CL2
CL3
CL4
CL5
CL6
CL7
1
P1
SPAN
ZERO
VR1
VR2
R1
C1
RZ1
RNG
R2
R3
R4
R5
R6
R7
U1
U2
U3
U4
U5
PD
SE
DIF
C3
C4
C5
C6
C7
R8
R9
R10
R11
C2
C8
U11
D1
D2
STD AIN-1 PN 2370
VersaLogic
Eugene, Oregon
C9
Y1
R13
U6
U7
C12
U10
C13
C10
U9
C11
C14
R15
Z2
C15
U8
R14
Z1
L1
D3
L2
D4
R16
C16
Z3
C17
C18
Q1
Q2
C19
C20
U14
ADDRESS
A1
A2
A3
IOX
SP1
U12
R17
R18
R19
U13
C21
R20
R21
U15
U17
C22
RP1
U18
U19
C23
R22
R23
C24
U16
L3
C25
WT
55


RP1
SPI
STD BUS
A7
A6
A5
A4
A3
A2
A1
IOX
R22
R17
U17 LS136
U18 LS136
U7
U19 LS138
AO
WR*
RD*
IORQ*
RDLO*
RDHI*
PRD*
U14 LS373
U15 LS373
U16 LS374
PD7
PD6
PD0
PDO-PD7
PWRLO
PWRHI
CWR*
BSY
U8
U12 7438
R19
R18
R23
WAIT*
WT
RDY
SYSRST*
RST*
+5V
GND
C25
C2,8,10,11,12,17,18,22,23


PD0-PD7
C9
Y1
R12
C13
U11
8035
U9
LS273
U10
2716
R21
C21
R20
U13
74C04
CK1
CK2
RST*
CWR*
U6
LS74
BSY
RDY
PWRHI
RST*
U7
U8
LS02
PWRLO
PWRHI
PRD*
A2
A1
A0
R13
-5
U5
14433
R10
C1
RZ1
R7
C6
C7
R11
RNG
R6
R2
R3
R8
R1
R4
R5
R9
VR2
VR1
-15
TL082
TL081
U4
U3
PD
SEN
DIF
ISE
U1
509
U2
509
CL0
CL1
CL2
CL3
CL4
CL5
CL6
CL7
P1
CH0+
CH0-
CH1-
CH1+
CH2+
CH2-
CH3-
CH3+
CH4+
CH4-
CH5-
CH5+
CH6+
CH6-
CH7-
CH7+
L3
L2
D4
R16
C20
Z3
C16
C4
C5
+15
C24
Q2
Q1
D3
R14
R15
L1
C19
Z1
C14
Z2
C15
D1
D2

STD AIN-1 Parts List

7/1/84
Rev. 0.0

Capacitors

C1, C2, C3, C4, C5, C8, C10, C11, C12, C17, C18, C22, C23	.01 mf Ceramic Disk, 50V
C6, C7	.1 mf Polyester
C9	5 pf Ceramic Disk
C13	22 pf Ceramic Disk
C14, C15, C16, C19, C20	1 mf Tantalum, 35V
C21	680 pf, 5%, NPO Ceramic
C24, C25	22 mf Electrolytic, 16V

Crystals

Y1	6.000 MHz

Inductors

L1, L2	100 mH
L3	10 mH

Integrated Circuits

U1, U2	DG509
U3	TL082CP
U4	TL081CP
U5	14433
U6	LS74
U7	LS04
U8	LS02
U9	LS273
U10	2716
U11	8035

U12	7438
U13	74C04 (4069)
U14, U15	LS373
U16	LS374
U17, U18	LS136
U19	LS138

Resistors

R1, R11	47K5 ohm, 1%, Metal
R2, R4	10K ohm, 1%, Metal
R3, R5	18K2 ohm, 1%, Metal
R6	57K6 ohm, 1%, Metal
R7	121K ohm, 1%, Metal
R8, R9	1M ohm, 1%, Metal
R10	2K2 ohm, 5%, 1/4W
R13, R16, R18, R19, R21, R22	1K ohm, 5%, 1/4W
R14	390 ohm, 5%, 1/4W
R15, R20	5K6 ohm, 5%, 1/4W
R17, R23	10K ohm, 5%, 1/4W

Resistor Pack

RP1	10K, 7 Res., SIP

Semiconductors

D1, D2, D3, D4	IN4148 Diode
Q1	PN2907 Transistor
Q2	PN2222 Transistor
RZ1	LM336Z Reference
Z1, Z3	IN5245 Zener

Z2	IN751 Zener

Switch Pack

SPI	BCD Rotary

Variable Resistors

VR1	100K, 15 Turn
VR2	10K, 15 Turn

Hardware

P1	26 pin .1" right angle header
Card Ejector	CP-06
Shipping Bag	Anti-static