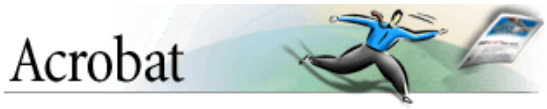

Reference Manual

VL-7806
VL-7807

Multifunction Z80 Processor
Card for the STD Bus

STD

VERSALOGIC CORPORATION

VL-7806
VL-7807

Multifunction Z80 Processor
Card for the STD Bus

M7806/7

Model VL-7806 & VL-7807

Multifunction Z80 Processor Card for the STD Bus

REFERENCE MANUAL

VL-7806 Rev. 1.00
VL-7807 Rev. 0.00
VL-78CT06 Rev. 1.00
Doc. Rev. 10/29/93

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M7806/7

Model VL-7806/7807
Multifunction Z80 Processor Card for the STD BUS

REFERENCE MANUAL

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1. Introduction

2. Installation and Configuration

3. Operation

4. Reference

VersaLogic Corporation
3888 Stewart Rd.
Eugene, OR 97402

(503) 485-8575

Section 1
INTRODUCTION

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7806 and VL-7807 Z80 processor cards.

The VL-7806 and VL-7807 cards offer identical processing and memory expansion capabilities, varying only in the on-board I/O devices that they include. The VL-7806 card is available in standard and extended temperature versions. Both the VL-7806 and VL-7807 cards are available in several different clock speeds.

This manual will refer to all these cards/versions in common, i.e. as the VL-7806/7 card. A differentiation will be made between them only when necessary.

OVERVIEW

Both the VL-7806 and VL-7807 microprocessor cards share the same features and functions, except for the type of on-board I/O ports that they include.

They feature a Z80 processor, four counter/timer channels, four 28 pin memory sockets, and two communications ports on a single STD BUS card.

The VL-7806/7 boards include a flexible memory mapping option that allows a mixture of memory devices to be accommodated. The on-board sockets can accept a wide variety of memory chips including 2 to 32K RAMs, 2 to 32K PROMs, EEPROMs, and non-volatile (zero power) RAMs. In addition, the memory expansion line (MEMEX) can be controlled by the board.

Normally one or two of the on-board timer channels are used for baud rate generation. The remaining two or three can be used as general purpose timers, external event counters, or as prioritizing interrupt inputs.

The VL-7800 cards are available in the following configurations.

VL-7806 Two RS-232 serial I/O ports.
VL-7807 One RS-232 serial I/O port and one Centronics I/O port.
VL-7842 Two RS-422 high speed serial I/O ports.

In addition to the varying I/O (communication) configurations, each of these products is available in several different speed versions (including 2.5 MHz, 3.6864 MHz, 4 MHz, and 6 MHz). The card's clock speed affects the overall thruput of the system (processing speed), as well as the communications speed (baud rates) at which the card may be operated.

FEATURES

- Fully Buffered Z80 CPU.
- Four 28 Pin JEDEC RAM/ROM Sockets.
- RS-232, RS-422, and Centronics I/O Ports.
- Three General Purpose Counter/Timers.
- MEMEX Line Supported.
- On-Board C4 BASIC Software (Optional).
- Plug-in Replacement for Pro-Log 7806/7 Boards.

SPECIFICATIONS

Size: Meets all STD BUS mechanical specifications.

Storage Temperature:
VL-7806/07: -40° to +75° C
VL-78CT06: -40° to +85° C

Free Air Operating Temperature:
VL-7806/07: 0° to +65° C
VL-78CT06: -40° to +85° C

Memory Sockets: Four 24/28 pin JEDEC compatible

Power Requirements:
VL-7806: 5V ±5% at 700 ma typ. (without on-board memory)
±12V ±10% at 35 ma typ.

VL-7807: 5V ±5% at 725 ma typ. (without on-board memory)
±12V ±10% at 18 ma typ.

VL-78CT06: 5V ±10% at 201 ma typ. (4 Mhz, without on-board memory)
±12V ±10% at 8 ma typ.

Wait State Control: Jumper selectable, op code cycle only

Reset Pulse: 35 ms typ., op code sychronized

Memory Map: 16 selectable maps (7 standard, 9 user programmable)

I/O Map: Standard (F0-F7, FD, and FE) or custom I/O mapping

CPU Clock Speed	RAM/ROM Access Speed (ns)*	Async. Baud Rates
2.5 MHz	600/450	75-38,400
3.6864 MHz	350/250	75-38,400
4.0 MHz	350/250	75-9,600
6.0 MHz	200/120	75-19,200

* shown with/without wait cycle.

Section 2
INSTALLATION AND CONFIGURATION

HANDLING

**** CAUTION **** The VL-7806/7 cards use chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

INSTALLATION

The VL-7806/7 cards can be used alone, as a single card microcomputer, or combined with other STD BUS I/O cards in an STD BUS system. When they are used with other STD BUS cards they can usually be inserted into any slot of an STD BUS card cage.

If the interrupt priority chain feature is used (supported by the VL-7806/7), cards must be inserted into the card cage according to their relative priority (usually left to right). See the Interrupt Priority Chain section for further information.

**** CAUTION **** When cards are installed in an STD BUS card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD BUS cards.

**** CAUTION **** Cards should be inserted or removed from the STD BUS card cage only when the system power is off.

EXTERNAL CONNECTIONS

Connections to the VL-7806/7 card can be made with standard cable assemblies(see Figure 2-1), or with the following mating connectors:

J1 & J2. Use 26-pin socket type connectors such as 3M #3399-7026, AMP #499505-7, or Ansley #609-2641.

J3. Use mating 2-pin socket type connectors, such as AMP #530554-1, for each interrupt/ground pair. Alternately use a single 14-pin socket type connector, such as 3M #3473-7014.

J4. Use a 2-pin socket type connector such as AMP #530554-1.

VL-7806 Connector	VersaLogic Cable P/N	Description
J1	9560 + 9553	1 foot to DB-25S + 10 foot RS-232 cable.
	or	
	9560 + 9554	1 foot to DB-25S + 25 foot RS-232 cable.
J2	Same as J1	

VL-7807 Connector	VersaLogic Cable P/N	Description
J1	9560 + 9556	1 foot to DB-25S + 6 foot Centronics cable.
J2	9560 + 9553	1 foot to DB-25S + 10 foot RS-232 cable.
	or	
	9560 + 9554	1 foot to DB-25S + 25 foot RS-232 cable.

Figure 2-1. VL-7806/7 Cable Assemblies.

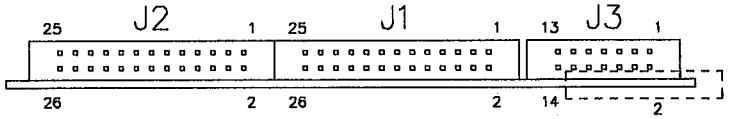


Figure 2-2. I/O Connector Physical Pin Locations

J1 / J2 Pin	Signal Name	RS-232-C Pin
1	-	1
2	-	14
3	TD	2
4	-	15
5	RD	3
6	-	16
7	RTS	4
8	-	17
9	CTS	5
10	-	18
11	DSR	6
12	-	19
13	GND	7
14	DTR	20
15	DCD	8
16	-	21
17	-	9
18	RI	22
19	-	10
20	-	23
21	-	11
22	-	24
23	-	12
24	-	25
25	-	13
26	-	-

Note: The serial port connectors can be converted to the RS-232-C pinout using VersaLogic cable #9560.

Figure 2-3. Serial Port Connector Pinout (VL-7806 J1 and J2, VL-7807 J1)

VL-7807 Connector J1	Signal Name	Centronics Connector
1	STROBE*	1
2	GND	19
3	DATA 1	2
4	GND	20
5	DATA 2	3
6	GND	21
7	DATA 3	4
8	GND	22
9	DATA 4	5
10	GND	23
11	DATA 5	6
12	GND	24
13	DATA 6	7
14	GND	25
15	DATA 7	8
16	GND	26
17	DATA 8	9
18	GND	27
19	-	10
20	GND	28
21	BUSY	11
22	GND	29
23	PE	12
24	GND	30
25	-	13
26	-	31

Note: Connector J1 can be converted to the Centronics pinout using VersaLogic cables #9560 and 9556.

Figure 2-4. Centronics Port Connector Pinout (VL-7807 J1)

J3 Pin	Signal Name	Input Load (Sink ma)	Output Drive (Sink ma)
1	GND		
2	CLOCK/ 3	1	
3	GND		
4	CLOCK/INT 2	1	
5	GND		
6	COUNT/TIME 2		2
7	GND		
8	CLOCK/INT 1	1	
9	GND		
10	COUNT/TIME 1		2
11	GND		
12	WAIT/READY* A	0.1	2
13	GND		
14	WAIT/READY* B	0.1	2

Figure 2-5. Counter/Timer Connector J3

J4 Pin	Signal Name	Input Load (Sink ma)
1	GND	
2	SEGMENT	1.3

Figure 2-6. Segment Connector / Jumper J4

OPTION JUMPERS

Various options available on the VL-7806/7 card are selected by installing or removing jumper plugs (shorting plugs) from the board as noted. "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 2-8 shows the jumper block locations on the VL-7806 board and indicates the position of the jumper plugs as shipped from the factory. Figure 2-7 (below) summerizes the jumper block functions. The VL-7807 board has jumper options similar to the VL-7806, except that it does not include jumpers V2, V3, V4, or V6.

Jumper Block	Description	As Shipped
M0-M3	Memory socket type configuration.	4-8K RAMs/ROMs
J4	Memory map select/ Segment signal connector.	IN
V1	CTC/DART clock options.	
	VL-7806 only	
	a - CTC output 1 to chan. B baud input.	a - IN
	b - CTC output 0 to chan. B baud input.	b - out
	c - SYSCKL/2 to CTC input 1.	c - IN
	VL-7807 only	
	a - SYSCLK/2 to CTC input 1.	a - out
V2-V9	Serial I/O port options. See Serial Ports.	
V10	Memory map selection. See Memory Map.	Map #0
V11	Memory socket enable/disable.	
	a - Socket M3 enabled.	a - IN
	b - Socket M2 enabled.	b - IN
	c - Socket M1 enabled.	c - IN
	d - Socket M0 enabled.	d - IN
V12	a - MEXEX is set high at power-up.[1]	a - out
	b - MEMEX is set low at power-up.	b - IN
	c - WAIT state enabled.	c - out[2]
V13	a - MEMEX signal controlled on-board.	a - IN
V14	a - IOEXP connected to ground.	a - IN
	b - AUX GND connected to digital ground.	b - IN

Notes:
1) Also inverts data written to the MEMEX control port.
2) IN on 6 MHz versions.

Figure 2-7. Jumper Functions

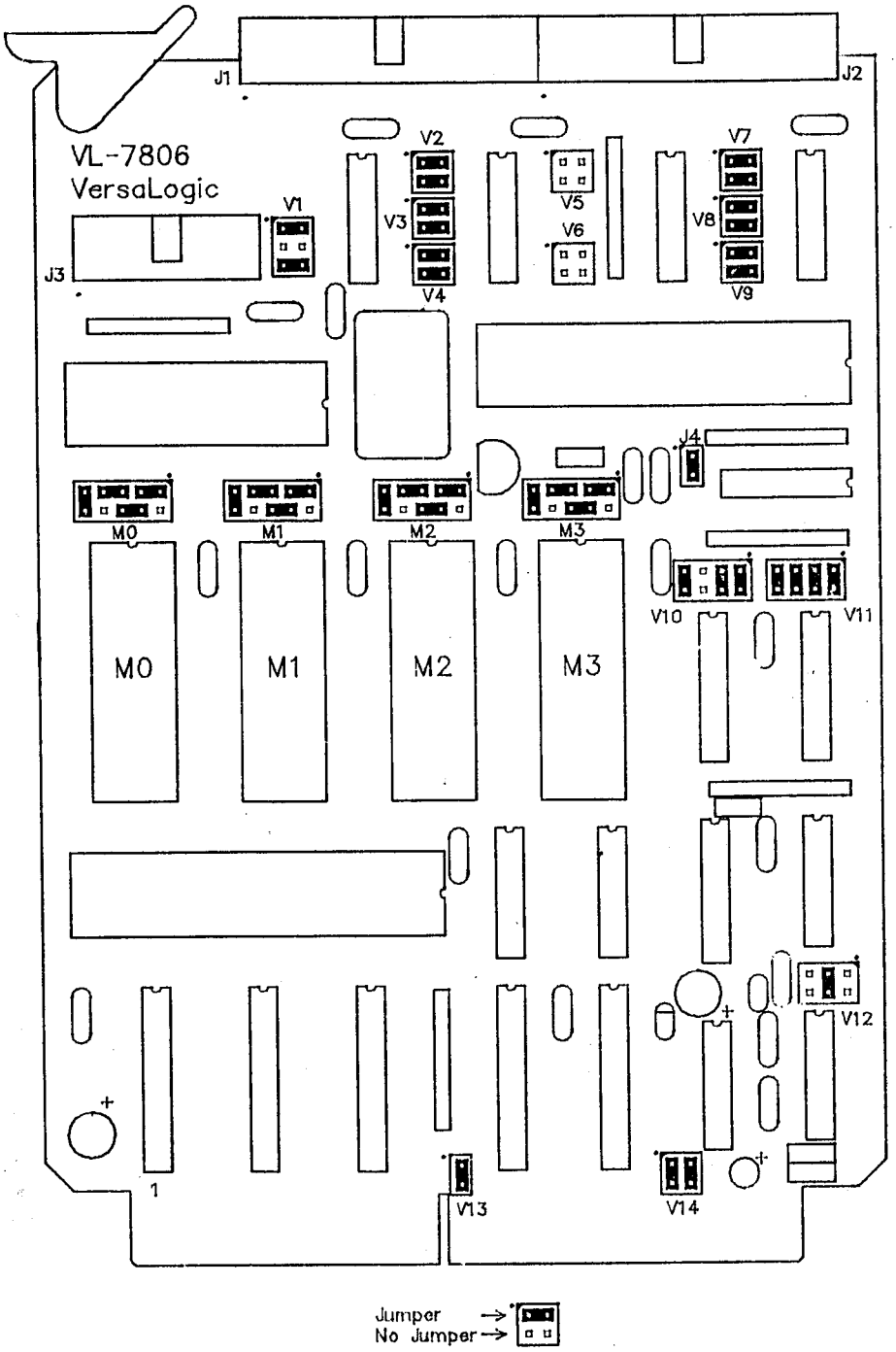


Figure 2-8. Jumper Block Locations

MEMORY

The VL-7800 cards have four on-board memory sockets. These sockets can be individually programmed (jumpered) to accept a variety of memory devices.

Installation of the on-board memory chips is accomplished in two separate steps. First, a memory map is selected that will allow each socket to be addressed at the desired memory location. Second, the jumpers for each memory socket are set to accommodate the type of chip that will be used in the socket.

Memory Map

The desired memory map is selected using jumper V10. There are various mapping combinations available in the memory decoder PROM. In addition, there are several blank (unprogrammed) options which may be programmed by the user for special applications.

Note that the memory map option only determines the memory space that is reserved for the on-board memory sockets. Whether or not the space is used by each socket, and the type of RAM or RAM which can be plugged into each socket, is determined by the memory socket jumpers (discussed later in this section).

Memory Map Selection

The desired memory map is selected using jumper plugs V10 and J4. J4 can also be used as a connector to an external "Segment select" signal for special applications.

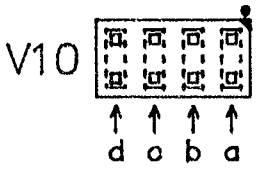
Both the MEMEX (memory expansion) and Segment signals can be used to control the currently selected memory map. However, most applications will not benefit from the use of these signals and normally they are not used.

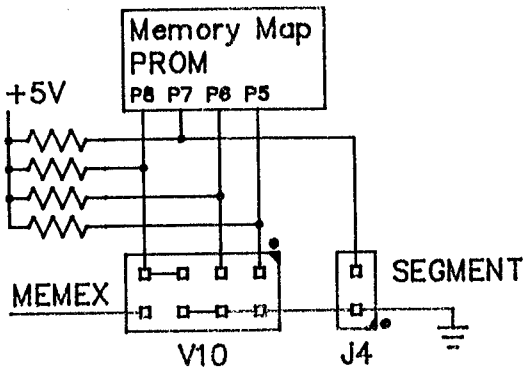
The following chart lists the standard jumper configurations used to select any of the 16 memory map options. These standard configurations ignore the state of the MEMEX and Segment signals.

Map#	Socket 0	Socket 1	Socket 2	Socket 3
0	4K 0000-0FFF	4K 1000-1FFF	4K 2000-2FFF	2K 3000-37FF
1	8K 0000-1FFF	8K 2000-3FFF	8K 4000-5FFF	8K 6000-7FFF
2	16K 0000-3FFF	16K 4000-7FFF	8K 8000-9FFF	8K A000-BFFF
3	32K 0000-7FFF	8K 8000-9FFF	8K A000-BFFF	8K C000-DFFF
4	4K 0000-0FFF	4K 1000-1FFF	4K 2000-2FFF	4K 3000-3FFF
5	16K 0000-3FFF	12K 4000-6FFF	2K 7000-77FF	2K 7800-7FFF
6	2K 0000-07FF	2K 0800-0FFF	2K 1000-17FF	2K 1800-1FFF
7*	32K 0000-7FFF	32K 8000-FFFF	-	-
8*	16K 0000-3FFF	16K 4000-7FFF	16K 8000-BFFF	16K C000-FFFF
9*	16K 0000-3FFF	32K 4000-BFFF	8K C000-DFFF	2K E000-E7FF
10*	16K 0000-3FFF	8K 4000-5FFF	8K 6000-7FFF	8K 8000-9FFF
11*	16K 0000-3FFF	32K 4000-BFFF	8K C000-DFFF	8K E000-FFFF
12*	16K 0000-3FFF	16K 4000-7FFF	32K 8000-FFFF	-
13	unprogrammed (all sockets selected)			
14	unprogrammed (all sockets selected)			
15*	32K 0000-7FFF	-	32K 8000-FFFF	-

* Available only with memory map ROM #I512X4 Vers. F.

Figure 2-9. Memory Map Options





J4	V10 d	V10 c	V10 b	V10 a	Map#
IN	-	IN	IN	IN	0
IN	-	IN	IN	-	1
IN	-	IN	-	IN	2
IN	-	IN	-	-	3
-	-	IN	IN	IN	4
-	-	IN	IN	-	5
-	-	IN	-	IN	6
-	-	IN	-	-	7
IN	-	-	IN	IN	8
IN	-	-	IN	-	9
IN	-	-	-	IN	10
IN	-	-	-	-	11
-	-	-	IN	IN	12
-	-	-	IN	-	13
-	-	-	-	IN	14
-	-	-	-	-	15

Standard Selection Method

P8	P7	P6	P5	Map#
LO	LO	LO	LO	0
LO	LO	LO	HI	1
LO	LO	HI	LO	2
LO	LO	HI	HI	3
LO	HI	LO	LO	4
LO	HI	LO	HI	5
LO	HI	HI	LO	6
LO	HI	HI	HI	7
HI	LO	LO	LO	8
HI	LO	LO	HI	9
HI	LO	HI	LO	10
HI	LO	HI	HI	11
HI	HI	LO	LO	12
HI	HI	LO	HI	13
HI	HI	HI	LO	14
HI	HI	HI	HI	15

Alternate Selection Method

Figure 2-10. Memory Map Selection

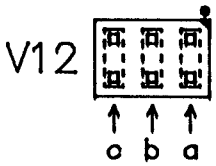
MEMEX Signal

The MEMEX (memory expansion) signal on the STD BUS is normally used to select between two different 64K byte memory banks or maps. It can be used to expand the available memory, or to control a bootstrap PROM.

The MEMEX signal can be controlled either on-board (by the VL-7806/7 card) or by another card on the bus. The MEMEX signal can also be set to a high (1) or low (0) state during system power-on. Jumpers V12 and V13 control these functions as shown in Figure 2-11.

The standard memory map selection jumpers (Figure 2-9) ignore the state of the MEMEX signal. These memory map selections may be used whether or not the MEMEX signal will be used by other cards in the system.

Alternately, the on-board memory map can change according to the state of the MEMEX signal. The jumper settings, and the resulting memory maps, can be determined using Figure 2-10.



Jumper Block	Description	As Shipped
V12	a - MEXEX is set high at power-up.[1] b - MEMEX is set low at power-up.	a - open b - IN
V13	IN - MEMEX signal controlled on-board. OUT - MEMEX signal controlled externally.	IN

Note:
1) Also inverts data written to MEMEX control port.

Figure 2-11. MEMEX Options

Segment Signal

The Segment signal is similar to MEMEX except that it is not carried by the STD BUS. This signal is generated, usually by an I/O card in the system, and externally connected to the memory (or other) cards to be controlled. The Segment signal is included on the VL-7806/7 card only for compatibility with older designs. Its use is not recommended.

To use a Segment signal with the VL-7806/7 the control cable is connected to J4. The memory maps selected, depending on the state of the Segment input, can be determined using Figure 2-10.

Memory Socket Configuration

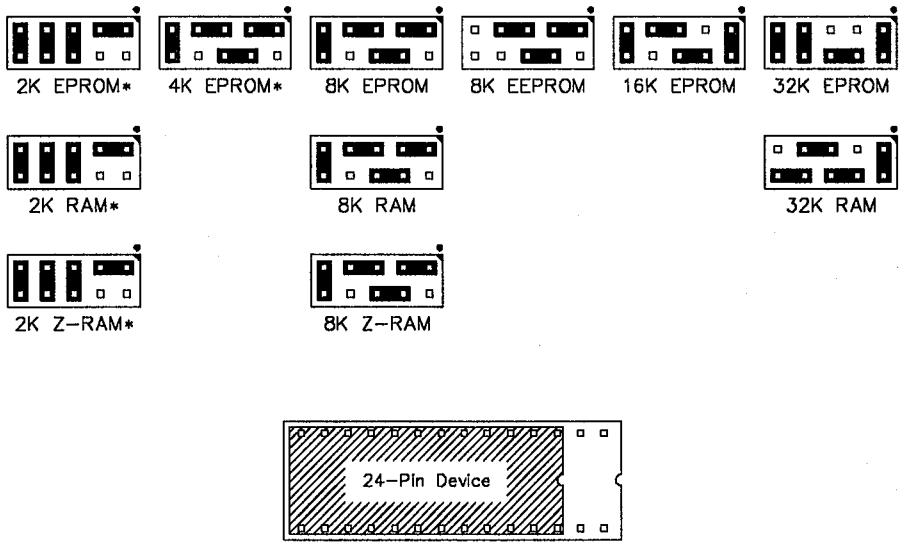
Once a memory map has been selected, each socket must be configured for the type of device that will be used in the socket. The sockets are individually configured using jumper blocks M0-M3 which are located directly above the sockets.

Refer to Figure 2-12 for selection of the appropriate jumpers for each memory device type. Jumpering is shown for EPROMs, RAMs, and Z-RAMs (Zero Power RAMs). The sockets can also accomodate standard ROMs (use EPROM jumpering) and 5V type EEPROMs (contact VersaLogic for jumper configurations).

Note that both 24 and 28 pin devices are plugged into the 28 pin sockets. Care must be taken to locate 24 pin devices at the bottom of the 28 pin socket.

Disabling Unused Sockets

Any unused socket(s) may be disabled, freeing its space in the memory map for off-board memory. Memory sockets are disabled by removing jumpers from the V11 jumper block (see Figure 2-13).



* 24 pin device. Locate in the 28 pin socket as shown.

Figure 2-12. Memory Socket Jumper Configuration

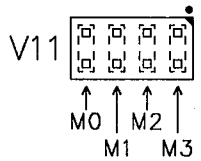


Figure 2-13. Memory Socket Enable Jumpers

I/O MAPPING

Mapping of the on-board I/O devices is controlled by a decoder PROM in location U8. The standard I/O map is shown below.

I/O Address	Port Type	Description
F0-F3	I/O	CTC channel 0-3
F4-F5	I/O	DART Channel A
F6-F7	I/O	DART Channel B
FD	OUT	Centronics Port (VL-7807 card only)
FE	OUT	MEMEX Control

Figure 2-14. I/O Port Mapping

The remaining I/O addresses, 00-EF and F8-FC, are available for use by off-board I/O devices.

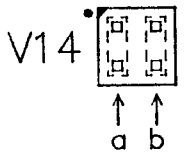
For special applications the I/O map can be altered as desired with a user programmed decoder PROM (contact VersaLogic for detailed information).

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD BUS can be used to select between two different 256 port I/O banks or maps. It is used to expand the number of available I/O ports.

The VL-7806/7 card does not control or decode the IOEXP signal. Since many I/O cards require this signal to be low on the bus, the IOEXP signal is connected to ground on the VL-7806/7.

For special applications the IOEXP signal can be disconnected from ground, allowing it to be controlled by another card in the system. To "float" the IOEXP signal, remove the jumper from position V14-a.



Jumper Block	Description	As Shipped
V14	a - IOEXP connected to ground.	a - IN
	b - AUX GND connected to digital ground.	b - IN

Figure 2-15. IOEXP and AUX GND Jumper Options

INTERRUPT PRIORITY CHAIN

The VL-7806/7 supports the STD BUS interrupt priority chain signal. This signal prioritizes system interrupts, and makes sure that only one interrupt source sends a vector address to the CPU in interrupt Mode 2. If more than one card in the system will be interrupting with Mode 2 interrupts, the priority chain must be used.

The priority chain establishes interrupt service priority based upon a card's physical position in the card cage. Cards of the highest priority should be placed in the right-most card cage slot. Note: VersaLogic and Pro-Log card cages establish priority from right to left; other card cage manufacturers may connect the priority signal from left to right.

Since the priority chain signal is passed from one slot to the next, ALL THE PRIORITIZED CARDS MUST BE IN ADJACENT SLOTS. Empty slots between cards will break the chain. Cards which do not use the priority chain (i.e. that don't use interrupts) can be placed in any of the remaining bus slots without concern for empty card slots.

SERIAL I/O PORTS

Connector Pinout

As shipped the serial I/O ports (two on the VL-7806, one on the VL-7807) are jumpered as data communications equipment (DCE) for connection to a video terminal or printer. The serial port(s) can also be jumpered as data terminal equipment (DTE) for connection to a modem or another computer.

The jumper blocks that control the serial port configuration are shown in Figure 2-16. Three standard configurations are shown along with the resulting RS-232 signal connections. For special applications jumpering refer to the VL-7806/7 schematics.

		DCE to Terminal	DTE to Modem	DTE to Computer
VL-7806/7 DART Signal		**RS-232 Signal (pin#)**		
TXD (Xmit. Data)	---->	RD(3)	TD(2)	TD(2)
RXD (Recv. Data)	<----	TD(2)	RD(3)	RD(3)
RTS (Recv. Handshake)	---->	CTS(5)	RTS(4)	RTS(4)
CTS (Xmit. Handshake)	<----	RTS(4)	CTS(5)	CTS(5)
DTR (Xmit. Eqpt. Stat.)	---->	DSR(6)	DTR(20)	DTR(20)
DCD (Recv. Eqpt. Stat.)	<----	DTR(20)	DCD(8)	DSR(6)
RI (Ring Indicator)	<----	-	RI(22)	-

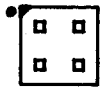
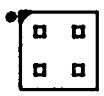
Jumper Setting for Channel A (VL-7806)	Channel B (VL-7806/7)	DCE to Terminal	DTE to Modem	DTE to Computer
V2	V7			
V3	V8			
V4	V9			
V6	V5			

Figure 2-16. Serial Port Configuration Jumpers

Baud Rate Clock, VL-7806 Only

The CTC chip contains four counter/timer channels (0 thru 3). Two of these are normally used to generate baud rate clocks for the two serial channels. The remaining two channels are available for general purpose timing/counting use.

The baud rate inputs to the DART chip are controlled by jumper block V1. Four configurations are available, depending on whether or not both serial channels will be used, and whether or not they will operate at different baud rates. As shipped, the board is jumpered for option #3.

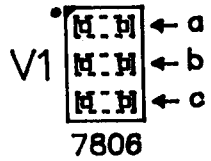
The baud rate options for the VL-7806 card are shown in Figure 2-17. They should be used as follows:

Option 1. Serial channel A is driven by CTC channel 0. Channel B is not used.

Option 2. Serial channel A and B are both driven by CTC channel 0. This frees CTC channel 1 for general purpose timing, but requires that both serial channels A and B operate at the same baud rate.

Option 3. Serial channel A is driven by CTC channel 0. Serial channel B is driven by CTC channel 1. This is the standard configuration which allows complete independence of the serial channels.

Option 4. Serial channel A is driven by CTC channel 0. Serial channel B is not used, but the system clock, divided by 2, is connected to CTC channel 1 for general purpose timing use. Note: Jumper V1c can also be added to option 2 for connection of the system clock to CTC channel 1.



	— Jumpers —			——— Resulting Connection ———			
	V1a	V1b	V1c	CTC in 0	CTC out 0	CTC in 1	CTC out 1
(1)	-	-	-	SYSCLK/2	DART A	-	-
(2)	-	IN	-	SYSCLK/2	DART A & B	-	-
(3)	IN	-	IN	SYSCLK/2	DART A	SYSCLK/2	DART B
(4)	-	-	IN	SYSCLK/2	DART A	SYSCLK/2	-

Figure 2-17. VL-7806 Baud Rate Options

Baud Rate Clock, VL-7807 Only

The CTC chip contains four counter/timer channels (0 thru 3). Channel 0 is reserved to generate a baud rate clock for serial channel B on the VL-7807 card. The remaining three channels are available for general purpose timing/counting use.

The CTC channel 0 output is hardwired to DART channel B. No jumpering is required.

Jumper V1 may be installed to connect the system clock, divided by two, to the CTC channel 1 trigger input. This allows more flexible use of CTC channel 1 in some applications but has no effect on serial port operation.

CENTRONICS PORT

The Centronics I/O port (VL-7807 only) is designed for connection to a standard data printer. Consisting of 9 output and 2 input lines, this port may also be used for TTL interfacing in special applications.

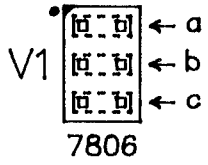
There are no jumper options associated with this port. See External Connections for connection/cabling information.

COUNTER/TIMER CHANNELS

The Counter/Timer Chip (CTC) consists of 4 timer/counter channels. Normally one (VL-7807) or two (VL-7806) of these channels are used to generate the baud rate clock for the serial I/O channel(s).

Depending on the application, on-board jumpers may be used to connect CTC inputs to the system clock, and/or connect CTC outputs to baud rate inputs on the serial I/O channel(s).

Different CTC jumper options are available on the VL-7806 and VL-7807 cards. Each is shown separately below. For additional information see the Serial I/O section.



VL-7806

Jumper	**Use**
V1a	Connects CTC output 1 to serial channel B baud input.
V1b	Connects CTC output 0 to serial channel B baud input.
V1c	Connects SYSCLK/2 to CTC input 1.

Figure 1-19. VL-7806 CTC Jumper Options.

VL-7807

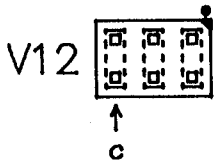
Jumper	**Use**
V1	Connects SYSCLK/2 to CTC input 1.

Figure 2-19. VL-7807 CTC Jumper Option.

WAIT STATE OPTION

The wait state jumper option allows the Z80 op code fetch cycle to be lengthened. This allows use of the VL-7806/7 card with slower memory devices without significant degradation in system processing speed. It is especially useful with the 6 MHz VL-7806/7 version.

The jumper option, and the resulting access times, are shown in Figure 2-20. As shown, a 4 MHz card operating without the wait state jumper would require RAM and ROM devices with an access time of 250 ns or better.



Jumper V12c	Minimum Access Speed 2.5 MHz	3.68 MHz	4.0 Mhz	6.0 MHz
IN	600	350	350	200
out	450	250	250	150

Figure 2-20. Wait State Option

SYSTEM GROUND

As delivered the VL-7806/7 card connects the +5V and ±12V power supply grounds together (STD BUS pins 3-4 to 53-54). Interconnection of these grounds is required whenever a serial I/O port is in use. They may also be connected together at the system power supply or on the backplane.

Special applications that require separated digital and auxiliary power supplies, and are not using an on-board serial port, may break the common ground by removing jumper V14b (see Figure 2-15).

Section 3
OPERATION

INTRODUCTION

This section includes information on the use (programming) of the various VL-7806/7 functions. Both background information and software examples are presented to assist you in constructing your own software routines.

MEMEX CONTROL

The MEMEX (memory expansion) signal on the STD BUS is normally used to select between two different 64K byte memory banks or maps. It can be used to expand the available memory, or to control a bootstrap PROM.

Memory cards in the system can choose to operate with MEMEX low (standard map), MEMEX high (secondary map), or ignore MEMEX (both maps).

In order for the MEMEX signal to be controlled by the VL-7806/7 board, jumper V13 must be installed. Jumper V12 determines the state of MEMEX at power-up and whether data is inverted when written to the MEMEX control port. The effect of the V12 jumper is shown in Figure 3-1.

The MEMEX signal is controlled by bit 0 at I/O port FE. Writing a 0 or 1 to this port will set MEMEX low or high depending on the setting of jumper V12.

Note that the routine that controls (changes) the state of MEMEX must be located in shared or common memory. That is, it must be in a section of memory (RAM or ROM) that is selected both when MEMEX is low and when MEMEX is high. If the switching routine is not resident in both memory maps, the system will crash when MEMEX is changed.

Figure 3-2 shows the typical code used to control the MEMEX signal (when jumper V12a is out and V12b is in).

Jumper V12 Description	MEMEX Port	As Shipped
a - MEXEX is set high at power-up.	Inverted	a - out
b - MEMEX is set low at power-up.	True	b - IN

Figure 3-1. MEMEX Jumper Options

```
                    ;Select secondary memory area routine
0100   3E 01       SELSEC LD       A,01H           ;
0102   D3 FE              OUT      (0FEH),A        ;Output 01H to MEMEX port
0104   C9                 RET
                    ;
                    ;Select primary memory area routine
0105   3E 00       SELPRI LD       A,00H           ;
0107   D3 FE              OUT      (0FEH),A        ;Output 00H to MEMEX port
0109   C9                 RET
```

Figure 3-2. MEMEX Software Example

COUNTER/TIMER CHIP (CTC)

The Counter/Timer Chip (CTC) can be used to count external events, measure pulse widths, and generate timed output pulses. Programmable options allow selection of external or on-board triggering, rising or falling edge triggering, prescaling, and Mode 2 interrupts at countdown completion. The CTC can also be used to generate prioritized vectored interrupts from three external inputs. The CTC supports the priority interrupt chain.

The CTC consists of four timer/counter channels. Normally one (VL-7807) or two (VL-7806) of the channels are used to generate the baud rate clock(s) for the serial I/O channel(s). This leaves two or three channels available for general purpose use. The number of available channels/functions is shown in Figure 3-3. The four channels are numbered 0 through 3.

	---- Baud Clocks Used ----		
	2 Baud Clocks	1 Baud Clock	No Baud Clocks
Function	**--- Channels Available ---**		
Timers	2,3	1,2,3	0,1,2,3
Inputs (for counting or interrupts)	2,3	1,2,3	1,2,3
Output Lines (for output pulses)	2	1,2	1,2

Figure 3-3. CTC Channels available

Internally each CTC channel has three registers- Load (initial count), Current Count, and Control. In addition, there is a vector register which is accessed through channel 0. All registers are 8 bits wide.

The Control and Current Count registers can be accessed directly by the processor. The Load registers are written after setting the required bit in a Control register. The Vector register is written directly using a special bit in the channel 0 control register. The port addresses for these registers are shown in Figure 3-4.

I/O Port	Write (OUT)	Read (IN)
F0	Chan. 0 Control, Load & Vector	Chan. 0 Current Count
F1	Chan. 1 Control and Load	Chan. 1 Current Count
F2	Chan. 2 Control and Load	Chan. 2 Current Count
F3	Chan. 3 Control and Load	Chan. 3 Current Count

Figure 3-4. CTC Register Addresses

CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
ENABLE INTPS.	COUNTER/ TIMER	CLOCK DIVIDER	CLOCK EDGE	TRIGGER	LOAD REG.	CHANNEL RESET	VECTOR LOAD

Bit Description

D7 1=Enable Interrupts

D6 0=Timer Mode
1=Counter Mode

D5* 0=Clock divided by 16
1=Clock divided by 256

D4 0=External trigger is falling edge sensitive
1=External trigger is rising edge sensitive

D3* 0=Timer starts when loaded
1=Timer starts from external trigger

D2 1=Next byte to this channel goes to the LOAD register

D1 1=Reset (stop) counter (until registers are reloaded)

D0 0=Vector register write (illegal except to channel 0)
1=Normal register access (must be 1 except for channel 0)

* Timer mode only.

Figure 3-5. CTC Control Registers

Control Register

The control register for each of the four channels is identical. Figure 3-5 shows the function of each data bit in the register.

D7 - Enable Interrupts: Allows an interrupt to be generated whenever the counter reaches zero.

D6 - Counter/Timer: Selects the counter mode or the timer mode.

D5 - Clock Divider: Divides the main CTC clock input by 16 or 256. Applies to the timer mode only.

D4 - Clock Edge: Selects rising or falling edge triggering from the external input.

D3 - Trigger: Starts timer from an external pulse, or whenever the Load register is written to. Applies to the timer mode only.

D2 - Load Register Control: Allows the next byte written to be put into this channel's Load register.

D1 - Channel Reset: Stops the counter. Does not clear any registers. Does not clear other control register bits (they must be set as desired when this bit is written). Counter/timer will restart when reloaded, retriggered, etc.

D0 - Vector Load: Writes the current byte (upper 5 bits) to the Vector register (channel 0 only). This bit must be set high at all other times.

Load Register

The Load register for each channel holds the initial value for the counter. The counter automatically reloads itself from the Load register when it reaches zero. This register may be loaded with a new value without disturbing a current countdown in progress. The Load register may hold 01 thru FF(255), and 00 which yields 256 counts.

Current Count Register

The Current Count register contains the current value in the counter. It may be read at any time without affecting the current countdown in progress.

Vector Register

A single Vector register, for the entire CTC chip, exists in channel 0. It is updated by writing to the channel 0 control register with D0 set to zero. The upper part of this byte (D3-D7) is immediately written to the Vector register.

CTC Operation

Operation of the CTC is based around the counters which can be loaded with an initial value, clocked from an internal or external source, and will do something when the count decrements down to zero.

To use a channel simply write the desired bits to the control register (with D2=1) and load a value into the Load register. If interrupts are used, the Vector register must also be initialized. Once started, the Current Count register can be read at any time to determine the current progress of the countdown.

In the timer mode, the counter is decremented by the system clock (divided by 16 or 256). No external clock input is needed. Note that the timer intervals will change if the same routines are used on a CPU card with a different system clock rate.

Since the counters count down only, the value read from the Current Count register should be inverted when counting external events or measuring time intervals. Loading the channel (Load register) with hex FF, and then inverting the value read from the Current Count register (do an Exclusive OR with FF) will yield the actual count.

Output Pulses. The CTC can be used to generate output pulses of a desired frequency. The output line for each channel goes high momentarily each time the counter reaches zero. Using the timer mode, the value of the Load register and clock divider determines the output frequency.

Cascading. Channels can be cascaded together for higher counts or longer time delays. This is done by connecting the output of the first channel (in counter or timer mode), to the external input of the second channel (in counter mode). Each time the first channel reaches zero, it will decrement the count in the second channel.

Software Trigger. Once a channel has been initialized, it can be triggered directly by the CPU if desired. In the timer mode the counter can be started by the processor. In the counter mode, the processor can decrement the counter by one. This is performed by writing to the control register of the desired channel, with the clock edge bit (D4) complemented from the last setting. This acts as a pulse, just as a change in polarity of the external input, and will start the timer or decrement the counter.

Interrupts. The CTC interrupts can only be used in the Z80 interrupt mode 2. The CTC Vector register must be initialized before interrupts are enabled from any CTC channel. The vector value generated by each counter channel is shown in Figure 3-16.

Note that the CTC can also be used as an external interrupt prioritizer. Putting a channel(s) in the counter mode, with a count of one in the Load register, will cause an interrupt every time the desired transition occurs on an external input line.

Care should be taken when disabling a CTC interrupt. It is possible to disable an interrupt while it is in progress (after the interrupt has

occurred and before the vector has been given to the processor). To avoid this possibility the following procedure should be followed whenever a CTC interrupt is disabled: Disable Z80 interrupts, disable CTC interrupt(s), re-enable Z80 interrupts.

The Z80 Return From Interrupt command should always be used at the end of your interrupt service routines. This re-enables the interrupt priority chain.

On-Board Connections. On-board jumpers may be used to connect CTC inputs to the system clock (divided by 2), and/or connect CTC outputs to baud rate inputs on the serial I/O channel(s).

Different CTC jumper options are available on the VL-7806 and VL-7807 cards. Each is shown separately below. For additional information see the Option Jumpers and Serial I/O sections.

Jumper	Use
V1a	Connects CTC output 1 to serial channel B baud input.
V1b	Connects CTC output 0 to serial channel B baud input.
V1c	Connects SYSCLK/2 to CTC input 1.

Figure 3-6. VL-7806 CTC jumper options.

Jumper	Use
V1	Connects SYSCLK/2 to CTC input 1.

Figure 3-7. VL-7807 CTC jumper option.

Timing Notes. Detailed timing for the CTC can be found in the Zilog Z8430A and Mostek MK3882-4 data sheets. Several general points are noted below.

- The zero state does not require an additional clock pulse. With a Load register of "4" the countdown would be 4, 3, 2, 1, 4, 3, ...

- The output line goes high (at zero count) for only about one system clock cycle. It does not stay high even in the counter mode.

- External trigger pulses must not be faster than one half of the system clock rate (2.5 to 6 MHz depending on the CPU version).

- External inputs must remain high or low at least 200 nanoseconds.

- If a Control register is written with the Load bit set, the timer trigger is not enabled until the Load register byte is written.

Software Example. Figure 3-8 shows a routine that uses CTC channel 3 to generate an interrupt every 1 millisecond.

```
                    ;CTC EXAMPLE
                    ;
                    ;FOR A 4.0 MHZ CARD
                    ;
          F0 00     CTC       EQU     0F0H    ;CTC base address
          F0 00     CTC0      EQU     CTC+0   ;CTC channel 0 control
          F3 00     CTC3      EQU     CTC+3   ;CTC channel 3 control
                    ;
0000                        ORG     0000H   ;Start of program
                    ;
                    ;Routine to generate an interrupt every 1ms
                    ;using CTC channel 3.  Uses mode 2 interrupts to
                    ;access interrupt service routine (SVC3)
                    ;
                    ;Load Interrupt Control Vector register with
                    ;upper 8 bits of interrupt table address
0000   3E 01        INITINT LD      A,01H           ;8 hi bits of INTSVC3
0002   ED 47                LD      I,A             ;Load CPU register
                    ;Set Z80 mode 2 interrupts
0004   ED 5E                IM      2               ;
                    ;Load CTC interrupt vector with lower 8 bits
                    ;of interrupt table address
0006   3E 20                LD      A,20H           ;8 lo bits of INTSVC3
0008   D3 F0                OUT     (CTC0),A        ;Load CTC interrupt vector
                    ;Initialize CTC to timer mode, divide system clock
                    ;by 16, with a counter value of 250.
                    ;(4MHZ/16/250 = 1KHZ)
000A   3E 85                LD      A,10000101B     ;Control data
000C   D3 F3                OUT     (CTC3),A        ;
000E   3E FA                LD      A,250           ;Count data
0010   D3 F3                OUT     (CTC3),A        ;1KHZ clock started
                    ;Enable CPU interrupts
0012   FB                   EI                      ;
0013   C9                   RET
                    ;
                    ;
                    ;Interrupt service jump address table
                    ;
0120                        ORG     120H
                    ;
0120   00 00        INTSVC0 DW      0000H   ;SVC0 = interrupt 0 routine
0122   00 00        INTSVC1 DW      0000H   ;SVC1 = interrupt 1 routine
0124   00 00        INTSVC2 DW      0000H   ;SVC2 = interrupt 2 routine
0126   50 01        INTSVC3 DW      SVC3    ;SVC3 = 1ms interrupt routine
                    ;
0150                        ORG     150H
                    ;
                    ;User supplied interrupt service routine for 1ms interrupt
0150   00           SVC3    NOP             ;USER CODE
0151   FB                   EI              ;Enable interrupts
0152   ED 4D                RETI            ;Return from interrupt
                    ;
```

Figure 3-8. CTC Software Example

DART CHIP

The serial I/O port(s) and the handshaking lines for the Centronics port (VL-7807) are both implemented with a DART (Dual Asynchronous Receiver/Transmitter) chip. General operation of the DART chip is discussed here, while its specific use on the VL-7806 or VL-7807 card is detailed in later sections.

Internal Structure

The DART chip includes two independent channels, channels A and B. Both channels are identical in structure and operation (except for the interrupt vector which is set in channel B and is common to both channels). Each DART channel has 11 registers. Four of these can be directly read/written by the processor. The remainder are accessed by setting pointer bits in the control 0 register.

A list of the DART's registers is shown in Figure 3-9. The detailed functions of these registers are shown in Figure 3-10. Each register is discussed in detail below.

I/O Port	Write (OUT)	Read (IN)
F4	Chan. A XMT data	Chan. A RCV data
F5	Chan. A Control Reg. 0	Chan. A Status Reg. 0
F6	Chan. B XMT data	Chan. B RCV data
F7	Chan. B Control Reg. 0	Chan. B Status Reg. 0

Figure 3-9. DART I/O Port Locations

Name	Use	Access
XMT	Data to transmit	I/O port
Control 0	Commands and other register access	I/O port
Control 1	Interrupt control	Via Control 0
Control 2	Interrupt vector set (chan B only)	Via Control 0
Control 3	Receiver control	Via Control 0
Control 4	Clock and word control	Via Control 0
Control 5	Transmitter control	Via Control 0
RCV	Data received	I/O port
Status 0	Ready/busy bits	I/O port
Status 1	Receive error flags	Via Control 0
Status 2	Interrupt vector read (chan B only)	Via Control 0

Figure 3-10. DART Registers

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
CNTL 0	-	-	------COMMANDS[e]----			---REGISTER SELECT---		
CNTL 1	WT/RDY ENABLE	±READY SELECT	WT/RDY ON RCV	RCV INT MODE[p]		VECTOR MODE[b,q]	XMT INT	HNDSHK INT
CNTL 2	----------INTERRUPT VECTOR (WRITE)[b]----------							
CNTL 3	---RCV CHAR--- LENGTH[k]		AUTO HNDSHK	-	-	-	-	RCV ENABLE
CNTL 4	CLOCK DIVIDER[m]		-	-	-STOP BITS[c]		EVEN PARITY	PARITY ENABLE
CNTL 5	DTR CNTL	---XMT CHAR--- LENGTH[k]		SEND BREAK	XMTR ENABLE	-	RTS CNTL	-
STAT 0	LINE[r] BREAK	-	CTS[r]	RI[r]	DCD[r]	XMT BUF. EMPTY	INT[a] PEND.	CHAR RCVD
STAT 1	-	FRAMING ERROR	OVERRUN ERROR	PARITY ERROR	-	-	-	XMTR DONE
STAT 2	----------INTERRUPT VECTOR (READ)[b,q]----------							

[a] Channel A only.
[b] Channel B only.

[e] 000 No operation
001 Invalid
010 Reset handshake INT
011 Channel reset
100 Enable INT on next char RCVD
101 Reset XMT INT
110 Error reset
111 Return from INT[b]

[p] 00 RCVR INT disable
01 RCVR INT on first char.
10 RCVR INT on every char., parity affects vector
11 RCVR INT on every char., parity doesn't affect vector

[k] 00 5 bits/char.
01 7 bits/char.
10 6 bits/char.
11 8 bits/char.

[m] 00 Invalid for async. use
01 Clock divided by 16
10 Clock divided by 32
11 Clock divided by 64

[c] 00 Invalid
01 1 stop bit
10 1 1/2 stop bits
11 2 stop bits

[q] INT vector will be modified as follows if D2 in CNTL 1 is set.

D3	D2	D1[b]	
0	0	0	Chan B XMT buffer empty
0	0	1	Chan B Handshake change
0	1	0	Chan B RCVD char. ready
0	1	1	Chan B Special RCV condition
1	0	0	Chan A XMT buffer empty
1	0	1	Chan A Handshake change
1	1	0	Chan A RCVD char. ready
1	1	1	Chan A Special RCV condition

[r] A "handshake interrupt" signal

Figure 3-11. DART Register Functions

RCV Register

The RCV register holds the data that has been received at the serial input port (RS-232 interface). It can be read directly by the processor.

The RCV register is triple buffered so that several characters can be received without the processor reading them immediately. Note however that the Status 1 register is always valid for the data currently in the RCV register. Once the RCV register is read, the next byte of received data (if any) is made available, and the Status 1 register is updated for the new byte in the RCV register. The Status 1 register should always be read first, before the data in the RCV register is read, or it will be lost.

In the receiver interrupt mode (see the Control 1 register) an error (in Stat. 1 register) will freeze both data and status registers until an error reset is executed (see Cntl. 0 register).

Note that if less than 8 data bits are being received the unused upper bit(s) will contain garbage. The unused bit positions should be cleared (with an AND command) before the data is processed.

XMT Register

The XMT register holds data to be transmitted by the channel. It is directly addressable by the processor. The XMT register is buffered, allowing the next character to be written while the current one is being transmitted.

An interrupt and/or flag (in the Status 0 register) indicates when the buffer is available to accept another character. The Status 1 register contains a flag that indicates when the actual transmitting has been completed.

Control 0 Register

The Control 0 register serves two functions. It executes special commands (as noted below), and its register pointer bits (D2-D0) allow other registers (Cntl. 1-5 and Stat. 1-2) to be accessed. It is directly addressable by the processor.

Access to most DART registers requires two writes to the DART chip. The first write sets the register pointer bits in the Cntl. 0 register. The second write contains data which is directed to the selected register. The second write is replaced by a read in the case of the status registers.

Special commands which are written to the Control 0 register are executed immediately. Register pointer bits can be included with most commands, in which case the next data byte written will be directed to the selected register. The special commands are described below.

No Operation. This command is used when the pointer register is being set and no other effect is desired.

Reset Handshake INT. If an incoming handshake line changes state, or a break or end of break is detected, bits 3, 4, 5, and 7 in Stat. 0 become frozen (and an interrupt is generated if enabled by Cntl. 1, bit 0). Until the Reset Handshake INT command is executed these bits will not change, and no further interrupts can be caused by them. If the command is executed and the status of external lines has changed, the bits are updated (with an interrupt if enabled) and then frozen once again.

Channel Reset. This command resets a single channel of the DART, as if a system reset had occurred. On Channel A it also resets the prioritization logic. All control registers must be reinitialized before the channel is used again. A delay of four clock states (i.e. one Z80 NOP instruction) must occur before the channel is written to again. Since this command clears the Control 0 register, the pointer bits cannot be set along with this command.

Enable INT On Next Character RCVD. If an "Interrupt on Received Character" mode is selected (Control 1, D4-D3) it must be re-enabled after each interrupt (by executing this command).

Reset XMT INT. This command resets a transmitter interrupt that occurs after the last character in a group has been sent (when you have no more characters to transmit). When additional characters are sent the XMT Buffer Empty interrupt (vector) will occur again (assuming the interrupt is enabled).

Error Reset. The Parity Error and Overrun flags are latching to allow their examination at the end of a block transfer. This command clears these flags.

Return From INT. This command has the same effect as a return-from-interrupt command performed by the processor. This command can only be issued to Channel A, but affects both DART channels by resetting the interrupt-under-service latch, allowing lower priority devices to interrupt.

Control 1 Register

This register is used for control of interrupts, and for controlling use (if any) of the Wait/Ready lines on the DART. The Wait/Ready lines can be used to control block transfers of data from/to the DART. Note that the VL-7806/7 board makes the Wait/Ready signals available on connector J3, but they must be externally connected (to the CPU wait line, or a DMA controller interface) before it is used. The Control 1 register is accessed via the Channel 0 register.

D7 - Wait/Ready Enable: The DART Wait/Ready line remains high (in the Ready mode) or floating (in the Wait mode) until it is enabled by setting this bit high.

D6 - ±Ready Select: Setting this bit high puts the Wait/Ready line into the Ready mode, while setting it low keeps it in the Wait mode. In the Ready mode, the Wait/Ready line (for the applicable channel) goes high whenever the receiver or transmitter needs service. In the Wait mode, the line goes high whenever the processor attempts to read or write data to the DART and it is not ready to accept or supply the requested data.

D5 - Wait/Ready on RCV: Set this bit high to use the Wait/Ready line for RCVR control, low for XMIT control.

D4-D3 - RCVR Interrupt Mode: Selects the Receiver Interrupt mode. See Figure 3-11 for the options available. Note that the Parity Affects Vector mode will cause the Special RCV Condition vector to be used when a parity error occurs (if D2 in this register is also set high).

D2 - Vector Mode: If this bit is set (high), the interrupt vector is altered depending on the interrupt condition. Refer to Figure 3-11 for the interrupts generated. This bit can be set only in Channel B but affects the whole DART.

D1 - XMT Interrupt Enable: Setting this bit high causes interrupts (Transmit vector) to occur when the XMT data register is empty.

D0 - Handshake Interrupt Enable: Enables interrupts to occur when there are changes on the handshake lines, or the start or end of a break condition. The handshake signals are DCD, RI, and CTS (Status 0 register).

Control 2 Register

The Control 2 register is used to program the interrupt vector. It can be written only to Channel B, but affects the whole DART. Three bits of the vector are replaced by the DART during interrupts if the Vector Mode bit (Control 1, D2) is set (the original vector written to this register is not changed). Note that in order to be compatible with the Z80 interrupt scheme the lowest bit of this register must be a zero. This register is accessed via the Control 0 register.

Control 3 Register

This register contains receiver control bits, and controls the auto handshake mode. It is accessed via the Control 0 register.

D7-D6 - RCVR Character Length: Sets the data word size for receiving (selected length should not include parity bit). Refer to Figure 3-11 for the lengths available. Note that if the data word length is less than 8 bits, the upper bits will contain garbage that should be discarded (masked) by the receive routine.

D5 - Auto Handshake Enable: Setting this bit high enables the auto handshake mode. When enabled the DCD* line must be active to enable the receiver. The CTS* line must be active before the transmitter is enabled. These signals appear in the Status 0 register and can be monitored directly if desired.

D0 - RCVR Enable: Setting this bit high enables the receiver. It is normally left high.

Control 4 Register

This register controls baud rate clock division, parity, and stop bit selection. It is accessed via the Control 0 register.

D7-D6 - Clock Divider: These bits select the number by which the incoming clock (usually from the CTC) is divided. This sets the baud rate for both the receive and transmit channels (they are always the same).

D3-D2 - Stop Bits: Selects the number of stop bits to be transmitted after each character. Note: The receiver always operates with one or more stop bits.

D1 - Even Parity Select: This bit selects even parity (high) or odd parity (low). It affects both transmitter and receiver.

D0 - Parity Enable: Setting this bit high adds a parity bit to the character length. It affects both the transmitter and receiver.

Control 5 Register

This register contains transmitter and handshake controls. It is accessed via the Control 0 register. Note that the DTR and RTS handshake lines may actually be jumpered to other signal lines (DSR and CTS respectively) depending on whether the channel is in the terminal or modem configuration. The descriptions below refer to the signals as they appear at the jumper block and the card edge, not as they come out of the DART chip (inverted).

D7 - DTR Control: The DTR signal goes high or low according to the setting of this bit. This line is used as the STROBE* signal on Channel A of the VL-7807 card.

D6-D5 - XMT Character Length: Sets the data word size for the transmitter (selected length should not include parity bit).

D4 - Send Break: Setting this bit forces the transmit data pin to go low (line break condition). Data being transmitted continues to be clocked through the buffer (and is lost). The transmit line is released when this bit is reset to zero.

D3 - XMIT Enable: Setting this bit high enables the transmitter. Setting it low disables the transmitter (after any character being sent is completed).

D1 - RTS Control: Setting this bit high causes the RTS signal to go high. Setting this bit low causes RTS to go low only after the transmitter is empty.

Status 0 Register

The Status 0 register contains handshake and DART status flags. It is directly accessible by the processor. Note that the CTS, RI, and DCD handshake lines may actually be jumpered to other signal lines depending on the configuration of the on-board jumpers. The descriptions below refer to the signals as they appear at the jumper block and the card edge, not as they come out of the DART chip (inverted).

D7 - Line Break: This bit indicates that a break condition has been detected on the receive data pin. When a break occurs the Framing Error flag is also be set.

D5 - CTS Status: This bit indicates the state of the CTS input line. This bit can become latched (see the Reset Handshake Interupt command in the Control 0 register).

D4 - RI Status: This bit indicates the status of the RI (Ring Indicator) line. It can be latched like the bit above.

D3 - DCD Status: This bit indicates the status of the DCD line. It can be latched like the bit above.

D2 - XMT Buffer Empty: This bit is set whenever the XMT Data register is empty.

D1 - Interrupt Pending: This bit is high if an interrupt is pending for either channel. It can be read only from Channel A.

D0 - Character RCVD: This bit indicates that a character is available in the RCV Data register. It is reset automatically when the RCV Data register is read.

Status 1 Register

The Status 1 register contains received data error and transmitter status flags. It is accessed via the Control 0 register.

D6 - Framing Error: This bit indicates that a framing error (improper location of the stop bit) occurred in the received character.

D5 - Overrun Error: This bit indicates that an overrun error has occurred. This is caused when characters received by the DART are not read soon enough by the system processor. On error, this bit latches and remains frozen until an Error Reset command is issued to the Control 0 register.

D4 - Parity Error: This bit indicates that a parity error occurred in the received character. On error, this bit latches and remains frozen until an Error Reset command is issued to the Control 0 register.

D0 - XMTR Done: This bit indicates that the transmitter itself (not the XMT buffer) is completely done transmitting.

Status 2 Register

The Status 2 register allows the current interrupt vector to be read. It is available only on Channel B, and is accessed via the Control 0 register. If the Status Affects Interrupt bit (CNTL 1, D2) is not set, the vector, exactly as written into the Control 2 register, is read. Otherwise the vector is modified according to the interrupt pending (see Vector Mode in the Control 1 register). If no interrupt is pending, the vector is modified with D3=0, D2=1, and D1=1.

SERIAL PORTS

This section discusses actual operation of the serial channels on the VL-7806/7 card. It encompasses information presented in the last several sections. Software examples are included for typical operating modes.

Initialization

Initialization of the serial channels should occur in the following order: CTC baud rate clock start-up, DART registers 2, 4, 5, 3, and 1.

Baud Rate Clock

The baud rate clock for the DART channel(s) is usually supplied by the on-board CTC chip. The CTC outputs can be jumpered to the DART clock inputs in several different configurations. The software examples in this manual assume that they are jumpered as follows.

VL-7806 only
- V1a - IN (CTC output 1 to chan. B baud input)
- V1b - out
- V1c - IN (SYSCLK/2 to CTC input 1)

VL-7807 only
- V1a - IN (SYSCLK/2 to CTC input 1)

Initializing the baud rate clock(s) consists of writing two bytes to the CTC. The first byte sets the counter/timer mode, the clock divider rate, and the load bit (that signals that the next byte written to the CTC will go the the Load register). The second byte written is the data that determines the beginning value of each countdown sequence.

The actual values for these parameters depend on the baud rate desired, and the system clock speed. Charts detailing the values for most common baud rates are included in the Reference section at the end of this manual. Note that some baud rates are not available with certain system clock rates (e.g. 19,200 baud with a 4 MHz clock) due to these clocks not being divisible closely enough to the standard baud rate.

Examples of CTC initialization are shown in Figure 3-12 and 3-13. Note that the VL-7806 uses two CTC channels (for its two serial channels), while the VL-7807 uses only one.

DART Initialization

Initialization of the DART channel(s) is most easily accomplished with a parameter table. This table can be written to the DART with the Z80 block move instruction.

There are a number of modes in which to operate the DART. The examples show in the listings below initialize it for polled (non-interrupt)

operation. The data in the initialization table can be changed to initialize the DART for any other type of operation desired. If channel A and B will be operated with different parameters (word length, etc.) then a second table can be created for the channel B initialization data (VL-7806 only).

```
                    ; DART INITIALIZATION EXAMPLE FOR THE VL-7806 CARD
                    ;
                    ; THIS EXAMPLE IS FOR A 4.0 MHZ VERSION CARD
                    ;
        F0 00       CTC     EQU     0F0H    ;CTC base address
        F0 00       CTC0    EQU     CTC+0   ;CTC channel 0 control
        F1 00       CTC1    EQU     CTC+1   ;CTC channel 1 control
                    ;
        F4 00       DART    EQU     0F4H    ;DART base address
        F4 00       CHADATA         EQU     DART+0  ;DART CHA data
        F5 00       CHACTRL         EQU     DART+1  ;DART CHA control
        F6 00       CHBDATA         EQU     DART+2  ;DART CHB data
        F7 00       CHBCTRL         EQU     DART+3  ;DART CHB control
                    ;
0000                        ORG     0000H   ;START OF PROGRAM
                    ;
                    ;Initialize CTC output 0 (DART channel A) for 9600 Baud
0000    3E 45               LD      A,01000101B   ;(45H) Control data
0002    D3 F0               OUT     (CTC0),A      ;Write control data
0004    3E 0D               LD      A,0DH         ;Count data for 9600 Baud
0006    D3 F0               OUT     (CTC0),A      ;Write count data - DONE
                    ;
                    ;Initialize CTC output 1 (DART channel B) for 1200 Baud
0008    3E 45               LD      A,01000101B   ;(45H) Control data
000A    D3 F1               OUT     (CTC1),A      ;Write control data
000C    3E 68               LD      A,68H         ;Count data for 1200 Baud
000E    D3 F1               OUT     (CTC1),A      ;Write count data - DONE
                    ;
                    ;Initialize DART channel A
0010    0E F5               LD      C,CHACTRL     ;C = Channel A control port
0012    21 23 00            LD      HL,DARTTBL    ;HL => DART initialize data table
0015    06 0B               LD      B,11          ;B = Number of bytes in table
0017    ED B3               OTIR                  ;Write data table to Channel A
                    ;
                    ;Initialize DART channel B
0019    0E F7               LD      C,CHBCTRL     ;C = Channel B control port
001B    21 23 00            LD      HL,DARTTBL    ;HL => DART initialize data table
001E    06 0B               LD      B,11          ;B = Number of bytes in table
0020    ED B3               OTIR                  ;Write data table to Channel A
0022    C9                  RET
                    ;
0023    10          DARTTBL DEFB    10H     ;Reset handshake command
0024    30                  DEFB    30H     ;Reset error flags command
0025    18                  DEFB    18H     ;Reset channel command
0026    04                  DEFB    04H     ;Select register 4
0027    47                  DEFB    47H     ;Even parity, 1 stop bit, /16 clock
0028    05                  DEFB    05H     ;Select register 5
0029    AA                  DEFB    0AAH    ;DTR & RTS on, xmit 7 data bits, on
002A    03                  DEFB    03H     ;Select register 3
002B    41                  DEFB    41H     ;Rcv 7 data bits, on
002C    01                  DEFB    01H     ;Select register 1
002D    00                  DEFB    00H     ;No interrupts
```

Figure 3-12. VL-7806 Initialization

```
                        ; DART INITIALIZATION EXAMPLE FOR THE VL-7807 CARD
                        ;
                        ; THIS EXAMPLE IS FOR A 4.0 MHZ VERSION CARD
                        ;
        F0 00           CTC     EQU     0F0H    ;CTC base address
        F0 00           CTC0    EQU     CTC+0   ;CTC channel 0 control
                        ;
        F4 00           DART    EQU     0F4H    ;DART base address
        F6 00           CHBDATA         EQU     DART+2  ;DART CHB data
        F7 00           CHBCTRL         EQU     DART+3  ;DART CHB control
                        ;
0000                            ORG     0000H   ;START OF PROGRAM
                        ;
                        ;Initialize CTC output 0 (DART channel B) for 9600 Baud
0000    3E 45                   LD      A,01000101B     ;(45H) Control data
0002    D3 F0                   OUT     (CTC0),A        ;Write control data
0004    3E 0D                   LD      A,0DH           ;Count data for 9600 Baud
0006    D3 F0                   OUT     (CTC0),A        ;Write count data - DONE
                        ;
                        ;Initialize DART channel B
0008    0E F7                   LD      C,CHBCTRL       ;C = Channel B control port
000A    21 12 00                LD      HL,DARTTBL      ;HL => DART initialize data table
000D    06 0B                   LD      B,11            ;B = Number of bytes in table
000F    ED B3                   OTIR                    ;Write data table to Channel A
0011    C9                      RET
                        ;
0012    10              DARTTBL DEFB    10H     ;Reset handshake command
0013    30                      DEFB    30H     ;Reset error flags command
0014    18                      DEFB    18H     ;Reset channel command
0015    04                      DEFB    04H     ;Select register 4
0016    47                      DEFB    47H     ;Even parity, 1 stop bit, /16 clock
0017    05                      DEFB    05H     ;Select register 5
0018    AA                      DEFB    0AAH    ;DTR & RTS on, xmit 7 data bits, on
0019    03                      DEFB    03H     ;Select register 3
001A    41                      DEFB    41H     ;Rcv 7 data bits, on
001B    01                      DEFB    01H     ;Select register 1
001C    00                      DEFB    00H     ;No interrupts
```

Figure 3-13. VL-7807 Initialization

Handshake Signals

The serial port handshake lines are used to control the flow of data from/to the serial port. Figure 3-14 lists the handshake lines available.

Signal	Direction	Use
CTS	<-- (IN)	Transmit handshake.
DTR	--> (OUT)	Transmit equipment status.
RTS	--> (OUT)	Receiver handshake.
DCD	<-- (IN)	Receiver equipment status.
RI	<-- (IN)	Ring indicator (from modem).

Figure 3-14. Serial Port Handshake Lines

Normally the data handshake lines (CTS and RTS) are used to signal readiness to accept data. The equipment status signals (DTR and DCD) are used to indicate whether an operating (powered on) device is connected to a port. The ring indicator signal is used with a modem to indicate an incoming call.

The DART can be programmed for the automatic handshake mode using control register 3, bit D5. In this mode the transmitter and receiver are automatically enabled/disabled by the CTS and DCD signals.

If the automatic handshake mode is not used, the CTS and DCD pins should be monitored by the processor in the Status 0 register. They can also generate interrupts if handshake interrupts are enabled.

The DTR and RTS output lines are controlled by writing to the Control 5 register. The RI signal can be read in the Status 0 register and can also generate interrupts.

Polled Operation

In the polled (non-interrupt) mode, the DART status registers are read by the processor to determine when a character has been received, or if the next character can be transmitted. It is the simplest mode of DART operation since all of the I/O routine is "in line". Program operation does not depend on the correct initialization of interrupt vectors, or the proper placement of routines at those vectors. This method does require the input routine to be called frequently enough that incoming characters don't overflow the triple buffered receive data register.

Figure 3-15 shows three subroutines for polled operation. INSTAT (input status) returns a flag indicating whether there is currently a received character waiting to be read from the DART. CHARIN (character input) returns a received character or waits until one is received. CHAROUT (character output) transmits a character.

```
                        ; DART I/O EXAMPLE FOR THE VL-7806 CARD
                        ;
        F4 00           DART    EQU     0F4H    ;DART base address
        F4 00           CHADATA         EQU     DART+0  ;DART CHA data
        F5 00           CHACTRL         EQU     DART+1  ;DART CHA control
        F6 00           CHBDATA         EQU     DART+2  ;DART CHB data
        F7 00           CHBCTRL         EQU     DART+3  ;DART CHB control
                        ;
0200                            ORG     200H
                        ;
                        ;Input status routine, checks DART to see if a character is
                        ;available.  If available, returns A = FFH (Z = 0).  If not
                        ;available, returns A = 00H (Z = 1).
0200    DB F5           INSTAT IN       A,(CHACTRL)  ;Read status
0202    CB 47                   BIT     0,A          ;Bit 0 = data available
0204    28 04                   JR      Z,INSTAT1    ;No data available
0206    3E FF                   LD      A,0FFH       ;Data available, set A = FFH
0208    A7                      AND     A            ;Z = 0
0209    C9                      RET
020A    AF              INSTAT1 XOR     A            ;A = 0, Z = 1
020B    C9                      RET
                        ;
                        ;
                        ;Character input routine, waits for data and returns
                        ;character in A.
020C    DB F5           CHARIN IN       A,(CHACTRL)  ;Read status
020E    CB 47                   BIT     0,A          ;Bit 0 = data available
0210    28 FA                   JR      Z,CHARIN     ;No data, wait
0212    DB F4                   IN      A,(CHADATA)  ;Read data
0214    E6 7F                   AND     7FH          ;Mask bit 7 (Junk)
0216    C9                      RET
                        ;
                        ;
                        ;Character output routine, checks CTS line and xmits
                        ;character in C when CTS is active (RS232 > +3 Volts)
0217    3E 10           CHAROUT LD      A,10H        ;DART handshake reset data
0219    D3 F5                   OUT     (CHACTRL),A  ;Update handshake register
021B    DB F5                   IN      A,(CHACTRL)  ;Read status
021D    CB 6F                   BIT     5,A          ;Check CTS bit
021F    28 F6                   JR      Z,CHAROUT    ;Wait until CTS is active
0221    DB F5           COUT1   IN      A,(CHACTRL)  ;Read status
0223    CB 57                   BIT     2,A          ;Xmit buffer empty?
0225    28 FA                   JR      Z,COUT1      ;Wait until buffer is empty
0227    79                      LD      A,C          ;Character to A
0228    D3 F4                   OUT     (CHADATA),A  ;Output data
022A    C9                      RET
```

Figure 3-15. Polled DART Operation

Interrupt Operation

The most common mode of DART interrupt operation is with the Z80 interrupt mode 2. In this mode the vector (supplied by the interrupt source) is combined with the contents of the Z80 interrupt register to form a 16 bit vector address of the interrupt service routine.

Since the CTC can only provide Mode 2 type interrupts, you must use interrupt Mode 2 if interrupts are needed from any of the timer/counters.

When using Mode 2 interrupts you must: Set the value of the Z80 interrupt vector (for the upper byte of the interrupt vector), set the interrupt vector in the DART (for the lower byte of the interrupt vector- the lowest bit of this vector must be 0), and always use the Z80 Return From Interrupt command at the end of the interrupt service routine (to re-enable the priority chain in the DART).

Normally the vectors for the CTC and DART are selected so that a single continuous jump table can be used. Programming the DART with a vector of XO hex, and the CTC with a vector of (X+1)0 hex will result in a jump table that is 23 bytes long (40 to 46, 50 to 56, etc.).

The on-board priorities of the CTC and DART interrupts are pre-set and cannot be altered. They are listed, along with the vectors they generate, in Figure 3-16 below.

Priority	Description	Vector
1	CTC Channel 0	XXXX X000
2	CTC Channel 1	XXXX X010
3	CTC Channel 2	XXXX X100
4	CTC Channel 3	XXXX X110
	DART Chan. A	
5	RCV char.	XXXX 110X
5	Special RCV cond.	XXXX 111X
6	XMT buffer empty	XXXX 100X
7	Handshake transition	XXXX 101X
	DART Chan. B	
8	RCV char.	XXXX 010X
8	Special RCV cond.	XXXX 011X
9	XMT buffer empty	XXXX 000X
10 (lowest)	Handshake transition	XXXX 001X

Figure 3-16. On-Board Interrupt Vector Priorities

Other Interrupt Modes

Other interrupt modes can be used in special situations as noted below.

- Other cards in the system generate interrupts with 8080 type restart vectors only.

Use Z80 interrupt mode 0 and program the DART with a restart instruction for the vector. Do not use the Status Affects Vector mode. Use the Z80 Return From Interrupt command after servicing the DART.

- Other cards in the system generate interrupts but do not provide vectors.

Use Z80 interrupt mode 1. Do not use the DART's Status Affects Vector mode. Upon interrupt check the possible sources of the interrupt. Check the Interrupt Pending bit in Status 0 of the DART. If set, check the other flags in Status 0 to determine the reason. Use the Z80 Return From Interrupt command (or the Return From Interrupt command in Control 0) after servicing the DART. This re-enables the DART's priority chain.

- Interrupts are not used at all.

The DART interrupt vectors can be used if desired, even if interrupts are not actually generated to the bus. Enable the DART's Status Affects Vector mode and monitor the Interrupt Pending bit in Status 0. When it is set, read the vector (from Status 2) and use the vector to determine what service is needed. Use the Return From Interrupt command in Control 0 after servicing the DART. This re-enables the priority chain in the DART (necessary only in the Status Affect Vector mode).

Block Transfer Mode

The DART can also be used in a block transfer mode. Block transfers can occur between the DART and the CPU, or the DART and a DMA controller. The transfers are controlled by the Wait/Ready lines (channels A and B) which are accessible at connector J3 (along with the CTC signals).

This mode is normally used only where large blocks of data must be received/transmitted at very high speeds.

For CPU transfers the Wait/Ready line must be connected to the STD BUS WAITRQ* line. The Wait/Ready line is programmed for the Wait mode and left enabled while block transfers may occur. The Wait line becomes active during certain reads or writes to the DART and causes the CPU to wait until the DART can supply or accept the requested data. The Z80 block I/O transfer instructions are used to transfer blocks of up to 256 bytes of data to/from the DART. The interrupt on First Character mode should be used when receiving in the block mode. Since the Wait line is open drain, a pull-up resistor should be used in this mode.

For DMA transfers, the Wait/Ready line must be connected directly to the DMA controller. After this line is initialized for the Ready mode it will go active whenever the DART is ready to transfer another byte.

CENTRONICS PORT

The VL-7807 card includes a Centronics port for connection of standard Centronics (parallel) interface printers to the system. It can also be used as a general purpose I/O port, providing nine output lines, and two input lines.

The Centronics port may be used much like the serial ports described above (for data output) since it uses the DART handshake lines on channel A for the Centronics port control lines. A separate 8 bit data port, located at I/O address FD, is used to send data to the printer. The control lines for the port are listed below. Figure 3-18 shows the typical routines needed to initialize and output a character to this port.

DART Register	Signal	Function
CNTL 5, D7	STROBE*	Controls the STROBE* signal to the printer.
STAT 0, D5	PE	Reads the PE signal from the printer.
STAT 0, D3	BUSY	Reads the BUSY signal from the printer.

Figure 3-17. Centronics Port Control Lines

```
                        ;CENTRONICS PRINTER PORT EXAMPLES FOR THE VL-7807 CARD
                        ;
        F4 00           DART    EQU     0F4H    ;DART base address
        F5 00           CHACTRL EQU     DART+1  ;DART Chan. A control
        FD 00           PRTDATA EQU     0FDH    ;DATA latch port
                        ;
0000                            ORG     0000H
                        ;
                        ;Parallel printer initialize routine
                        ;
                        ;Reset DART channel A
0000    3E 18           PRTINIT LD      A,18H           ;Reset channel command
0002    D3 F5                   OUT     (CHACTRL),A     ;Reset channel A
                        ;Set strobe line hi (DTR CHA)
0004    3E 05                   LD      A,05H           ;Select register 5
0006    D3 F5                   OUT     (CHACTRL),A     ;
0008    3E 00                   LD      A,00H           ;Data to set DTR hi
000A    D3 F5                   OUT     (CHACTRL),A     ;
                        ;Clear data latch
000C    D3 FD                   OUT     (PRTDATA),A     ;Write 00H to latch
000E    C9                      RET
                        ;
                        ;
                        ;Parallel printer output routine, checks busy line (DCD CHA)
                        ;and paper empty line (CTS CHA).  When both are low, ASCII data
                        ;in C is output to latch and strobe line (DTR CHA) goes low
                        ;for approx. 10us.
000F    3E 10           PRTOUT  LD      A,10H           ;Handshake reset data
0011    D3 F5                   OUT     (CHACTRL),A     ;Update status register
0013    DB F5                   IN      A,(CHACTRL)     ;Read status register
0015    E6 28                   AND     28H             ;Mask all but DCD and CTS
0017    FE 28                   CP      28H             ;Both should be hi
0019    20 F4                   JR      NZ,PRTOUT       ;Wait if not
001B    79                      LD      A,C             ;OK, output to printer
001C    D3 FD                   OUT     (PRTDATA),A     ;ASCII data to latch
001E    3E 05                   LD      A,05H           ;Do strobe
0020    D3 F5                   OUT     (CHACTRL),A     ;Select register 5
0022    3E 80                   LD      A,80H           ;Data for strobe lo
0024    D3 F5                   OUT     (CHACTRL),A     ;Strobe goes lo
0026    C5                      PUSH    BC              ;Waste time
0027    C1                      POP     BC              ;
0028    3E 05                   LD      A,05H           ;
002A    D3 F5                   OUT     (CHACTRL),A     ;Select register 5
002C    3E 00                   LD      A,00H           ;Data for strobe hi
002E    D3 F5                   OUT     (CHACTRL),A     ;Strobe goes hi
0030    C9                      RET
```

Figure 3-18. Centronics Port Software Example

Section 4
REFERENCE

SPECIFICATIONS

VL-7806, VL-78CT06, and VL-7807 Multifunction Z80 CPU Cards

Size: Meets all STD BUS mechanical specifications.

Storage Temperature:
VL-7806/07: -40° to +75° C
VL-78CT06: -40° to +85° C

Free Air Operating Temperature:
VL-7806/07: 0° to +65° C
VL-78CT06: -40° to +85° C

Memory Sockets: Four 24/28 pin JEDEC compatible

Power Requirements:
VL-7806: 5V ±5% at 700 ma typ. (without on-board memory)
±12V ±10% at 35 ma typ.

VL-7807: 5V ±5% at 725 ma typ. (without on-board memory)
±12V ±10% at 18 ma typ.

VL-78CT06: 5V ±10% at 201 ma typ. (4 Mhz, without on-board memory)
±12V ±10% at 8 ma typ.

Wait State Control: Jumper selectable, op code cycle only

Reset Pulse: 35 ms typ., op code sychronized

Memory Map: 16 selectable maps (7 standard, 9 user programmable)

I/O Map: Standard (F0-F7, FD, and FE) or custom I/O mapping

CPU Clock Speed	RAM/ROM Access Speed (ns)*	Async. Baud Rates
2.5 MHz	600/450	75-38,400
3.6864 MHz	350/250	75-38,400
4.0 MHz	350/250	75-9,600
6.0 MHz	200/150	75-19,200

* shown with/without wait cycle.

JUMPER OPTIONS

Jumper Block	Description	As Shipped
M0-M3	Memory socket type configuration.	4-8K RAMs/ROMs
J4	Memory map select/ Segment signal connector.	IN
V1	CTC/DART clock options.	
	VL-7806 only	
	a - CTC output 1 to chan. B baud input.	a - IN
	b - CTC output 0 to chan. B baud input.	b - out
	c - SYSCKL/2 to CTC input 1.	c - IN
	VL-7807 only	
	a - SYSCLK/2 to CTC input 1.	a - out
V2-V9	Serial I/O port options. See Serial Ports.	
V10	Memory map selection. See Memory Map.	Map #0
V11	Memory socket enable/disable.	
	a - Socket M3 enabled.	a - IN
	b - Socket M2 enabled.	b - IN
	c - Socket M1 enabled.	c - IN
	d - Socket M0 enabled.	d - IN
V12	a - MEXEX is set high at power-up.[1]	a - out
	b - MEMEX is set low at power-up.	b - IN
	c - WAIT state enabled.	c - out[2]
V13	a - MEMEX signal controlled on-board.	a - IN
V14	a - IOEXP connected to ground.	a - IN
	b - AUX GND connected to digital ground.	b - IN

Notes:
1) Also inverts data written to the MEMEX control port.
2) IN on 6 MHz versions.

Jumper Functions

I/O MAP

I/O Address	Port Type	Description
F0-F3	I/O	CTC channel 0-3
F4-F5	I/O	DART Channel A
F6-F7	I/O	DART Channel B
FD	OUT	Centronics Port (VL-7807 card only)
FE	OUT	MEMEX Control

I/O Port Mapping

INTERRUPT VECTORS

Priority	Description	Vector
1	CTC Channel 0	XXXX X000
2	CTC Channel 1	XXXX X010
3	CTC Channel 2	XXXX X100
4	CTC Channel 3	XXXX X110
	DART Chan. A	
5	RCV char.	XXXX 110X
5	Special RCV cond.	XXXX 111X
6	XMT buffer empty	XXXX 100X
7	Handshake transition	XXXX 101X
	DART Chan. B	
8	RCV char.	XXXX 010X
8	Special RCV cond.	XXXX 011X
9	XMT buffer empty	XXXX 000X
10 (lowest)	Handshake transition	XXXX 001X

Interrupt Vectors

CTC INFORMATION

Port	Write (OUT)	Read (IN)
F0	Chan. 0 Control, Load & Vector.	Chan. 0 Current Count.
F1	Chan. 1 Control and Load.	Chan. 1 Current Count.
F2	Chan. 2 Control and Load.	Chan. 2 Current Count.
F3	Chan. 3 Control and Load.	Chan. 3 Current Count.

CTC Register Addresses

CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
ENABLE INTPS.	COUNTER/ TIMER	CLOCK DIVIDER	CLOCK EDGE	TRIGGER	LOAD REG.	CHANNEL RESET	VECTOR LOAD

Bit Description

D7 1=Enable Interrupts

D6 0=Timer Mode
1=Counter Mode

D5* 0=Clock divided by 16
1=Clock divided by 256

D4 0=External trigger is falling edge sensitive
1=External trigger is rising edge sensitive

D3* 0=Timer starts when loaded
1=Timer starts from external trigger

D2 1=Next byte to this channel goes to the LOAD register

D1 1=Reset (stop) counter (until registers are re-loaded)

D0 0=Vector register write (illegal except to channel 0)
1=Normal register access (must be 1 except for channel 0)

* Timer mode only.

CTC Control Registers

DART INFORMATION

I/O Port	Write (OUT)	Read (IN)
F4	Chan. A XMT data	Chan. A RCV data
F5	Chan. A Control Reg. 0	Chan. A Status Reg. 0
F6	Chan. B XMT data	Chan. B RCV data
F7	Chan. B Control Reg. 0	Chan. B Status Reg. 0

DART I/O Port Locations

Name	Use	Access
XMT	Data to transmit	I/O port
Control 0	Commands and other register access	I/O port
Control 1	Interrupt control	Via Control 0
Control 2	Interrupt vector set (chan B only)	Via Control 0
Control 3	Receiver control	Via Control 0
Control 4	Clock and word control	Via Control 0
Control 5	Transmitter control	Via Control 0
RCV	Data received	I/O port
Status 0	Ready/busy bits	I/O port
Status 1	Receive error flags	Via Control 0
Status 2	Interrupt vector read (chan B only)	Via Control 0

DART Registers

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
CNTL 0	-	-	-------COMMANDS[e]----			---REGISTER SELECT---		
CNTL 1	WT/RDY ENABLE	±READY SELECT	WT/RDY ON RCV	RCV INT MODE[p]		VECTOR MODE[b,q]	XMT INT	HNDSHK INT
CNTL 2	----------INTERRUPT VECTOR (WRITE)[b]----------							
CNTL 3	---RCV CHAR--- LENGTH[k]		AUTO HNDSHK	-	-	-	-	RCV ENABLE
CNTL 4	CLOCK DIVIDER[m]		-	-	-STOP BITS[c]		EVEN PARITY	PARITY ENABLE
CNTL 5	DTR CNTL	---XMT CHAR--- LENGTH[k]		SEND BREAK	XMTR ENABLE	-	RTS CNTL	-
STAT 0	LINE[r] BREAK	-	CTS[r]	RI[r]	DCD[r]	XMT BUF. EMPTY	INT[a] PEND.	CHAR RCVD
STAT 1	-	FRAMING ERROR	OVERRUN ERROR	PARITY ERROR	-	-	-	XMTR DONE
STAT 2	----------INTERRUPT VECTOR (READ)[b,q]----------							

[a] Channel A only.
[b] Channel B only.

[e] 000 No operation
001 Invalid
010 Reset handshake INT
011 Channel reset
100 Enable INT on next char RCVD
101 Reset XMT INT
110 Error reset
111 Return from INT[b]

[p] 00 RCVR INT disable
01 RCVR INT on first char.
10 RCVR INT on every char., parity affects vector
11 RCVR INT on every char., parity doesn't affect vector

[k] 00 5 bits/char.
01 7 bits/char.
10 6 bits/char.
11 8 bits/char.

[m] 00 Invalid for async. use
01 Clock divided by 16
10 Clock divided by 32
11 Clock divided by 64

[c] 00 Invalid
01 1 stop bit
10 1 1/2 stop bits
11 2 stop bits

[q] INT vector will be modified as follows if D2 in CNTL 1 is set.

D3	D2	D1[b]	
0	0	0	Chan B XMT buffer empty
0	0	1	Chan B Handshake change
0	1	0	Chan B RCVD char. ready
0	1	1	Chan B Special RCV condition
1	0	0	Chan A XMT buffer empty
1	0	1	Chan A Handshake change
1	1	0	Chan A RCVD char. ready
1	1	1	Chan A Special RCV condition

[r] A "handshake interrupt" signal

DART Register Functions

BAUD RATE TABLES

The data required to program the CTC and DART for common baud rates is shown below. The baud rate used by the DART chip can also be determined as follows (7806/7 card only):

CTC in Counter Mode: Baud rate = system clock/2/16/count
CTC in Timer Mode: Baud rate = system clock/2/16/16/count

2.5 MHz Clock

Baud Rate	CTC Divider	Count Hex	Count Decimal	CTC Mode	DART Divider	Baud Rate Error (%)
38.4K	1	02	2	Counter	16	+1.72
19.2K	1	04	4	Counter	16	+1.72
9600	1	08	8	Counter	16	+1.72
4800	1	10	16	Counter	16	+1.72
2400	1	21	33	Counter	16	-1.37
1800	1	2B	43	Counter	16	+0.94
1200	1	41	65	Counter	16	+0.16
600	1	82	130	Counter	16	+0.16
300	16	21	33	Timer	16	-1.36
150	16	41	65	Timer	16	+0.16
110	16	59	89	Timer	16	-0.025
75	16	82	130	Timer	16	+0.16

Baud Rate Programming For 2.5 MHz VL-7806/7 Boards

3.6864 MHz Clock

Baud Rate	CTC Divider	Count Hex	Count Decimal	CTC Mode	DART Divider	Baud Rate Error (%)
38.4K	1	03	3	Counter	16	0
19.2K	1	06	6	Counter	16	0
9600	1	0C	12	Counter	16	0
4800	1	18	24	Counter	16	0
2400	1	30	48	Counter	16	0
1800	1	40	64	Counter	16	0
1200	1	60	96	Counter	16	0
600	1	C0	192	Counter	16	0
300	16	30	48	Timer	16	0
150	16	60	96	Timer	16	0
110	16	83	131	Timer	16	-0.07
75	16	C0	192	Timer	16	0

Baud Rate Programming For 3.6864 MHz VL-7806/7 Boards

4.0 MHz Clock

Baud Rate	CTC Divider	Count Hex	Count Decimal	CTC Mode	DART Divider	Baud Rate Error (%)
9600	1	0D	13	Counter	16	+0.16
4800	1	1A	26	Counter	16	+0.16
2400	1	34	52	Counter	16	+0.16
1800	1	45	69	Counter	16	+0.64
1200	1	68	104	Counter	16	+0.16
600	1	D0	208	Counter	16	+0.16
300	16	34	52	Timer	16	+0.16
150	16	68	104	Timer	16	+0.16
110	16	8E	142	Timer	16	+0.03
75	16	D0	208	Timer	16	+0.16

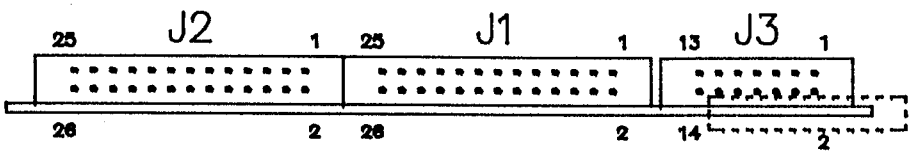
Baud Rate Programming For 4 MHz VL-7806/7 Boards

6.0 MHz Clock

Baud Rate	CTC Divider	Count Hex	Count Decimal	CTC Mode	DART Divider	Baud Rate Error (%)
38400	1	05	5	Counter	16	-2.34
19200	1	0A	10	Counter	16	-2.34
9600	1	14	20	Counter	16	-2.34
4800	1	27	39	Counter	16	0.16
2400	1	4E	78	Counter	16	0.16
1800	1	68	104	Counter	16	0.16
1200	1	9C	156	Counter	16	0.16
600	16	27	39	Timer	16	0.16
300	16	4E	78	Timer	16	0.16
150	16	9C	156	Timer	16	0.16
110	16	D5	213	Timer	16	0.03
75	16	4E	78	Timer	64	0.16

Baud Rate Programming For 6 MHz VL-7806/7 Boards

CONNECTOR PINOUTS



I/O Connector Physical Pin Locations

J1 / J2 Pin	Signal Name	RS-232-C Pin
1	-	1
2	-	14
3	TD*	2
4	-	15
5	RD*	3
6	-	16
7	RTS	4
8	-	17
9	CTS	5
10	-	18
11	DSR	6
12	-	19
13	GND	7
14	DTR	20
15	DCD	8
16	-	21
17	-	9
18	RI	22
19	-	10
20	-	23
21	-	11
22	-	24
23	-	12
24	-	25
25	-	13
26	-	-

Note: The serial port connectors can be converted to the RS-232-C pinout using VersaLogic cable #9560.

Serial Port Connector Pinout (VL-7806 J1 and J2, VL-7807 J1)

VL-7807 Connector J1	Signal Name	Centronics Connector
1	STROBE*	1
2	GND	19
3	DATA 1	2
4	GND	20
5	DATA 2	3
6	GND	21
7	DATA 3	4
8	GND	22
9	DATA 4	5
10	GND	23
11	DATA 5	6
12	GND	24
13	DATA 6	7
14	GND	25
15	DATA 7	8
16	GND	26
17	DATA 8	9
18	GND	27
19	-	10
20	GND	28
21	BUSY	11
22	GND	29
23	PE	12
24	GND	30
25	-	13
26	-	31

Note: Connector J1 can be converted to the Centronics pinout using VersaLogic cables #9560 and 9556.

Centronics Port Connector Pinout (VL-7807 J1)

J3 Pin	Signal Name	Input Load (Sink ma)	Output Drive (Sink ma)
1	GND		
2	CLOCK/INT 3	1	
3	GND		
4	CLOCK/INT 2	1	
5	GND		
6	COUNT/TIME 2		2
7	GND		
8	CLOCK/INT 1	1	
9	GND		
10	COUNT/TIME 1		2
11	GND		
12	WAIT/READY* A	0.1	2
13	GND		
14	WAIT/READY* B	0.1	2

Counter/Timer Connector J3

J4 Pin	Signal Name	Input Load (Sink ma)
1	GND	
2	SEGMENT	1.3

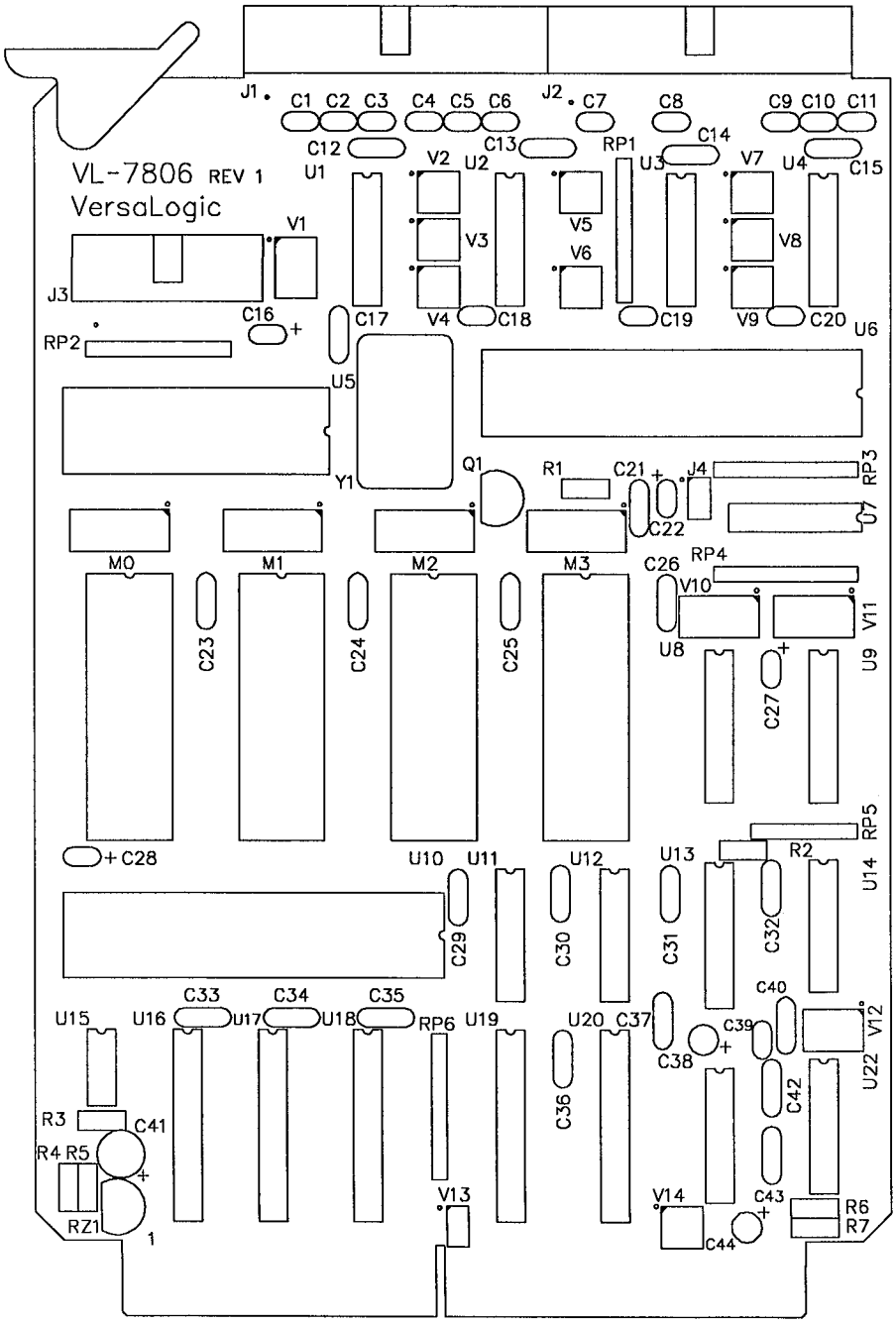
Segment Connector / Jumper J4

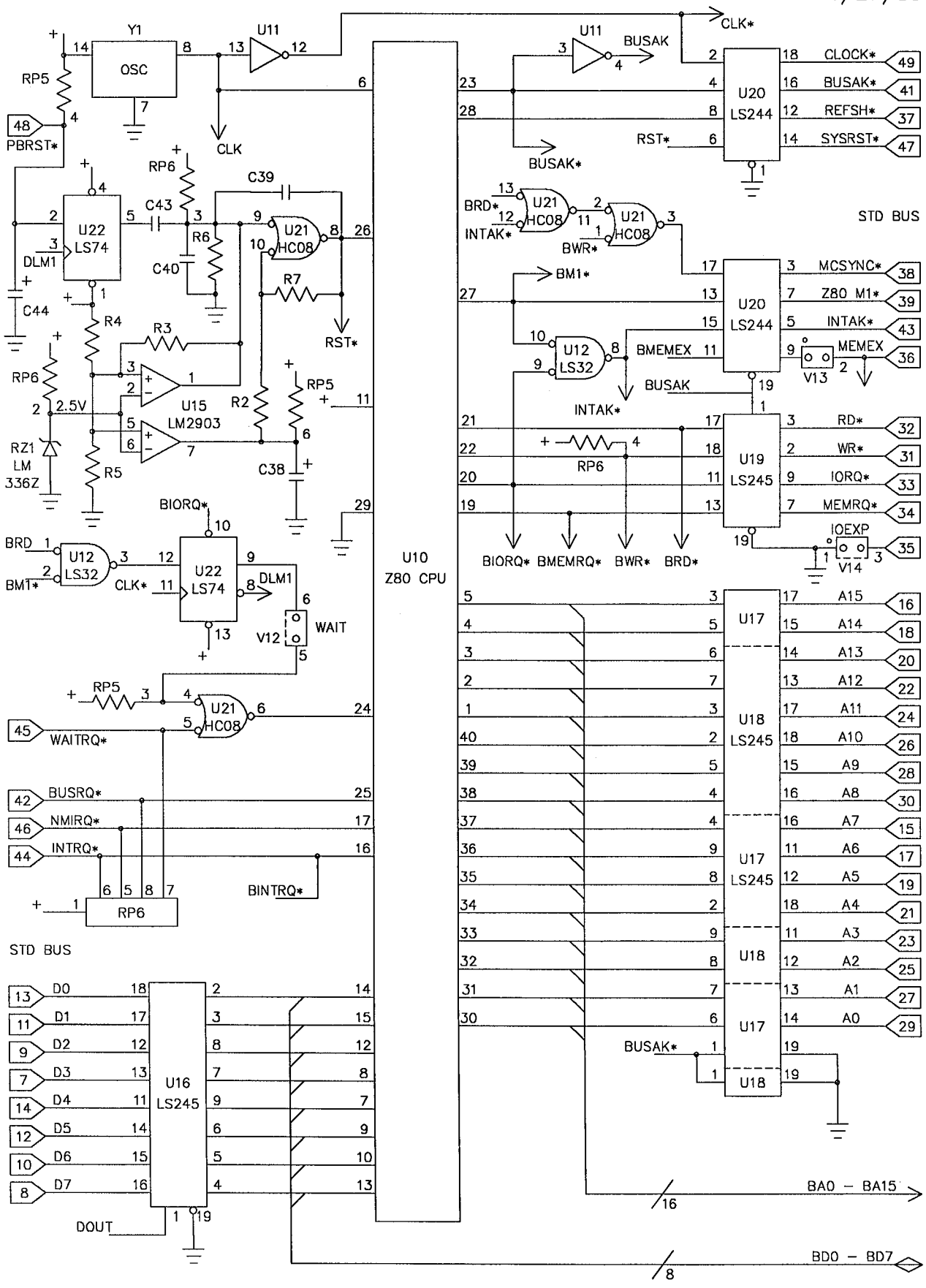
STD BUS Pinout

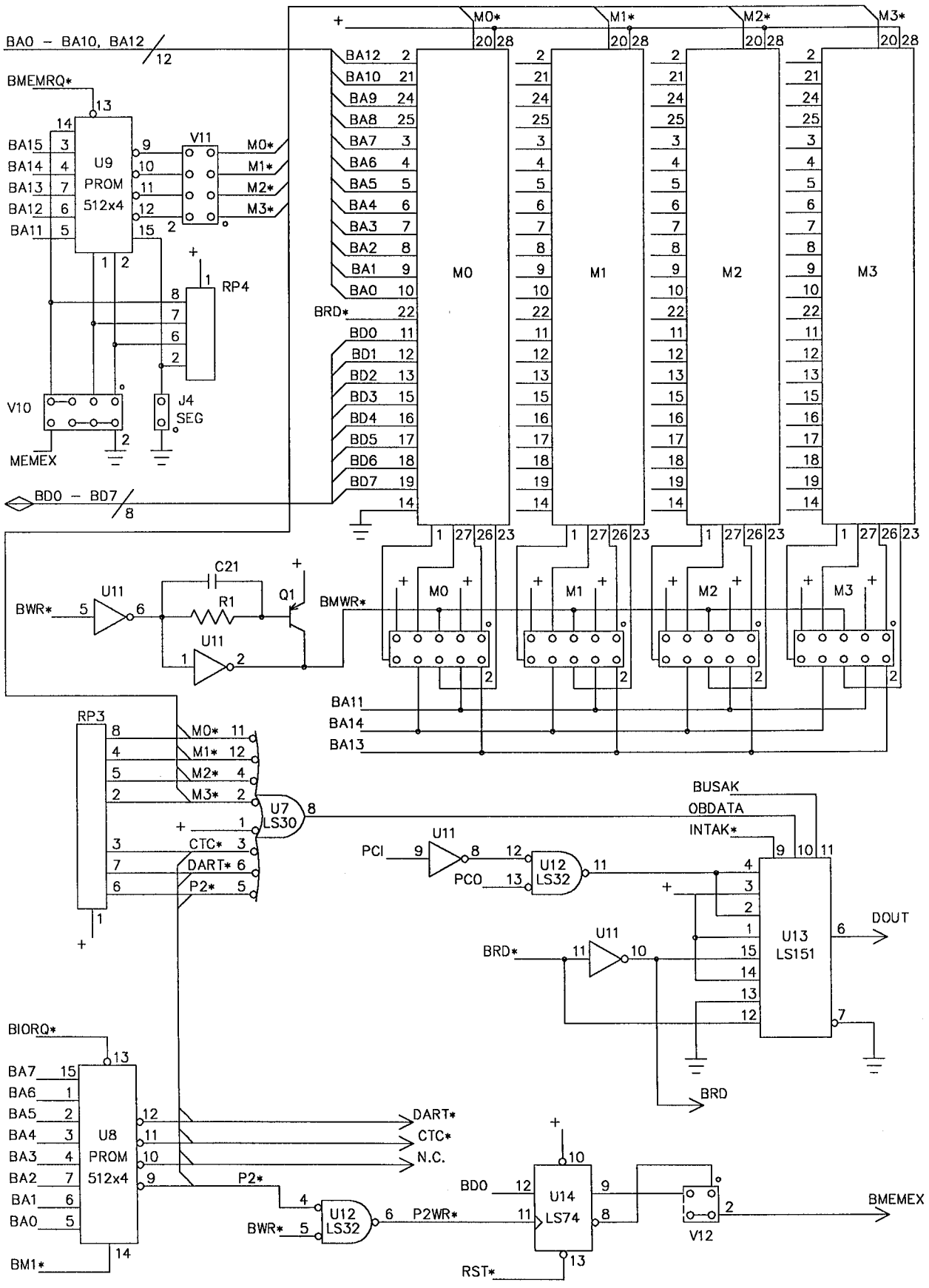
Connections from the VL-7806/7 to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7806/7.

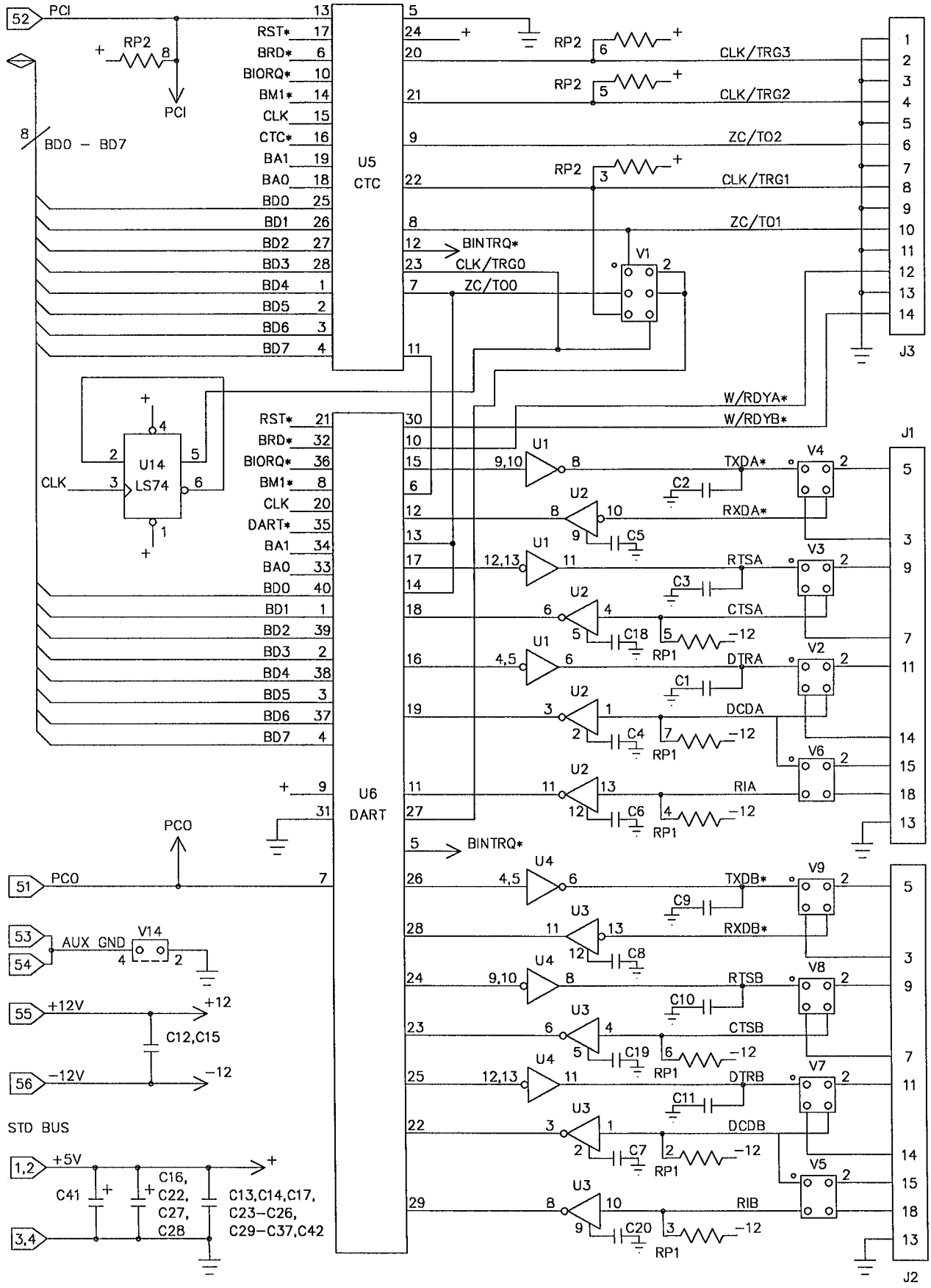
COMPONENT SIDE				SOLDER SIDE			
PIN	SIGNAL	FLOW	DESCRIPTION	PIN	SIGNAL	FLOW	DESCRIPTION
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	-	-5V or bat. backup	6	-5V	-	-5V power
7	D3	I/O	Data bus	8	D7	I/O	Data bus
9	D2	I/O	Data bus	10	D6	I/O	Data bus
11	D1	I/O	Data bus	12	D5	I/O	Data bus
13	DO	I/O	Data bus	14	D4	I/O	Data bus
17	A6	Out	Address bus	18	A14	Out	Address bus
19	A5	Out	Address bus	20	A13	Out	Address bus
21	A4	Out	Address bus	22	A12	Out	Address bus
23	A3	Out	Address bus	24	A11	Out	Address bus
25	A2	Out	Address bus	26	A10	Out	Address bus
27	A1	Out	Address bus	28	A9	Out	Address bus
29	AO	Out	Address bus	30	A8	Out	Address bus
31	WR*	Out	Write strobe	32	RD*	Out	Read strobe
33	IORQ*	Out	I/O addr. select	34	MEMRQ*	Out	Memory addr. select
35	IOEXP*	(1)	I/O expansion	36	MEMEX*	(2)	Memory expansion
37	REFRESH*	Out	Refresh timing	38	MCSYNC*	Out	Machine cycle sync.
39	STATUS1*	Out	Z80 M1*	40	STATUSO*	-	CPU status
41	BUSAK*	Out	Bus acknowledge	42	BUSRQ*	In	Bus request
43	INTAK*	Out	Interrupt acknowl.	44	INTRQ*	In	Interrupt request
45	WAITRQ*	In	Wait request	46	NMIRQ*	In	Non-maskable int.
47	SYSRESET*	In	System reset	48	PBRESET*	In	Push button reset
49	CLOCK*	Out	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	(3)	±12 volt ground	54	AUXGND	(3)	±12 volt ground
55	AUX+V	In	+12 volt input	56	AUX-V	In	-12 volt input

Notes:
1) Jumper option. Normally strapped to ground.
2) Jumper option. Normally an output.
3) Jumper option. Normally strapped to digital ground (pins 3-4).
-) All address, data, and status lines (except 37, 41, 47 and 49) can be driven by another source while BUSAK* is active. DMA can be performed to on-board memory devices.


VL-7806 REV 1
VersaLogic
J1
J2
J3
J4
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U22
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
RP1
RP2
RP3
RP4
RP5
RP6
R1
R2
R3
R4
R5
R6
R7
RZ1
Q1
Y1
M0
M1
M2
M3
1


Y1
OSC
U11
RP5
PBRST*
CLK
CLK*
U22
LS74
DLM1
C44
RP6
C43
C39
R6
C40
U21
HC08
R7
RST*
R4
R3
RP6
2.5V
U15
LM2903
RZ1
LM
336Z
R5
R2
RP5
C38
BIORQ*
BRD
BM1*
U12
LS32
CLK*
DLM1
WAIT
V12
RP5
WAITRQ*
BUSRQ*
NMIRQ*
INTRQ*
BINTRQ*
RP6
STD BUS
D0
D1
D2
D3
D4
D5
D6
D7
U16
LS245
DOUT
U10
Z80 CPU
BUSAK
BUSAK*
U20
LS244
RST*
CLOCK*
BUSAK*
REFSH*
SYSRST*
BRD*
INTAK*
BWR*
STD BUS
BM1*
MCSYNC*
Z80 M1*
INTAK*
BMEMEX
MEMEX
V13
BUSAK
INTAK*
RD*
WR*
IORQ*
MEMRQ*
IOEXP
V14
RP6
BIORQ*
BMEMRQ*
BWR*
BRD*
U19
LS245
U17
U18
LS245
U17
LS245
U18
U17
U18
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BUSAK*
BA0 – BA15
16
BD0 – BD7
8


BA0 – BA10, BA12
12
BMEMRQ*
U9
PROM
512x4
BA15
BA14
BA13
BA12
BA11
V11
M0*
M1*
M2*
M3*
RP4
V10
MEMEX
J4
SEG
BD0 – BD7
8
BA12
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
BRD*
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
M0
M1
M2
M3
C21
R1
Q1
U11
BWR*
BMWR*
BA11
BA14
BA13
RP3
U7
LS30
CTC*
DART*
P2*
BUSAK
OBDATA
INTAK*
PCI
PCO
U12
LS32
U13
LS151
DOUT
BRD
BIORQ*
U8
PROM
512x4
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
BM1*
DART*
CTC*
N.C.
P2*
BWR*
P2WR*
BD0
U14
LS74
RST*
V12
BMEMEX


52 PCI
RP2
PCI
8 BD0 – BD7
U5 CTC
RST* 17
BRD* 6
BIORQ* 10
BM1* 14
CLK 15
CTC* 16
BA1 19
BA0 18
BD0 25
BD1 26
BD2 27
BD3 28
BD4 1
BD5 2
BD6 3
BD7 4
CLK/TRG3
CLK/TRG2
ZC/TO2
CLK/TRG1
ZC/TO1
BINTRQ*
CLK/TRG0
ZC/TO0
V1
J3
U14 LS74
CLK
W/RDYA*
W/RDYB*
U6 DART
RST* 21
BRD* 32
BIORQ* 36
BM1* 8
CLK 20
DART* 35
BA1 34
BA0 33
BD0 40
BD1 1
BD2 39
BD3 2
BD4 38
BD5 3
BD6 37
BD7 4
U1
U2
U3
U4
TXDA*
RXDA*
RTSA
CTSA
DTRA
DCDA
RIA
TXDB*
RXDB*
RTSB
CTSB
DTRB
DCDB
RIB
V2
V3
V4
V5
V6
V7
V8
V9
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
RP1
J1
J2
PCO
51 PCO
53 AUX GND
54
V14
55 +12V
56 –12V
C12,C15
STD BUS
1,2 +5V
3,4
C41
C16, C22, C27, C28
C13,C14,C17, C23–C26, C29–C37,C42

VL-7806 PARTS LIST
Multifunction CPU Board

Capacitors

C1-C11, C18-C20	390 pf NPO ceramic
C12-C15, C17, C22-C26, C29-C37, C42, C43	.01 uf ceramic
C16, C27, C28	1 uf 35V tant.
C21, C40	680 pf NPO ceramic
C38, C44	2.2 uf 50V elect. radial
C39	270 pf NPO ceramic
C41	10 uf 10V tant.

Integrated Circuits

U1, U4	1488
U2, U3	1489A
U5	Z80-A CTC, 8430
U6	Z80-A DART/SIO/0, 8470/8440
U7	74LS030
U8	Bipolar PROM "B" (I/O map)
U9	Bipolar PROM "A" (memory map)
U10	Z80-A CPU, 8400
U11	74LS04
U12	74LS32
U13	74LS151
U14, U22	74LS74
U15	LM2903
U16, U17, U18, U19	74LS245
U20	74LS244

U21	74HC08

Resistors

R1, R4	10K ohm, 1%, 1/4W
R2	2.2K ohm, 5%, 1/4W
R3	215K ohm, 1%, 1/4W
R5, R6	12.1K ohm, 1%, 1/4W
R7	27K ohm, 5%, 1/4W
RP1	22K ohm, 7 resistor SIP
RP2, RP4, RP6	4K7 ohm, 7 resistor SIP
RP3	1K ohm, 7 resistor SIP
RP5	10K ohm, 5 resistor SIP

Semiconductors

Q1	2N2907
RZ1	LM336Z-2.5V
Y1	Crystal osc. (frequency depends on version)

Miscellaneous

J1, J2	26 pin R/A header
J3	14 pin R/A header

VL-78CT06 PARTS LIST
Multifunction CPU Board (Extended Temperature Version)

Capacitors

C1-C11, C18-C20	Not used
C12-C15, C17, C22-C26, C29-C37, C42, C43	.01 uf ceramic
C16, C27, C28	1 uf 35V tant.
C21, C40	680 pf NPO ceramic
C38, C44	2.2 uf 50V elect. radial
C39	270 pf NPO ceramic
C41	10 uf 10V tant.

Integrated Circuits

U1, U4	14C88
U2, U3	14C89A
U5	CMOS Z80-A CTC, 84C30
U6	CMOS Z80-A DART/SIO/0, 84C70/84C40
U7	74HCT030
U8	Bipolar PROM "B" (I/O map), 54S571
U9	Bipolar PROM "A" (memory map), 54S571
U10	CMOS Z80-A CPU, 84C00
U11	74HCT04
U12	74HCT32
U13	74HCT151
U14, U22	74HCT74
U15	LM2903
U16, U17, U18, U19	74ACT245
U20	74ACT244

U21	74HC08

Resistors

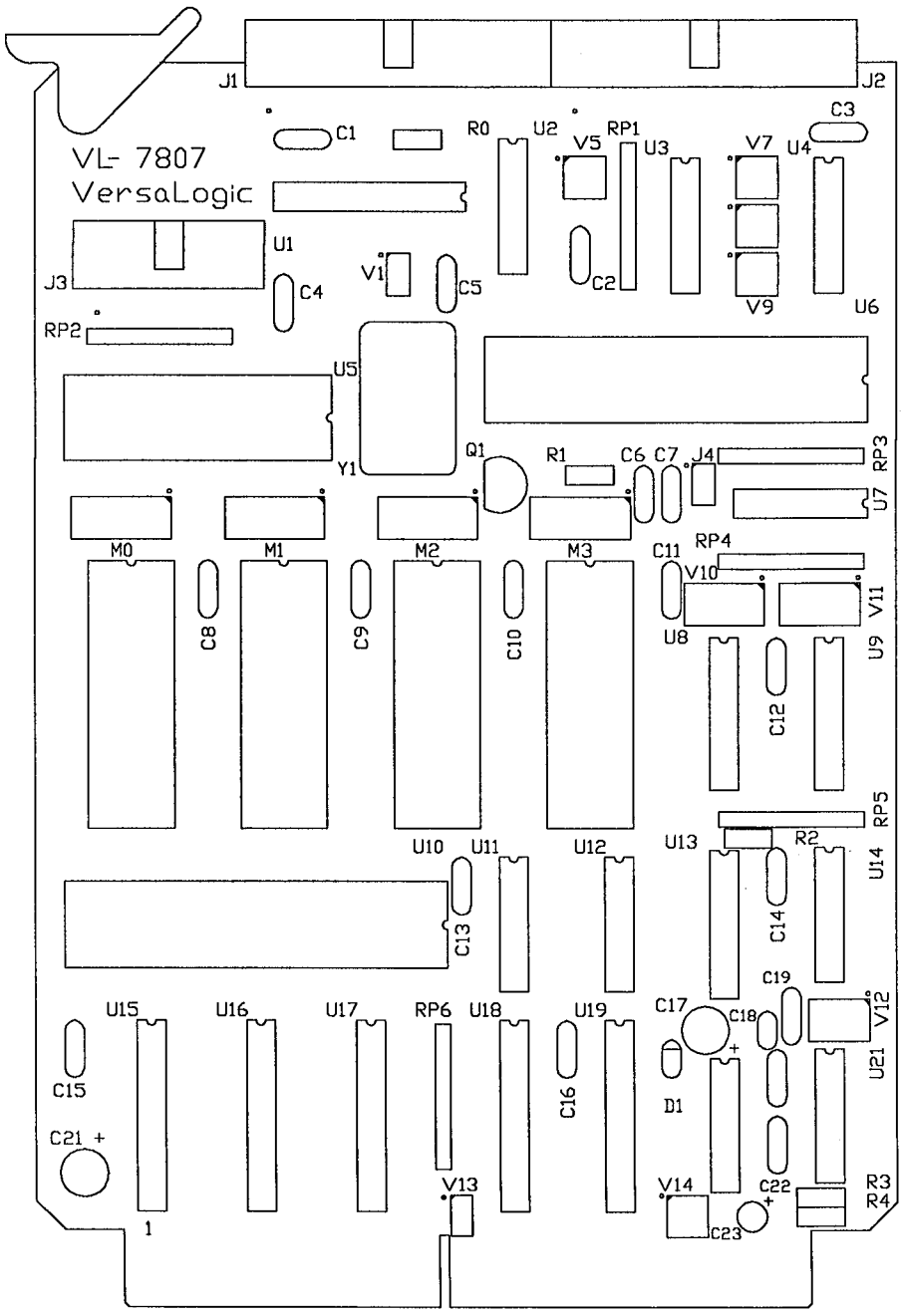
R1, R4	10K ohm, 1%, 1/4W
R2	2.2K ohm, 5%, 1/4W
R3	215K ohm, 1%, 1/4W
R5, R6	12.1K ohm, 1%, 1/4W
R7	27K ohm, 5%, 1/4W
RP1, RP4	22K ohm, 7 resistor SIP
RP2	10K ohm, 7 resistor SIP
RP3	1K ohm, 7 resistor SIP
RP5	10K ohm, 5 resistor SIP
RP6	4.7K ohm, 7 resistor SIP

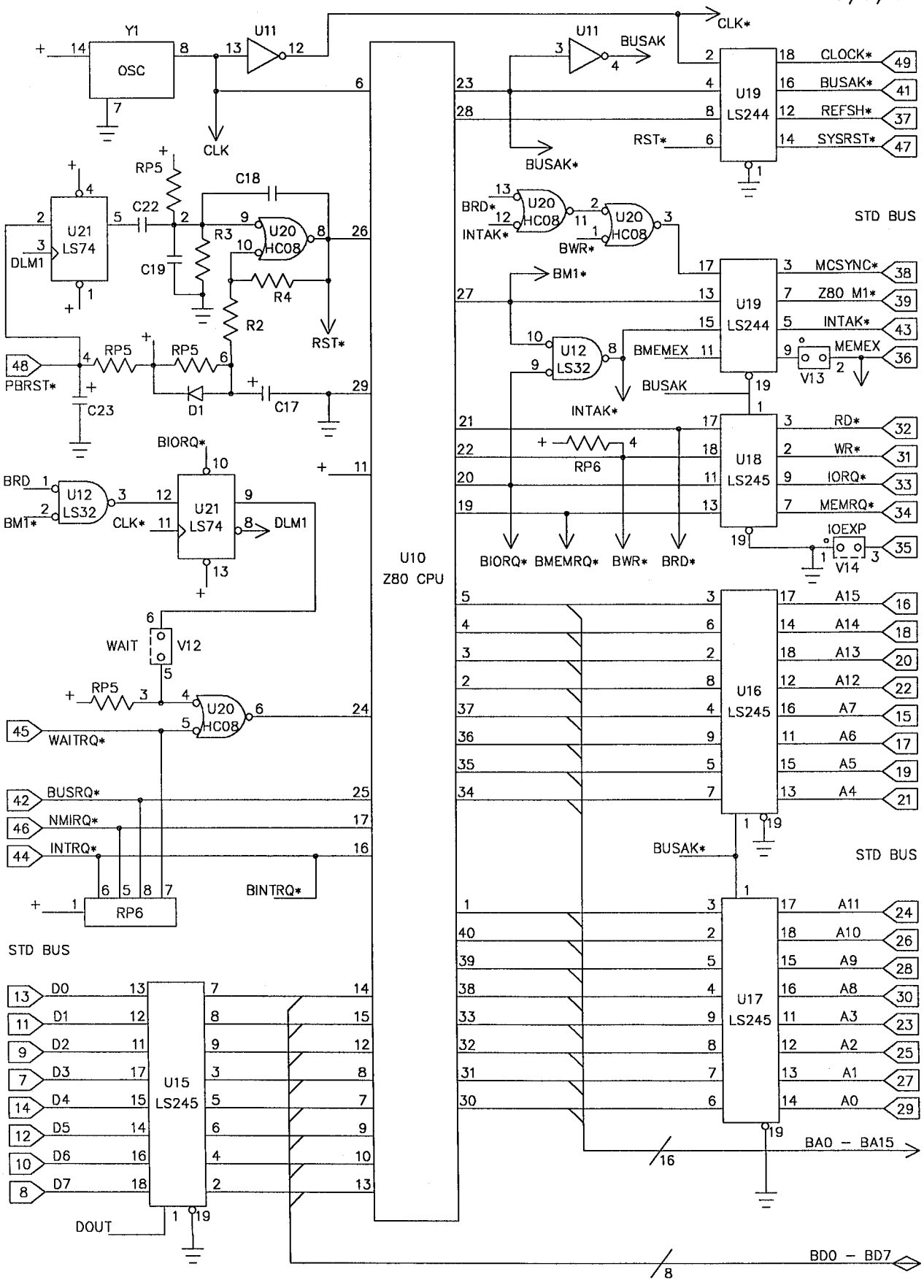
Semiconductors

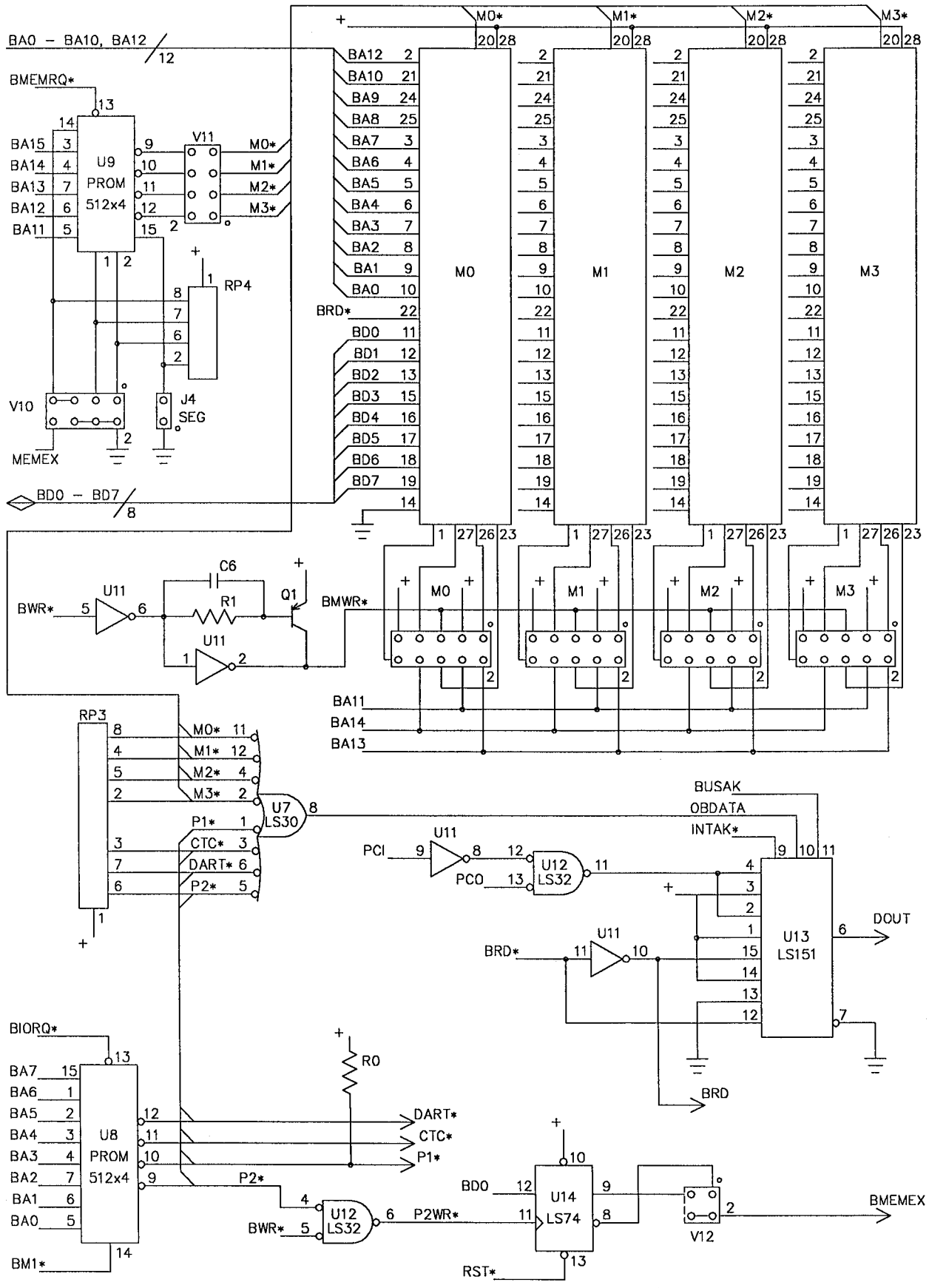
Q1	PN2907
RZ1	LM236H-2.5V or LM136
Y1	CMOS Crystal osc. (frequency depends on version)

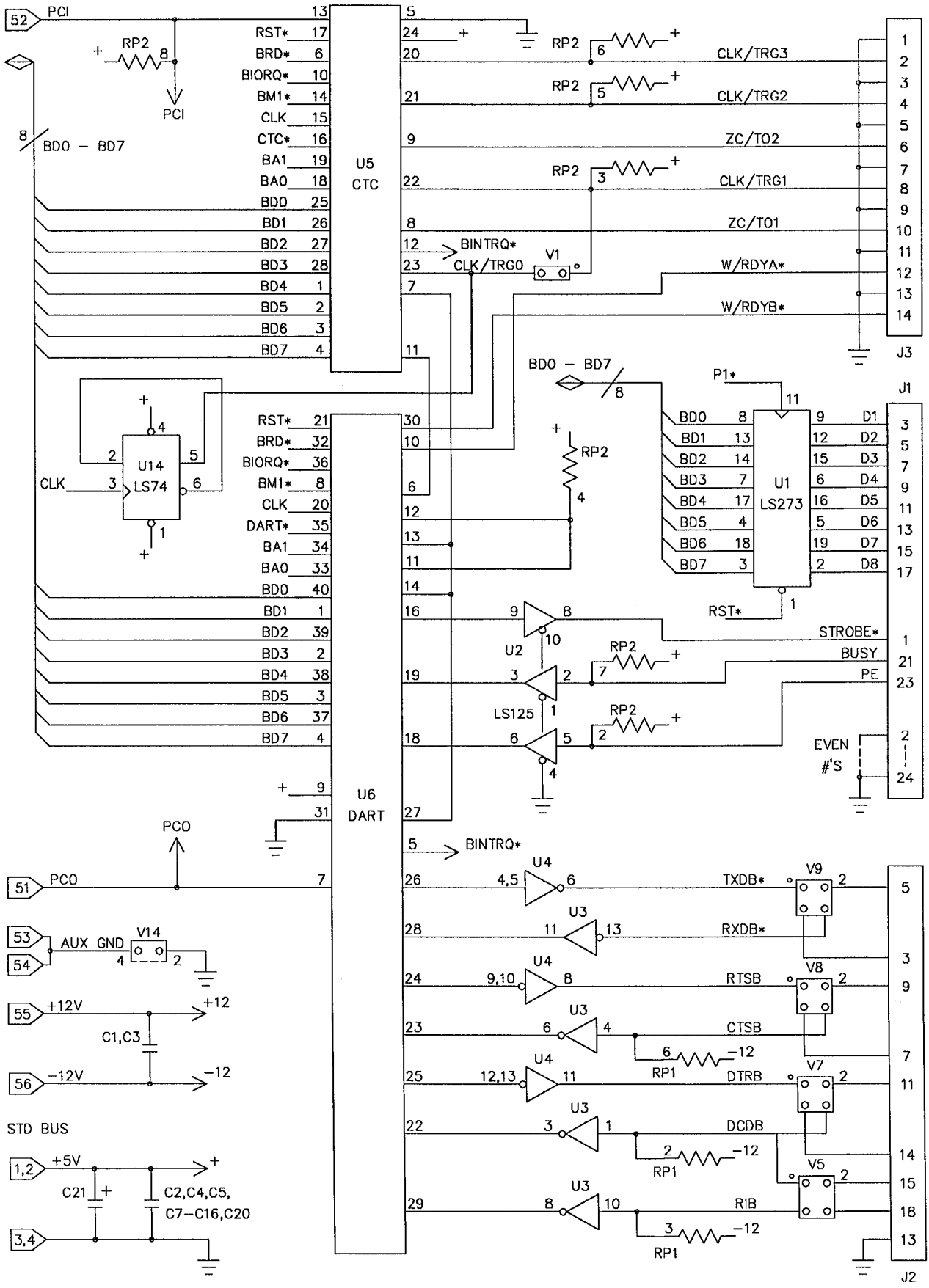
Miscellaneous

J1, J2	26 pin R/A header
J3	14 pin R/A header


VL- 7807
VersaLogic
J1
J2
J3
C1
C2
C3
C4
C5
R0
U1
U2
V5
RP1
U3
V7
U4
V1
V9
U6
RP2
U5
Y1
Q1
R1
C6
C7
J4
RP3
U7
M0
M1
M2
M3
C11
RP4
V10
V11
C8
C9
C10
U8
U9
C12
RP5
U10
U11
U12
U13
R2
U14
C13
C14
C19
U15
U16
U17
RP6
U18
U19
C17
C18
V12
C15
D1
U21
C21
V13
V14
C22
R3
R4
C23
1


Y1
OSC
U11
CLK
CLK*
RP5
C18
C22
R3
C19
R4
R2
RST*
U21
LS74
DLM1
U20
HC08
PBRST*
C23
D1
C17
BIORQ*
BRD
BM1*
U12
LS32
CLK*
DLM1
WAIT
V12
RP5
WAITRQ*
BUSRQ*
NMIRQ*
INTRQ*
BINTRQ*
RP6
STD BUS
U15
LS245
D0
D1
D2
D3
D4
D5
D6
D7
DOUT
U10
Z80 CPU
BUSAK
BUSAK*
U19
LS244
CLOCK*
BUSAK*
REFSH*
SYSRST*
RST*
BRD*
INTAK*
BWR*
STD BUS
BM1*
MCSYNC*
Z80 M1*
INTAK*
BMEMEX
MEMEX
V13
BUSAK
INTAK*
U18
LS245
RD*
WR*
IORQ*
MEMRQ*
IOEXP
V14
RP6
BIORQ*
BMEMRQ*
BWR*
BRD*
U16
LS245
A15
A14
A13
A12
A7
A6
A5
A4
BUSAK*
STD BUS
U17
LS245
A11
A10
A9
A8
A3
A2
A1
A0
BA0 – BA15
16
BD0 – BD7
8


BA0 – BA10, BA12
12
BMEMRQ*
U9
PROM
512x4
BA15
BA14
BA13
BA12
BA11
V11
M0*
M1*
M2*
M3*
RP4
V10
MEMEX
J4
SEG
BD0 – BD7
8
BA12
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
BRD*
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
M0
M1
M2
M3
C6
R1
Q1
U11
BWR*
BMWR*
BA11
BA14
BA13
RP3
U7
LS30
P1*
CTC*
DART*
P2*
BUSAK
OBDATA
INTAK*
PCI
PCO
U12
LS32
DOUT
U13
LS151
BRD
BIORQ*
U8
PROM
512x4
R0
DART*
CTC*
P1*
P2*
BM1*
P2WR*
U14
LS74
BDO
RST*
V12
BMEMEX


52 PCI
RP2
PCI
8 BD0 - BD7
U5 CTC
RST* 17
BRD* 6
BIORQ* 10
BM1* 14
CLK 15
CTC* 16
BA1 19
BA0 18
BD0 25
BD1 26
BD2 27
BD3 28
BD4 1
BD5 2
BD6 3
BD7 4
13
5
24
20
21
9
22
8
12
23
7
11
BINTRQ*
CLK/TRG0
V1
CLK/TRG3
CLK/TRG2
ZC/TO2
CLK/TRG1
ZC/TO1
W/RDYA*
W/RDYB*
J3
U14 LS74
CLK
U6 DART
RST* 21
BRD* 32
BIORQ* 36
BM1* 8
CLK 20
DART* 35
BA1 34
BA0 33
BD0 40
BD1 1
BD2 39
BD3 2
BD4 38
BD5 3
BD6 37
BD7 4
9
31
30
10
6
12
13
11
14
16
19
18
BD0 - BD7
P1*
U1 LS273
BD0 8
BD1 13
BD2 14
BD3 7
BD4 17
BD5 4
BD6 18
BD7 3
D1 9
D2 12
D3 15
D4 6
D5 16
D6 5
D7 19
D8 2
RST*
J1
STROBE*
BUSY
PE
EVEN #'S
U2
LS125
PCO
51 PCO
53 AUX GND
54
V14
55 +12V
56 -12V
C1,C3
STD BUS
1,2 +5V
3,4
C21
C2,C4,C5, C7-C16,C20
BINTRQ*
U4
U3
TXDB*
RXDB*
RTSB
CTSB
DTRB
DCDB
RIB
V9
V8
V7
V5
RP1
J2

VL-7807 PARTS LIST

Capacitors

C1, C2, C3, C4, C5, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C20, C22	.01 uf ceramic disk
C6, C19	680 pf NPO ceramic
C17, C21	22 uf, 25V, elect.
C18	270 pf NPO ceramic
C23	2.2 uf 50V elect. radial

Integrated Circuits

U1	LS273
U2	LS125
U3	1489A
U4	1488
U5	Z80-A CTC, 8430
U6	Z80-A DART/SIO/0, 8470/8440
U7	74LS030
U8	Bipolar PROM "B" (I/O map)
U9	Bipolar PROM "A" (Memory map)
U10	Z80-A CPU, 8400
U11	74LS04
U12	74LS32
U13	74LS151
U14, U21	74LS74
U15, U16, U17, U18	74LS245
U19	74LS244

U20	74HC08

Resistors

R1	10K ohm, 5%, 1/4W
RO, R2	1K ohm, 5%, 1/4W
R3	12K ohm, 5%, 1/4W
R4	10K ohm, 5%, 1/4W
RP1	22K ohm, 7 resistor SIP
RP2, RP4, RP5, RP6	4K7 ohm, 7 resistor SIP
RP3	1K ohm, 7 resistor SIP

Semiconductors

D1	1N4148
Q1	2N2907
Y1	Crystal osc. (frequency depends on version)

Miscellaneous

J1, J2	26 pin R/A header
J3	14 pin R/A header