Reference Manual

VL-7804a

Z80 CPU
Card for the STD Bus

VERSALOGIC
CORPORATION

VL-7804A

Z80 CPU Card for the STD Bus

Model VL-7804A

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REFERENCE MANUAL

VL-7804A Rev. 2.00
VL-7804A1 Rev. 2.00
Doc. Rev. 09/26/94

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M7804

Model VL-7804A
Z80 Processor Card for the STD BUS

REFERENCE MANUAL

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Section 1
INTRODUCTION

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7804A Z80 processor card. This low cost CPU card features several on-board functions including three 16-bit timer/counters, four 28-pin RAM/ROM sockets, MEMEX control, and a single I/O line. These features simplify system construction, and lower the total system cost.

The VL-7804A card is part of the full line of STD BUS products which are available from VersaLogic. Contact VersaLogic for further information on the compatible STD BUS expansion cards that are currently available for use with the VL-7804A processor cards.

OVERVIEW

The VL-7804A CPU card features a Z80 processor, three counter/ timer channels, four 28-pin memory sockets, and an external I/O line.

It includes flexible memory chip type selection that allows a mixture of 2, 4, or 8K memory devices (RAM, ROM, EEPROM) to be accommodated on-board. In addition, the memory expansion line (MEMEX) can be controlled by the board.

The three 16-bit counter/timer channels can provide a number of programmable functions including external event counting, pulse train and square wave output, time interval measurement, and one-shot pulse output. Timing/counting can occur simultaneously on all three channels and the channels can be cascaded for extended timing/counting functions.

One input and one output line are available for external I/O.

The VL-7804A operates at 4 MHz.

FEATURES

- Fully Buffered Z80A CPU.
- 4 MHz Operation.
- 32K RAM/ROM Capacity.
- Four 28-Pin Memory Sockets.
- Three Independent 16-Bit Timer/Counters.
- External Timer/Counter Inputs.
- DMA to On-Board Memory.
- Interrupt Controls for Counter/Timer Channels.
- Latching Timer/Counter Connector.
- 1-Bit External Input and Output Lines.
- MEMEX Line Control.
- Direct Plug-In Replacement for Pro-Log 7804A.

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications

Storage Temperature: -40° to +75° C

Free Air Operating Temperature: 0° to +65° C

Power Requirements: 5V ±5% @ 550 ma typ. (without on-board memory)

Operating Frequency: 4.0 MHz

Maximum Counter Frequency: 2.5 MHz

I/O Interface:

- Counter/timer output drive: 39 ma @ .7V, 15 ma @ .4V (1)
- Counter/timer clock input load: 1.6 ma @ .4V
- Counter/timer gate input load: 1.2 ma @ .35V (4.7K ohm pull-up)

- External output line: 23 ma @ .35V (4.7K ohm pull-up)
- External input line: 1.2 ma @ .35V (4.7K ohm pull-up)

(1) Open collector output with 4.7 ohm pull-up

Section 2
INSTALLATION AND CONFIGURATION

HANDLING

**** CAUTION **** The VL-7804A card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

INSTALLATION

The VL-7804A can be inserted into any slot of an STD BUS card cage.

The VL-7804A does not support the STD Bus priority chain interrupt structure. The physical order of the VL-7804A or other cards in the card cage has no effect on the operation of the system.

**** CAUTION **** When cards are installed in an STD BUS card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD BUS cards.

**** CAUTION **** Cards should be inserted or removed from the STD BUS card cage only when the system power is off.

EXTERNAL CONNECTIONS

Connection to the VL-7804A can be made for access to the counter/timer I/O lines, or the one-bit input and output lines. A pinout of connector J1 is shown below.

Connection to the 26-pin latching header type connector can be made with mating connectors such as 3M #3399-7026, AMP #499505-7, or Ansley #609-2641. The connector used should include a strain relief in order to use the built-in latch bars.

J1 Pin	I/O	Signal Name
2	Out	EXT-OUT
4	In	GATE-2
6	In	CLOCK-2
8	Out	OUT-2
10	In	GATE-1
12	In	CLOCK-1
14	Out	OUT-1
16	In	GATE-0
18	In	CLOCK-0
20	Out	OUT-0
22	In	EXT-IN
1-25		All odd pins = Ground

Figure 2-1. Connector J1

JUMPER SUMMARY

Various options available on the VL-7804A card are selected using removable jumper plugs (shorting plugs). Features are selected or de-selected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 2-2 shows the jumper block locations on the VL-7804A board. It also indicates the position of the jumper plugs when the board was shipped from the factory. The function of each jumper block is detailed in Figure 2-3.

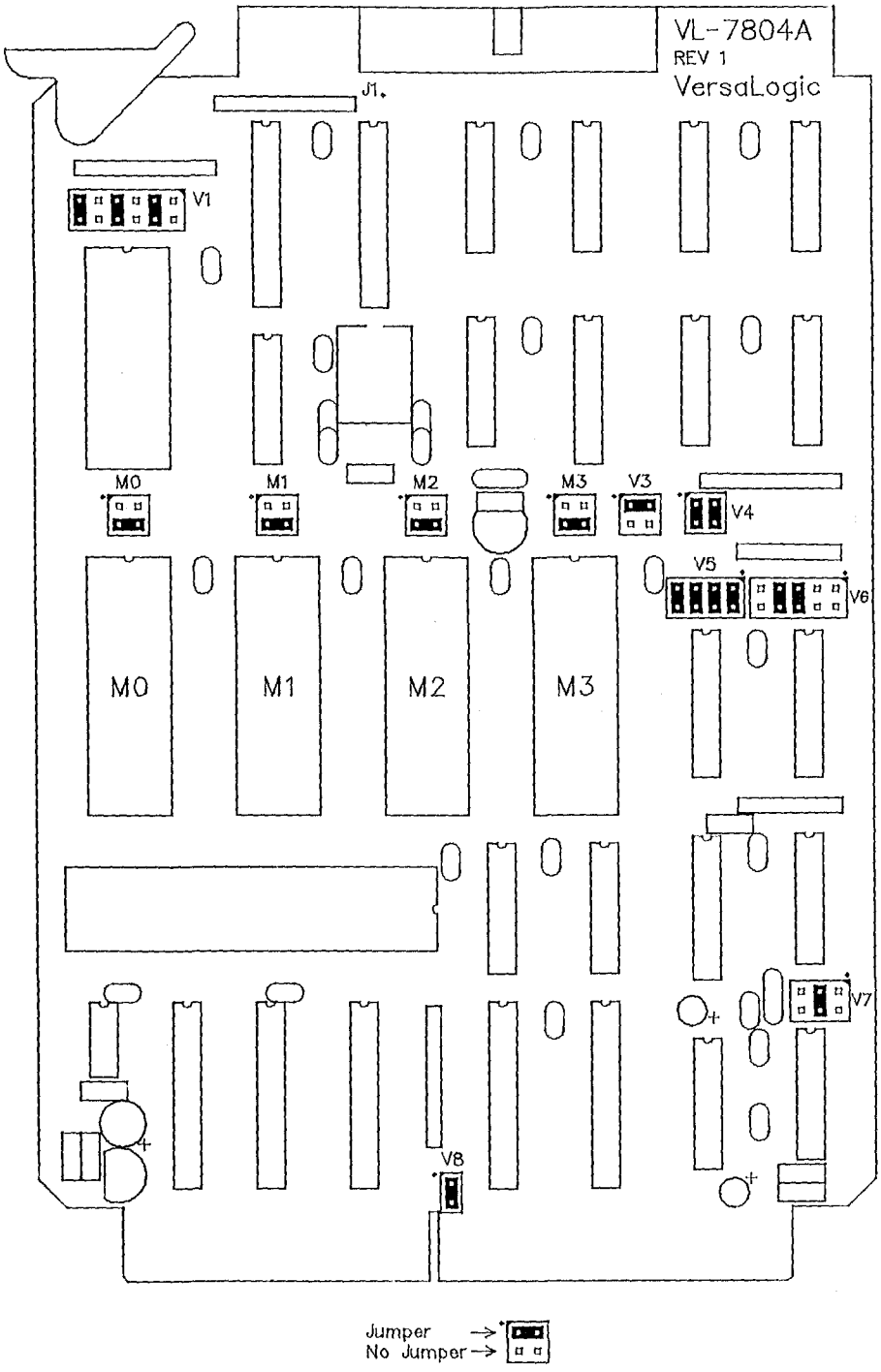


Figure 2-2. Jumper Block Locations

Jumper Block	Description	As Shipped
M0-M3	Memory socket type configuration.	4/8K RAMs/ROMs
V1	Counter/timer clock inputs.	
	a - Channel 2 clock from external connector.	out
	b - Channel 2 clock from internal 2 MHz source.	IN
	c - Channel 1 clock from external connector.	out
	d - Channel 1 clock from internal 2 MHz source.	IN
	e - Channel 0 clock from external connector.	out
	f - Channel 0 clock from internal 2 MHz source.	IN
V2	Not used.	
V3	Reset address.	
	a - Reset to address 0000.	a - IN
	b - Reset to address F000.	b - out
V4	I/O map selection. See I/O Mapping.	Hex F0-F5
V5	Memory socket enable/disable.	
	a - Socket M3 enabled.	a - IN
	b - Socket M2 enabled.	b - IN
	c - Socket M1 enabled.	c - IN
	d - Socket M0 enabled.	d - IN
V6	Memory map selection. See Memory Map.	Map #4
V7	a - MEMEX is set high at power-up.(1)	a - out
	b - MEMEX is set low at power-up.	b - IN
	c - WAIT state enabled.	c - out
V8	a - MEMEX signal controlled on-board.	a - IN
V9	a - IOEXP signal grounded.	a - IN

Notes:
1) Also inverts data written to the MEMEX control port.

Figure 2-3. Jumper Functions

MEMORY

The VL-7804 card has four on-board memory sockets. These sockets can be individually programmed (jumpered) to accept 2, 4, or 8K RAM or ROM type chips.

Installation of the on-board memory chips is accomplished in two separate steps. First, a memory map is selected that will allow each socket to be addressed at the desired memory location. Second, the jumpers for each memory socket are set to accommodate the type of chip that will be used in the socket.

Memory Map Selection

The desired memory map is selected using jumper V6. There are eight pre-programmed options from which to choose.

Note that the memory map option only determines the memory space that is reserved for the on-board memory sockets. Whether or not the space is used by each socket, and the type of RAM or RAM which can be plugged into each socket, is determined by the memory socket jumpers (discussed later in this section).

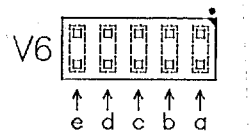
The MEMEX (memory expansion) signal can be used to control the currently selected memory map. Most applications will not benefit from its use, except for system start-up when it can be used to switch a boot PROM out of the memory map. Maps #1-7 can be jumpered for selection when MEMEX is low, or selection all the time (ignore MEMEX). Map #8 is selected only when MEMEX is high. Refer to the Reset Address headings for additional information on start-up options.

The chart below summarizes the memory maps available. Figure 2-5 details the jumper configurations used to select one of the eight memory map options and the resulting addresses of each socket.

Map#	Starting Address	MEMEX	Socket 0	Socket 1	Socket 2	Socket 3
1	0000	Low*	4K	4K	4K	2K
2	0000	Low*	2K	2K	2K	2K
3	0000	Low*	4K	4K	4K	4K
4	0000	Low*	8K	8K	8K	8K
5	0000	Low*	4K	2K	2K	2K
6	0000	Low*	8K	8K	8K	2K
7	F000	Low*	4K	-	-	-
8	0000	High	4K	-	-	-

* May be jumpered to select when MEMEX low or ignore MEMEX.

Figure 2-4. Memory Map Option Summary



V6 e	V6 d	V6 c	V6 b	V6 a	Map#	Socket 0	Socket 1	Socket 2	Socket 3
(1)	(1)	X	X	X	1	4K 0000-0FFF	4K 1000-1FFF	4K 2000-2FFF	2K 3000-37FF
(1)	(1)	X	X	-	2	2K 0000-07FF	2K 0800-0FFF	2K 1000-17FF	2K 1800-1FFF
(1)	(1)	X	-	X	3	4K 0000-0FFF	4K 1000-1FFF	4K 2000-2FFF	4K 3000-3FFF
(1)	(1)	X	-	-	4	8K 0000-1FFF	8K 2000-3FFF	8K 4000-5FFF	8K 6000-7FFF
(1)	(1)	-	X	X	5	4K 0000-0FFF	2K 1000-17FF	2K 1800-1FFF	2K 2000-27FF
(1)	(1)	-	X	-	6	8K 0000-1FFF	8K 2000-3FFF	8K 4000-5FFF	2K 6000-67FF
(1)	(1)	-	-	X	7	4K F000-FFFF	-	-	-
X	-	-	-	-	8(2)	4K 0000-0FFF	-	-	-

Notes:
X = Jumper installed.
- = Jumper removed.
1) Jumper V6e IN and V6d OUT to select this map when MEMEX is low.
Jumper V6e OUT and V6d IN to select this map always (ignore MEMEX).
2) This map is selected only when MEMEX is high.

Figure 2-5. Memory Map Selection

MEMEX Signal

The MEMEX (memory expansion) signal on the STD BUS is normally used to select between two different 64K byte memory banks or maps. It can be used to expand the available memory, or to control a bootstrap PROM.

The MEMEX signal can be controlled either on-board (by the VL-7804A card) or by another card on the bus. The MEMEX signal can also be set to a high (1) or low (0) state during system power-on. The jumpers that control these functions are shown below.

Jumper Block	Description	As Shipped
V7	a - MEMEX is set high at power-up.[1] b - MEMEX is set low at power-up.	a - out b - IN
V8	a - MEMEX signal controlled on-board.	a - IN

1) Also inverts data written to the MEMEX control port.

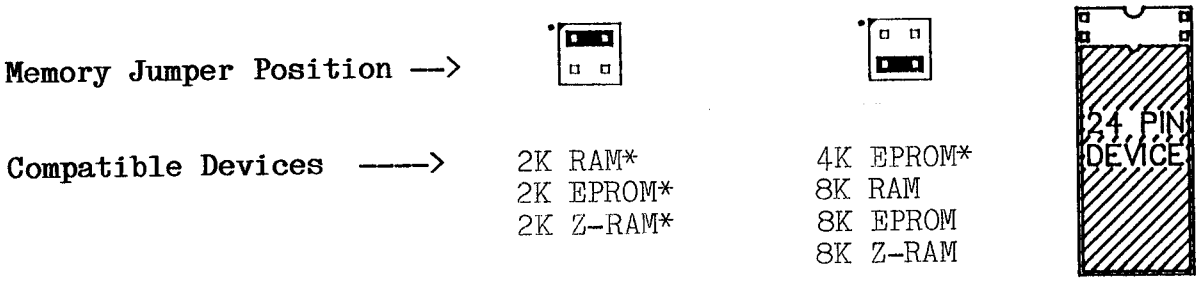
Figure 2-6. MEMEX Options

Memory Socket Configuration

Once a memory map has been selected, each socket must be configured for the type of device that will be used in the socket. The sockets are individually configured using jumper blocks M0-M3 which are located directly above the sockets.

Refer to the figure below for the appropriate jumpers for each memory device type. Jumpering is shown for EPROMs, RAMs, and Z-RAMs (Zero Power RAMs). The sockets can also accommodate standard ROMs (use EPROM jumpering).

Note that both 24 and 28-pin devices are plugged into the 28-pin sockets. Care must be taken to locate 24-pin devices at the bottom of the 28-pin socket as shown below.



* 24-pin device. Locate in the 28-pin socket as shown.

Figure 2-7. Memory Socket Jumper Configuration

Disabling Unused Sockets

Any unused socket(s) may be disabled, freeing its space in the memory map for off-board memory. Memory sockets are disabled by removing jumpers from the V5 jumper block.

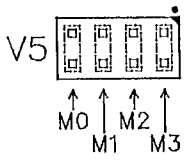
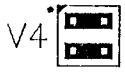


Figure 2-8. Memory Socket Enable Jumpers

I/O MAPPING

As shipped the on-board I/O devices (counter/timer, MEMEX control, bootstrap control, etc.) are located at I/O address F0 to F5. Alternately, jumper block V4 can be used to map these devices at E8-ED. All other I/O addresses are available for use by off-board I/O devices. The jumper setting for each of these options is shown below.

Alternate I/O Address	As Shipped
	

Alternate I/O Address	As Shipped	Port Type	Description
E8-EA	F0-F2	I/O	Counter/Timer Channel 0-2
EB	F3	OUT	Counter/Timer Mode Register
EC	F4	I/O	Interrupt and GP Register
ED	F5	OUT	MEMEX Control

Figure 2-9. I/O Port Mapping

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD BUS can be used to select between two different 256-port I/O banks or maps. It is used to expand the number of I/O ports that can be accessed by the processor.

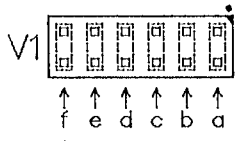
The VL-7804A card does not control or decode the IOEXP signal. Since many I/O cards require this signal to be low on the bus, the IOEXP signal is connected to ground on the VL-7804A.

For special applications the IOEXP signal can be disconnected from ground, allowing it to be controlled by another card in the system. To "float" the IOEXP signal, cut the trace jumper (on the back side of the board) at position V9.

COUNTER/TIMER CHANNELS

The counter/timer chip consists of three timer/counter channels. The clock input line for each of these channels may be connected to an internal 2 MHz source, or to the external I/O connector (for timing or counting external events).

The figure below shows the jumpers used for selection of the clock input source. Only one of the input options should be selected for each channel.



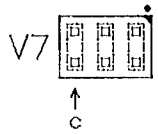
Jumper Block	Description	As Shipped
V1	Counter/timer clock inputs.	
	a - Channel 2 clock from external connector.	out
	b - Channel 2 clock from internal 2 MHz source.	IN
	c - Channel 1 clock from external connector.	out
	d - Channel 1 clock from internal 2 MHz source.	IN
	e - Channel 0 clock from external connector.	out
	f - Channel 0 clock from internal 2 MHz source.	IN

Figure 2-10. Counter/Timer Input Jumpers

WAIT STATE

The wait state jumper option allows the Z80 op code fetch cycle to be lengthened. This allows use of the VL-7804A card with slower memory devices without significant degradation in system processing speed.

The jumper option, and the resulting access times, are shown below. As shown, the card operating at 4 MHz without the wait state jumper would require RAM and ROM devices with an access time of 250 ns or better.



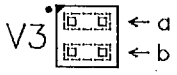
Jumper V7c	Min. Access Speed
IN	350
out	250

Figure 2-11. Wait State Option

RESET ADDRESS

Normally the processor jumps to location 0000 at power-on or when a system reset occurs. The VL-7804A includes an option which allows the reset to occur to address F000 if desired. This option is used primarily for booting of disk based systems (i.e. CP/M) which require RAM to be located at 0000.

The reset address can be changed by selecting jumper V3a or V3b as shown below. Use of the F000 reset address is discussed further in the Operation section.



Jumper Block	Description	As Shipped
V3	Reset address. a - Reset to address 0000. b - Reset to address F000.	a - IN b - out

Figure 2-12. Reset Address Jumper

Section 3
OPERATION

INTRODUCTION

This section includes information on the use (programming) of the various VL-7804A functions. Both background information and software examples are presented to assist you in constructing your own software routines.

I/O MAP

As shipped the on-board I/O devices occupy I/O address F0-F5. Alternately jumper block V4 can be used to map these devices at E8-ED. All other I/O addresses are available for use by off-board I/O devices.

The standard and alternate address are shown below with the functions that they control. Each of these functions is covered in detail later in this section.

Alternate I/O Address	As Shipped	Port Type	Description
E8-EA	F0-F2	I/O	Counter/Timer Channel 0-2
EB	F3	OUT	Counter/Timer Mode Register
EC	F4	I/O	Interrupt and GP Register
ED	F5	OUT	MEMEX Control

Figure 3-1. I/O Port Mapping

EXTERNAL I/O LINES

The VL-7804A includes two external I/O lines; one output line, and one input line. These lines are accessed through bits in the General Purpose Control and Status registers. These registers (one read and one write) are normally located at I/O address F4. They can be optionally jumpered to I/O address ED. Both of these lines are present on connector J1. Care must be taken when using these signals as they both go through inverting buffers.

Refer to Figure 2-1 for the connector pinout. The external I/O lines are named EXT-OUT and EXT-IN.

The external input line is read at bit D4 of the G. P. Status Register (see Figure 3-10). This register can be read at any time. Since this input is inverting, a low bit represents a high signal on the external input. This input has a pull-up resistor attached and will be high (reading a zero) when no input signal is attached to the connector pin.

The external output line is controlled through bit D4 of the G. P. Control Register (see Figure 3-9). Care must be taken when writing to this register since the state of the other bits at this port should not be changed from the last time they were written. Since this output is inverting, writing a low bit will cause the output line to go high.

MEMEX CONTROL

The MEMEX (memory expansion) signal on the STD BUS is normally used to select between two different 64K byte memory banks or maps. It can be used to expand the available memory, or to control a bootstrap PROM.

Memory cards in the system can choose to operate with MEMEX low (standard map), MEMEX high (secondary map), or ignore MEMEX (both maps).

In order for the MEMEX signal to be controlled by the VL-7804A board, jumper V8 must be installed. Jumper V7 determines the state of MEMEX at power-up and whether data is inverted when written to the MEMEX control port. The effect of the V7 jumper is shown in Figure 3-2.

The MEMEX signal is controlled by bit 0 at the MEMEX control port (F5 as shipped). Writing a 0 or 1 to this port will set MEMEX low or high depending on the setting of jumper V7.

Note that the routine that controls (changes) the state of MEMEX must be located in shared or common memory. That is, it must be in a section of memory (RAM or ROM) that is selected both when MEMEX is low and when MEMEX is high. If the switching routine is not resident in both memory maps, the system will crash when MEMEX is changed.

Figure 3-3 shows the typical code used to control the MEMEX signal (when jumper V7a is out and V7b is in).

Jumper V7 Description	MEMEX Port	As Shipped
a - MEMEX is set high at power-up.	Inverted	a - out
b - MEMEX is set low at power-up.	True	b - IN

Figure 3-2. MEMEX Jumper Options

```
                    ;Select secondary memory area routine
0100    3E 01       SELSEC LD       A,01H           ;
0102    D3 F5              OUT      (0F5H),A        ;Output 01H to MEMEX port
0104    C9                 RET
                    ;
                    ;Select primary memory area routine
0105    3E 00       SELPRI LD       A,00H           ;
0107    D3 F5              OUT      (0F5H),A        ;Output 00H to MEMEX port
0109    C9                 RET
```

Figure 3-3. MEMEX Software Example

RESET ADDRESS

Normally the processor jumps to location 0000 at power-on or when a system reset occurs. The VL-7804A includes an option which allows the reset to occur to address F000 if desired. This option is used primarily for booting of disk based systems (i.e. CP/M) which require RAM to be located at 0000 (and the boot ROM to be located somewhere else).

The reset address option is selected with jumper V3.

When the F000 address reset option is selected, the upper four address lines will be held high whenever a power-up or reset occurs. This forces the processor to artificially address only locations F000-FFFF.

The upper address lines are released (for normal operation) by writing a one to data bit 0 in the General Purpose Control Register. This register is normally located at I/O address F4.

The procedure required for start-up in this mode is shown below.

```
                    ;F000 start-up example.
                    ORG   F000H
                    ;
F000  C3 03 F0      START  JP  S1        ;Set program counter to F003.
F003  3E 01        S1      LD  A,01H     ;and release the upper
F005  D3 F4                OUT (F4H),A  ;address lines.
                    ;
                    ;The bootstrap routine starts here
```

Figure 3-4. F000 Reset Address Start-Up Example

COUNTER/TIMER CHIP

The VL-7804A includes three 16-bit counter/timer channels. These counter/timers can be used for event counting, one-shot interval generation, square-wave and pulse waveform generation, and timed interrupt generation. Counting can be triggered or gated by internal (software) or external (hardware) events. The three counter channels are totally independent and may be simultaneously operated in identical or differing modes.

Hardware Interface

Each counter/timer channel has three hardware interface lines; a clock input, gate input, and an output signal line. All of these signals are available at the on-board 26-pin connector.

The **clock input** line is used to decrement the counter for all counting operations. The clock input for each channel may be connected to an external signal (to count at an externally determined rate, or to count each external event that occurs) or jumpered to the internal 2 MHz clock source. The internal counter is changed on the negative going (high to low) transition of the clock signal.

The **gate input** line is used to qualify the clock signal. It allows or disallows counting to occur, regardless of clock activity. The gate signal is active low. A low state allows counting to occur or start; a high state inhibits counting.

The **output signal** provides a hardware output line that is dependent on the counter's contents. Depending on the operating mode it may stay low (active) until the count period completes, or it may output a pulse at the end of the count period. The output line is an active low signal. The output line for each channel is also used to cause system interrupts when the appropriate interrupt control bit is enabled. If there is any question about interrupt occurrence the output line can be examined to confirm proper channel operation. Interrupts are set (latched) whenever the corresponding output line is low.

Internal Registers

Internally each channel has four registers- Count, Mode, Data Write, and Data Read. All registers are 16 bits wide except the 8-bit Mode Register.

The **Count Register** holds the current count. It is connected to the clock and gate input lines, and drives the output control line. Under the proper conditions it can load data from the Data Write Register, or can be read directly by the processor through the Data Read Register. A command is also available to latch the current count into the Data Read register for accurate reading of both bytes while counting is still in progress. All counting occurs in the downward direction. Normally an initial count is loaded into the register and some action occurs when the zero count is reached.

The **Mode Register** controls the operating mode for each channel. Although all mode commands occur to the same I/O address, internally each channel has its own Mode Register and each channel can be operated in a different mode.

The **Data Write Register** can be accessed by the processor. It holds data that will be loaded into the counter (upon hardware or software command, depending on the operating mode). Depending on the setting of the Data Mode bits in the Mode Register, data written to this register will be latched into the upper or lower 8 bits of the register.

The **Data Read Register** can be accessed by the processor to read data from the counter. Depending on the setting of the Data Mode bits in the Mode Register, data read from this register will be either the upper or lower 8 bits of the current count in the counter. An additional mode allows the current count to be latched into the Data Read Register so that the processor can read stable (synchronized) low and high bytes of data while the counter continues to change.

User Registers

The following registers are used to control the counter/timer channels. The port addresses for these registers are shown below. As shown, the Data Registers for each channel have their own port. The Mode and Interrupt Control registers each have a single port location. The data written to these control ports determines what channel they affect. The Interrupt Control Registers are detailed at the end of this section.

Alternate I/O Address	As Shipped	Port Type	Description
E8	F0	I/O	Channel 0 Data Register
E9	F1	I/O	Channel 1 Data Register
EA	F2	I/O	Channel 2 Data Register
EB	F3	OUT	Mode Register
EC	F4	I/O	Interrupt Control / Status

Figure 3-5. Counter/Timer I/O Ports

Mode Register

The Mode Register is the control for all the counter/timer channels. It programs each counter/timer for its operating mode (what kind of counting/timing it will do), how data will be sent to it and read from it, and whether it will operate in hexadecimal or decimal (BCD) mode. The Mode Register format is shown below.

Counter/Timer Mode Register

D7	D6	D5	D4	D3	D2	D1	D0
COUNTER SELECT		-DATA MODE-		--OPERATING MODE--			H/D

Bit	Description
D7-D6	Counter Select 00 - Counter 0 01 - Counter 1 10 - Counter 2 11 - (Invalid)
D5-D4	Data Register Mode 00 - Latched read (one time only) 01 - R/W lower byte only 10 - R/W upper byte only 11 - R/W lower then upper bytes
D3-D1	Operating Mode 000 - Mode 0: Software triggered countdown 001 - Mode 1: Hardware triggered countdown 010 - Mode 2: Rate generator (pulse generator) 011 - Mode 3: Square wave generator 100 - Mode 4: Software triggered countdown w/strobe output 101 - Mode 5: Hardware triggered countdown w/strobe output
D0	Hex/Decimal Select 0 - Hexadecimal mode 1 - Decimal (BCD) mode

Figure 3-6. Counter/Timer Mode Register

Counter/Timer Operation

To use one of the counter/timer channels it must be decided what mode will be used, and what connections (if any) will be made to the clock, gate, and output lines.

For software oriented timing, the clock input line can be jumpered to the internal 2 MHz source, and the output line can be ignored. The end of the timing period can be detected either by reading the counter (i.e.

waiting for a count of zero) or using the interrupt capability. However, to enable counting the gate input line must be held low. If no other connections will be made to the external signal lines, this can be done by inserting shorting jumpers between each gate signal and the opposing connector pin (all odd pins are grounded).

For counting of external events, the clock input should be jumpered for connection to the external signal. The gate input line must be connected to ground. Since the counters count down only, the value read from the Current Count Register should be inverted when counting external events or measuring time intervals. Loading an initial value of hex FF (or FFFF) to the channel, and then inverting the value read from Data Read Register (do an Exclusive OR with FF) will yield the actual event count.

Channels can be cascaded together for higher counts or longer time delays. This is done by connecting the output of the first channel to the clock input of the second channel. Each time the first channel reaches zero, it will decrement the count in the second channel.

Each channel is initialized by writing a new mode to it. The mode instruction must contain the channel number (of the channel being initialized), the data mode (the 00 mode can not be used until after the counter has started), the mode number, and the hex or decimal number selection. A copy of this mode instruction should be kept in memory. If any additional writes are made to this channel's Mode Register (such as to change the data mode) the rest of the bits must be identical to the original initialization.

If interrupts will be used, then the channel's interrupt should be reset and the interrupt enable bit should be set (if it is not already). Care must be taken not to change the setting of the other bits in the Interrupt Control Register. This is most easily done by keeping a copy of the last data written to the register in memory, and adding or bring the new bit into this copy before it is written to the register.

Data is written to the counter via the Data Registers. There is one Data Register port address for each channel. Data written to this register is latched and may or may not be immediately transferred to counter (depending on the current operating mode).

The data written to the register may represent the upper or lower 8 bits of the 16-bit counter value. This depends on the setting of the data mode bits when the last mode instruction was written to this channel. If data mode 11 is selected, then two bytes may be written in sequence. The first will be the lower byte, and the second will be the high byte. In this mode data is never transferred to the counter until both low and high bytes have been written into the register. The low/high byte sequencer is reset whenever a new operating mode is selected. If only low or high data is written to the Data Register (data modes 01 or 10) then the previously latched low or high byte remains in the Data Register and will be transferred to the counter with the other 8 bits of new data. Data mode 00 effects only reading of data from the counter and has no effect on the previously set data mode for writing of data.

Data can be read from the counter via the Data Registers. There is one Data Register port address for each channel. Data read via this register is normally not latched but comes directly from the the counter. A latched read mode is available as discussed below. Data should not be read from the counter until it has been started (i.e. data written to it from the Data Write Register and one rising and falling edge of the clock has occurred). Data read before the counter has started may be invalid.

Data read from this register may represent the upper or lower 8 bits of data from the 16-bit counter. This depends on the setting of the Data Mode bits when the last mode instruction was written to this channel. If Data Mode 11 is selected, then two bytes should be read in sequence. The first will be the lower byte, and the second will be the high byte. The low/high byte sequencer is reset whenever a new operating mode is selected. When reading a full 16-bit value from the counter, data mode 00 can be used to latch the counter value into the Read Register. This prevents errors from reading high and low data bytes that are out of sync because the counter has changed between the two reads. Latching of the data from the counter into the Data Read Register occurs when the data mode 00 command is written to the mode register. The data can then be read by the processor when desired. The Data Mode 00 command latches the data for a single read only. It must be written again if another latched read is desired. The data available from the Data Read Register after the latch command occurs will be either the low byte, high byte, or low and high bytes (two reads) depending on the last setting of the Data Mode bits.

Each counter may be operated in hexadecimal or decimal (BCD) mode. Examples of each are shown below.

Count Mode	**Maximum Count**	**17 Step Count Example**
Hexadecimal	FFFF	11,10,0F,0E,0D,0C,0B,0A,09,08,07...01,00
Decimal (BCD)	9999	17,16,15,14,13,12,11,10,09,08,07...01,00

Figure 3-7. Counting Modes

Operating Modes

The operating mode is set by bits D3-D1 in the Mode Register. Each of the available operating modes is described in detail below.

Mode 0: Software triggered countdown (one-shot). The output is set low when the mode instruction is written. Counting begins when an initial value is written to the Data Register of the corresponding channel. The output stays low until the counter reaches zero. The output then goes high and stays high until another new count is written or a new mode selected. Writing to the Data Register during counting stops the counter. It then waits for another data value to be written which it loads into the counter and restarts counting.

Mode 1: Hardware triggered countdown (retriggerable one-shot). The output goes low and counting begins on the 1st clock following the falling edge of the gate input (the gate is the trigger). The output goes high when the count reaches zero.

If a new value is written to the Data Write Register while counting is occurring it will have no effect on the current output period, however, the new value will be loaded to the counter and used for the next output period when the next trigger (gate input) occurs. The one-shot action is retriggerable; the output will remain low for the full count after any falling edge of the gate input.

Mode 2: Rate generator (pulse generator). The output will go low for a single pulse (one clock period long) at the end of each count period. The count value will then be automatically reloaded to the counter and the process will be repeated indefinitely.

If a new value is written to the Data Write Register while counting is occurring it will have no effect on the current output period, however, the new value will be used for all future output periods. If the gate input is forced high then the output will go high. When the gate goes low the counter will start again from the initial value. This allows the gate to synchronize the counter. When the operating mode is originally set, the output will remain high until an initial count is written to the Data Register. This allows the the output to be synchronized by software.

Mode 3: Square wave generator. This mode is similar to Mode 2 except that the output goes low for half of the count and goes high for the other half. Even values will result in symmetrical output. Odd values will result in high output for (N+1)/2 counts and low output for (N-1)/2 counts.

Mode 4: Software triggered countdown with strobe output. The output line will be high after the mode is set. Counting begins when the value is written to the Data Register. The output will go low for one clock period when the counter reaches zero. The output will then go high again and the process will be automatically repeated. If a new value is written to the Data Register while counting is occurring the present countdown will not be affected, however, the new value will be used for all future output periods.

Mode 5: Hardware triggered countdown with strobe output. Similar to Mode 1 but the output only goes low for a short pulse (one clock period) when the clock reaches zero. The counter will start counting after the falling edge of the gate input (the gate is the trigger). The counter is retriggerable. The output pulse will not occur until a full count after any falling edge of the gate input.

As noted in the mode descriptions above, the gate input signal can enable and disable the counting function. A summary of the gate inputs effects is shown below.

Mode	High or rising	Falling	Low
0	Disables counting	-	Enables counting
1	-	Initiates counting Resets output on next clock	-
2	Disables counting Sets output high	Reloads counter Starts counting	Enables counting
3	Disables counting Sets output high	Initiates counting	Enables counting
4	Disables counting	-	Enables counting
5	-	Initiates counting	-

Figure 3-8. Gate Input Functions

INTERRUPTS

The counter/timer channels can all provide interrupts to the processor if desired. All interrupts are disabled at power-up or system reset. They can be enabled by writing to the General Purpose Control Register as shown in Figure 3-9.

Since the 7804A interrupts are polled (not vectored), the General Purpose Status Register must be read to determine the source of the interrupt. The format of this register is shown in Figure 3-10.

In use an interrupt will occur when the output line on any counter/timer goes low for a channel that has the interrupts enabled. The interrupt will remain until it is reset.

Interrupts are reset by writing to bits D7-D5 on the G. P. Control Register. Since the reset circuitry is edge sensitive, a 0 and then a 1 must be written to the channel being reset. The interrupt reset will not occur unless the corresponding counter/timers output line is currently high. Care must be taken not to disturb the current settings of the other bits in this control register when doing a reset.

The General Purpose Control (out) and Status (in) registers are located at I/O address F4 as shipped. Alternate jumpering can place them at I/O address EC.

Since the 7804A interrupts are not vectored, and are rather clumsy to use, it should be noted that the output signal line from each counter-/timer can be connected to a vectored interrupt input elsewhere in the system if desired.

GEN. PURPOSE CONTROL REGISTER							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT2 RST	INT1 RST	INT0 RST	EXT OUT	INT2 ENBL	INT1 ENBL	INT0 ENBL	RESET ADDR

Bit **Description**

D7 Chan. 2 interrupt reset
Write 0 then 1 to reset the interrupt latch

D6 Chan. 1 interrupt reset
Write 0 then 1 to reset the interrupt latch

D5 Chan. 0 interrupt reset
Write 0 then 1 to reset the interrupt latch

D4 External output line control (inverting)
1 - Sets output line low
0 - Sets output line high

D3 Chan. 2 interrupt enable
0 - Disable this interrupt
1 - Enable interrupts from this channel

D2 Chan. 1 interrupt enable
0 - Disable this interrupt
1 - Enable interrupts from this channel

D1 Chan. 0 interrupt enable
0 - Disable this interrupt
1 - Enable interrupts from this channel

D0 Reset address control.
1 - Release upper address lines after start-up to F000

Figure 3-9. General Purpose Control Register

GEN. PURPOSE STATUS REGISTER							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**DO**
INT2 STAT	INT1 STAT	INTO STAT	EXT INP	-	-	-	-

Bit **Description**

D7 Chan. 2 interrupt status
=1 when interrupt has occurred

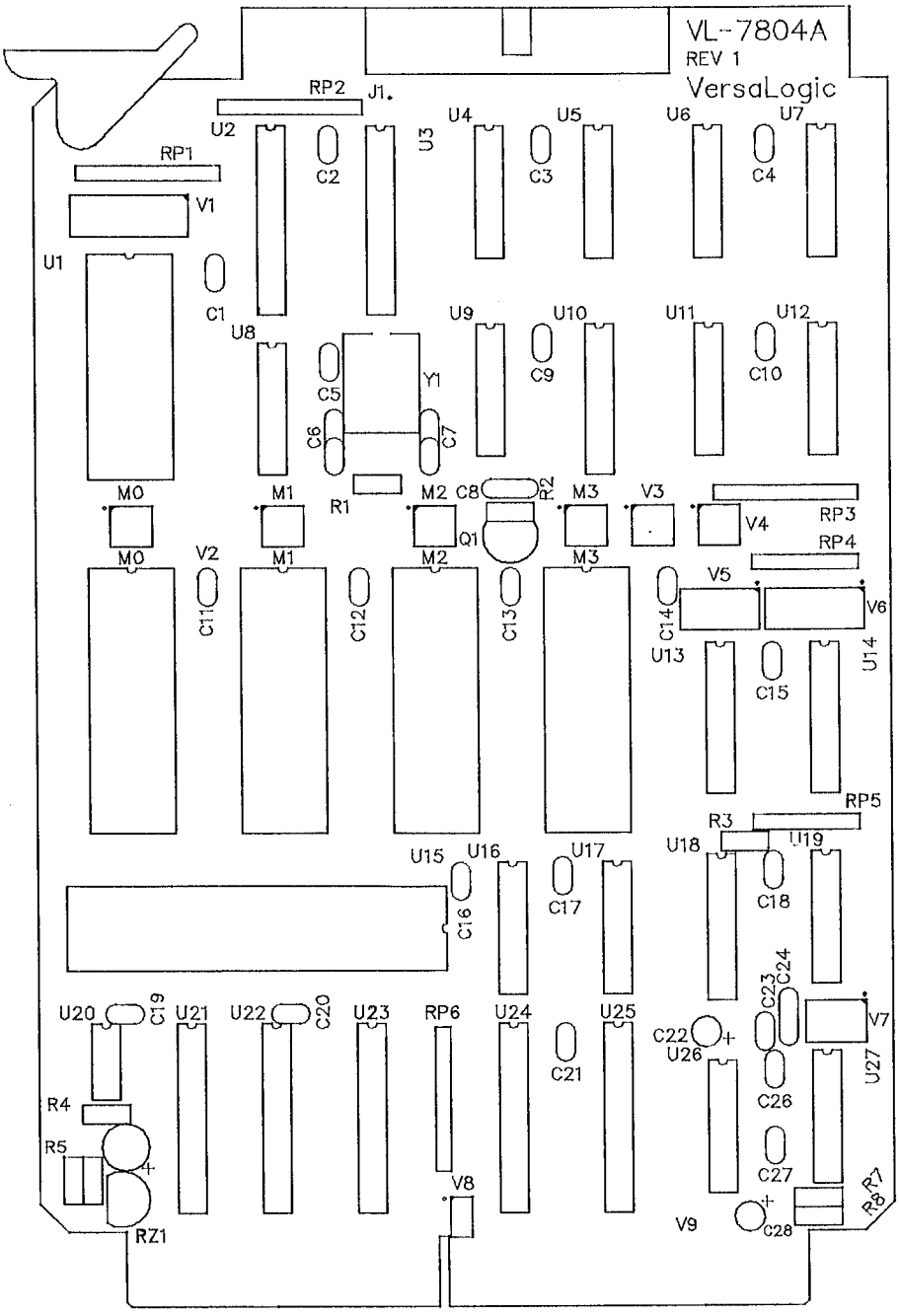
D6 Chan. 1 interrupt status
=1 when interrupt has occurred

D5 Chan. 0 interrupt status
=1 when interrupt has occurred

D4 External input line status (inverting)
=1 when input signal is low
=0 when input signal is high

D3-DO (Not used)

Figure 3-10. General Purpose Status Register


VL-7804A
REV 1
VersaLogic
J1
RP1
RP2
RP3
RP4
RP5
RP6
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C26
C27
C28
Y1
R1
R2
R3
R4
R5
R7
R8
Q1
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V3
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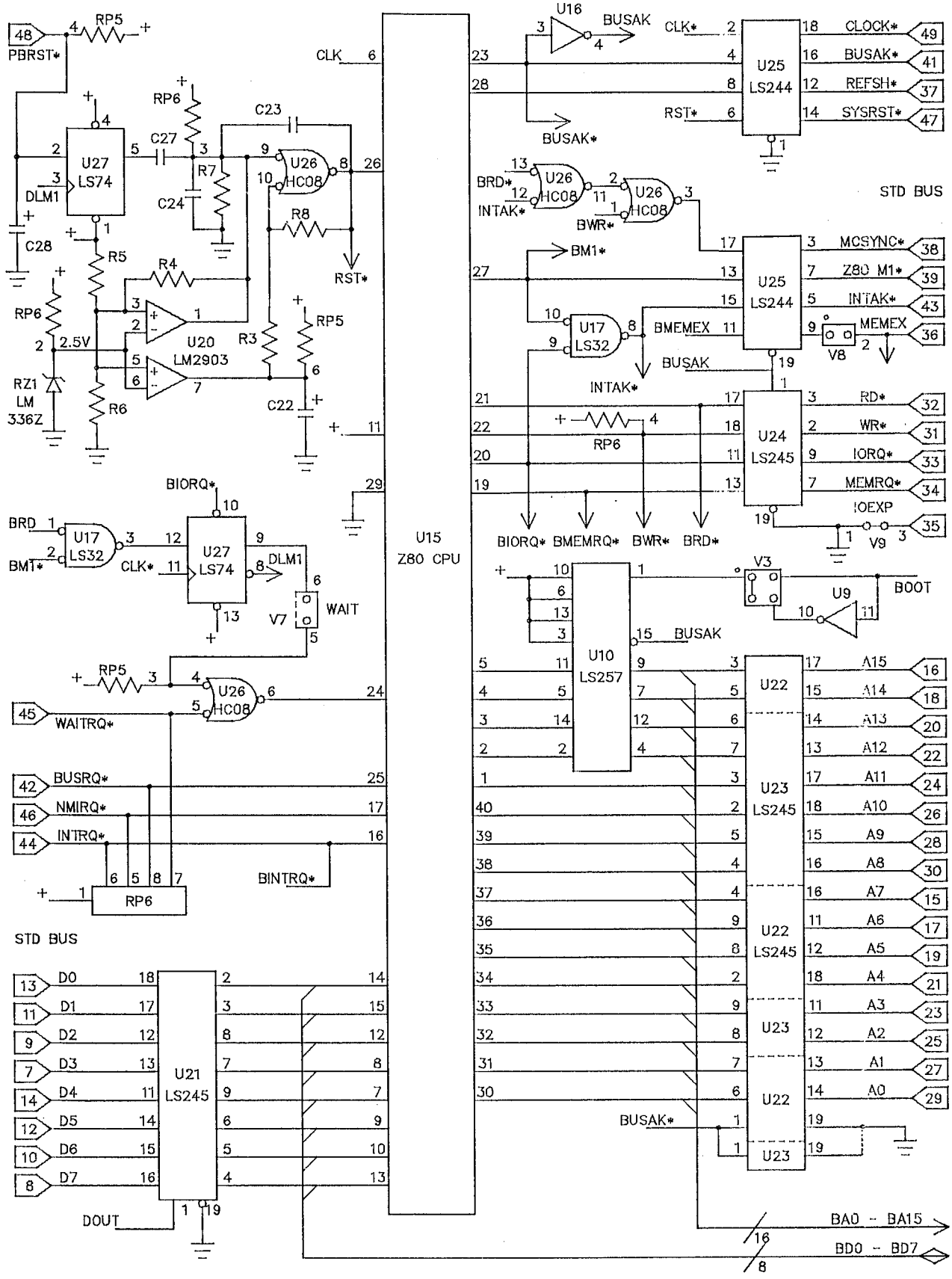
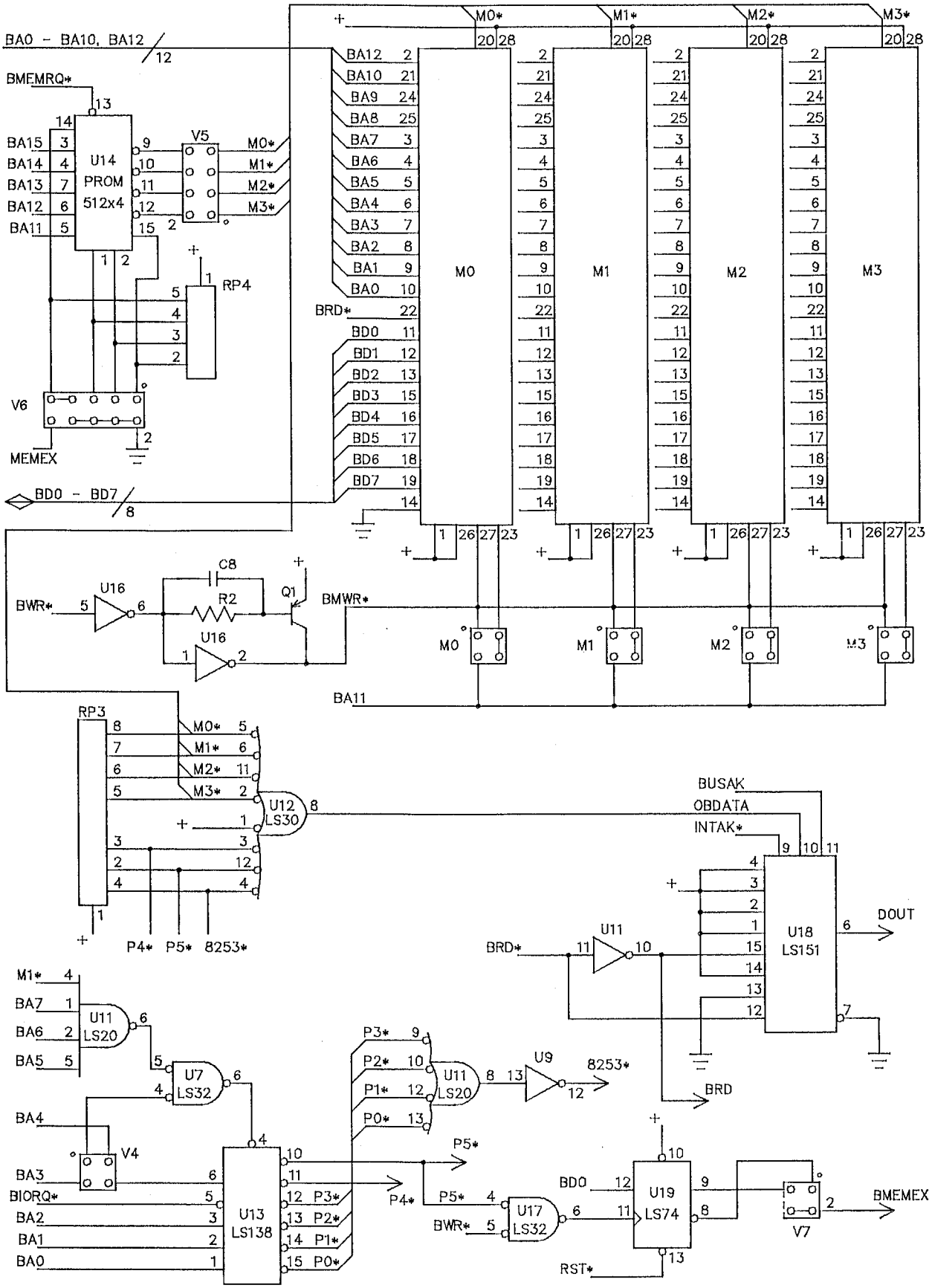
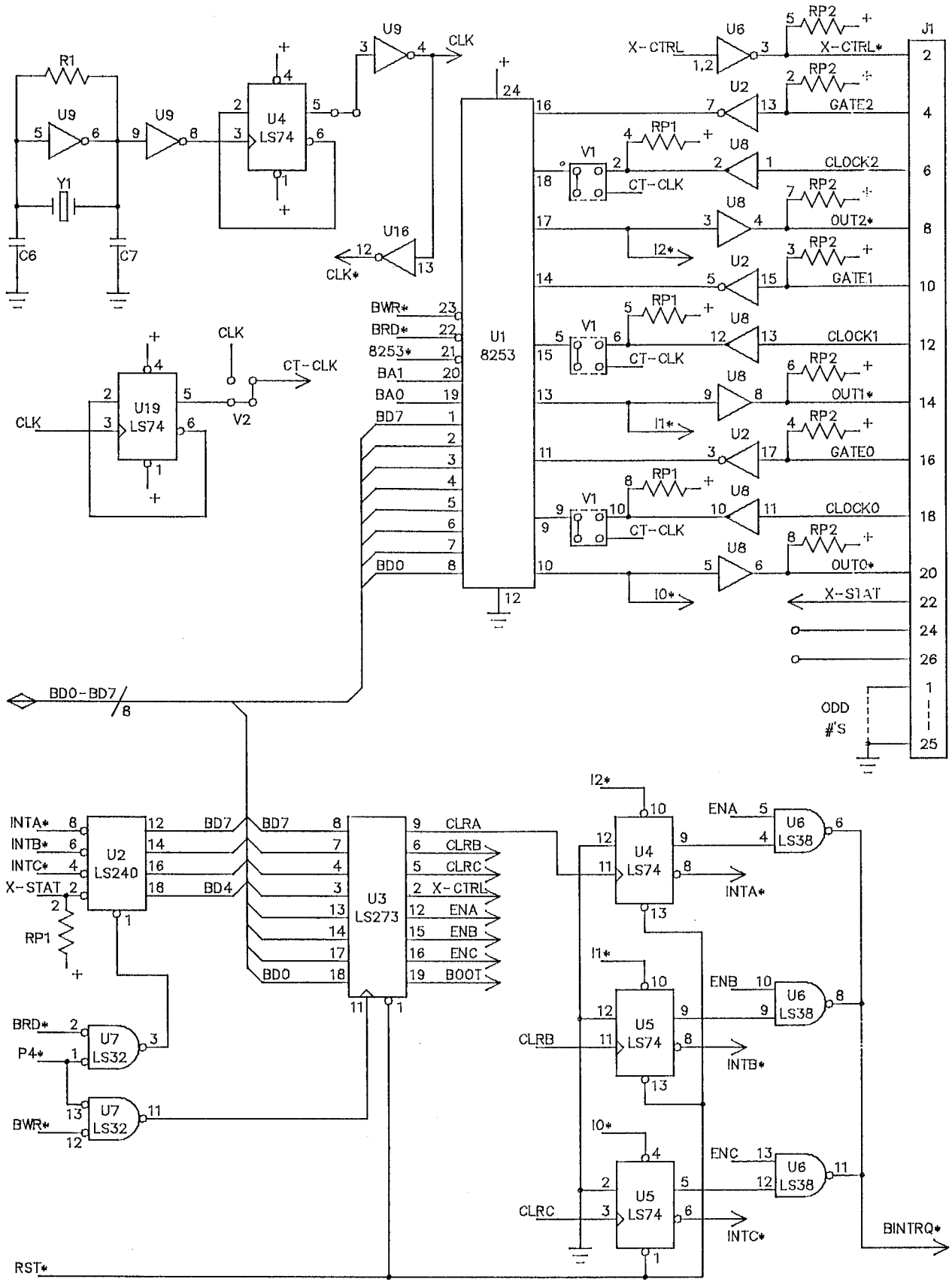
V6
V7
V8
V9
M0
M1
M2
M3


PBRST*
RP5
RP6
C23
C27
C24
R7
R8
U27 LS74
DLM1
C28
R5
R4
RP6
2.5V
U20 LM2903
R3
RP5
RZ1 LM 336Z
R6
C22
RST*
CLK
U15 Z80 CPU
U16
BUSAK
BUSAK*
CLK*
RST*
U25 LS244
CLOCK*
BUSAK*
REFSH*
SYSRST*
STD BUS
BRD*
INTAK*
BWR*
U26 HC08
BM1*
MCSYNC*
Z80 M1*
INTAK*
MEMEX
V8
U17 LS32
BMEMEX
BUSAK
INTAK*
U24 LS245
RD*
WR*
IORQ*
MEMRQ*
IOEXP
V9
BIORQ*
BMEMRQ*
BWR*
BRD*
BRD
BM1*
CLK*
WAIT
V7
V3
BOOT
U9
U10 LS257
BUSAK
WAITRQ*
BUSRQ*
NMIRQ*
INTRQ*
BINTRQ*
U22 LS245
U23 LS245
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
U21 LS245
D0
D1
D2
D3
D4
D5
D6
D7
DOUT
BA0 - BA15
BD0 - BD7


BA0 - BA10, BA12
12
BMEMRQ*
U14
PROM
512x4
BA15
BA14
BA13
BA12
BA11
V5
M0*
M1*
M2*
M3*
RP4
V6
MEMEX
BD0 - BD7
8
BA12
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
BRD*
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
M0
M1
M2
M3
C8
R2
Q1
U16
BWR*
BMWR*
BA11
RP3
U12
LS30
P4*
P5*
8253*
BUSAK
OBDATA
INTAK*
U18
LS151
DOUT
BRD*
BRD
U11
LS20
U7
LS32
BA4
V4
BA3
BIORQ*
BA2
BA1
BA0
U13
LS138
P3*
P2*
P1*
P0*
U9
8253*
U17
LS32
BDO
U19
LS74
RST*
V7
BMEMEX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U9
U9
U9
U4
LS74
Y1
C6
C7
U16
CLK
CLK*
U19
LS74
CT-CLK
V2
U1
8253
BWR*
BRD*
8253*
BA1
BA0
BD7
BD0
U6
X-CTRL
X-CTRL*
U2
GATE2
RP1
V1
CT-CLK
U8
CLOCK2
OUT2*
I2*
GATE1
CLOCK1
OUT1*
I1*
GATE0
CLOCK0
OUT0*
I0*
X-STAT
RP2
J1
ODD
#'S
BD0-BD7
8
U2
LS240
INTA*
INTB*
INTC*
X-STAT
RP1
BD7
BD4
U3
LS273
CLRA
CLRB
CLRC
X-CTRL
ENA
ENB
ENC
BOOT
U7
LS32
BRD*
P4*
BWR*
U4
LS74
U5
LS74
U5
LS74
U6
LS38
U6
LS38
U6
LS38
INTA*
INTB*
INTC*
BINTRQ*
RST*

VL-7804A PARTS LIST
Z80 CPU Board

Capacitors

C1-C5, C9-C21, C26, C27	.01 uf ceramic
C6, C7	22 pf NPO ceramic
C8, C24	680 pf NPO ceramic
C22, C28	2.2 uf electrolytic, radial
C23	270 pf NPO ceramic
C25	22 uf electrolytic, radial

Integrated Circuits

U1	8253-5
U2	74LS240
U3	74LS273
U4, U5, U19, U27	74LS74
U6	74LS38
U7, U17	74LS32
U8	7417
U9, U16	74HCT04
U10	74LS257
U11	74LS20
U12	74LS30
U13	74LS138
U14	I512X4C (Bipolar PROM "C")
U15	Z80-A CPU
U18	74LS151
U20	LM2903
U21, U22, U23, U24	74LS245

U25	74LS244
U26	74HC08

Resistors

R1	1M ohm, 1%, 1/4W
R2, R5	10K ohm, 1%, 1/4W
R3	2K2 ohm, 5%, 1/4W
R4	215K ohm, 1%, 1/4W
R6, R7	12.1K ohm, 1%, 1/4W
R8	27K ohm, 5%, 1/4W
RP1, RP2, RP6	4K7 ohm, 7 resistor SIP
RP3	1K ohm, 7 resistor SIP
RP4, RP5	10K ohm, 5 resistor SIP

Semiconductors

Q1	2N2907
RZ1	LM336Z-2.5V
Y1	8.000 MHz crystal

Miscellaneous

J1	26 pin R/A latching header

Section 4
REFERENCE

STD Bus Pinout

Connections from the VL-7804A to the STD Bus are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7804A.

Component Side				Solder Side			
Pin	**Signal**	**Flow**	**Description**	**Pin**	**Signal**	**Flow**	**Description**
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	-	-5V or bat. backup	6	-5V	-	-5V power
7	D3	I/O	Data bus	8	D7	I/O	Data bus
9	D2	I/O	Data bus	10	D6	I/O	Data bus
11	D1	I/O	Data bus	12	D5	I/O	Data bus
13	D0	I/O	Data bus	14	D4	I/O	Data bus
17	A6	Out	Address bus	18	A14	Out	Address bus
19	A5	Out	Address bus	20	A13	Out	Address bus
21	A4	Out	Address bus	22	A12	Out	Address bus
23	A3	Out	Address bus	24	A11	Out	Address bus
25	A2	Out	Address bus	26	A10	Out	Address bus
27	A1	Out	Address bus	28	A9	Out	Address bus
29	A0	Out	Address bus	30	A8	Out	Address bus
31	WR*	Out	Write strobe	32	RD*	Out	Read strobe
33	IORQ*	Out	I/O addr. select	34	MEMRQ*	Out	Memory addr. select
35	IOEXP*	(1)	I/O expansion	36	MEMEX*	(2)	Memory expansion
37	REFRESH*	Out	Refresh timing	38	MCSYNC*	Out	Machine cycle sync.
39	STATUS1*	Out	Z80 M1*	40	STATUS0*	-	CPU status
41	BUSAK*	Out	Bus acknowledge	42	BUSRQ*	In	Bus request
43	INTAK*	Out	Interrupt acknowl.	44	INTRQ*	In	Interrupt request
45	WAITRQ*	In	Wait request	46	NMIRQ*	In	Non-maskable int.
47	SYSRESET*	In	System reset	48	PBRESET*	In	Push button reset
49	CLOCK*	Out	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	(3)	Priority chain out	52	PCI	(3)	Priority chain in
53	AUXGND	-	±12 volt ground	54	AUXGND	-	±12 volt ground
55	AUX+V	-	+12 volt input	56	AUX-V	-	-12 volt input

Notes:
* Denotes an active low signal.
1) Jumper option. Normally strapped to ground.
2) Jumper option. Normally an output.
3) PCO and PCI are connected to each other.
\- All address, data, and status lines (except 37, 41, 47 and 49) can be driven by another source while BUSAK* is active. DMA can be performed to on-board memory devices.

DECIMAL / HEX / ASCII CONVERSION CHART

The chart below is useful for both ASCII and decimal/hex conversion. The "^" symbol is used to denote control characters. "^A" represents control A, etc.

Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL	32	20		64	40	@	96	60	`
1	01	^A SOH	33	21	!	65	41	A	97	61	a
2	02	^B STX	34	22	"	66	42	B	98	62	b
3	03	^C ETX	35	23	#	67	43	C	99	63	c
4	04	^D EOT	36	24	$	68	44	D	100	64	d
5	05	^E ENQ	37	25	%	69	45	E	101	65	e
6	06	^F ACK	38	26	&	70	46	F	102	66	f
7	07	^G BEL	39	27	'	71	47	G	103	67	g
8	08	^H BS	40	28	(	72	48	H	104	68	h
9	09	^I HT	41	29	)	73	49	I	105	69	i
10	0A	^J LF	42	2A	*	74	4A	J	106	6A	j
11	0B	^K VT	43	2B	+	75	4B	K	107	6B	k
12	0C	^L FF	44	2C	,	76	4C	L	108	6C	l
13	0D	^M CR	45	2D	-	77	4D	M	109	6D	m
14	0E	^N SO	46	2E	.	78	4E	N	110	6E	n
15	0F	^O SI	47	2F	/	79	4F	O	111	6F	o
16	10	^P DLE	48	30	0	80	50	P	112	70	p
17	11	^Q DC1	49	31	1	81	51	Q	113	71	q
18	12	^R DC2	50	32	2	82	52	R	114	72	r
19	13	^S DC3	51	33	3	83	53	S	115	73	s
20	14	^T DC4	52	34	4	84	54	T	116	74	t
21	15	^U NAK	53	35	5	85	55	U	117	75	u
22	16	^V SYN	54	36	6	86	56	V	118	76	v
23	17	^W ETB	55	37	7	87	57	W	119	77	w
24	18	^X CAN	56	38	8	88	58	X	120	78	x
25	19	^Y EM	57	39	9	89	59	Y	121	79	y
26	1A	^Z SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL