Reference Manual

VL-7601a
VL-7602a
VL-7603a
VL-7604a
VL-76CT04a

64-Line TTL Interface
Card for the STD Bus

STD

VERSALOGIC
CORPORATION

VL-7601a
VL-7602a
VL-7603a
VL-7604a
VL-76CT04a

64-Line TTL Interface Card for the STD Bus

Model VL-7601-4a & VL-76CT04a

64-Line TTL Interface Card for the STD Bus

REFERENCE MANUAL

VL-7601a Rev. 0.00
VL-7602a Rev. 0.00
VL-7603a Rev. 0.00
VL-7604a Rev. 0.00
VL-76CT04a Rev. 0.00
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M7601/4

Models VL-7601A Through VL-7604A
64-Line TTL Interface Cards

REFERENCE MANUAL

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Section 1
OVERVIEW

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7601A, VL-7602A, VL-7603A, and VL-7604A interface cards. These cards provide 64 TTL type I/O lines for general purpose interfacing requirements.

The four boards are similar in function, except that the VL-7601A, '02A and '03A boards are manufactured with different interfacing configurations of the 64 I/O lines. The VL-7604A includes all of the circuitry needed for any combination of 64 input or output lines and can be configured as needed by the user. The board types are summarized below.

VL-7601A: 32 input and 32 line output lines
VL-7602A: 64 output lines
VL-7603A: 64 input lines
VL-7604A: 64 user configurable I/O lines

These four boards are available in standard (VL-7601/4A) and extended temperature (VL-76CT01/4) versions. Throughout this manual "VL-7601/4A" refers to all the versions of these boards.

OVERVIEW

The VL-7601/4A cards provide several configurations of 64 TTL input/output lines.

The VL-7601A, '02A and '03A cards are pre-configured for their I/O function. The VL-7604A card is user configurable for input or output function on each of the eight 8-bit I/O ports. I/O configuration is accomplished by physically removing or inserting selected chips from the board (one input and output chip per 8-bit port).

Each 8-bit port of non-inverting input lines can be read at any time by the system processor. Pull-up resistors are included to assure that unconnected lines do not have an undetermined state. On the VL-7604A board the input ports can also be used in conjunction with output ports to "read back" the output data. LS244 type chips with .4V hysteresis (ACT244 in the extended temperature version) are used for the data input buffers.

The output lines are non-inverting and can drive 17 LS TTL loads (6.8 ma sink, 3.5 ma CT version). LS273 type chips (HCT273 in the CT version) are used for the data output latches. On the VL-7604A board, output ports can optionally be configured with the corresponding input buffer left in place. This allows the state of the output lines for that port to be read by the processor.

External connections to the board are made through eight 16-pin connectors. Each connector interfaces eight I/O lines (one 8-bit port) to an external device. Alternating ground lines, paired with each signal line, improve noise immunity and reduce cross talk.

The VL-7601/4A uses 8-bit I/O addressing, and is compatible with all common STD Bus processor types. The IOEXP line is supported for extended I/O addressing.

The VL-7602A, '03A and '04A boards normally occupy eight consecutive I/O addresses. The VL-7601A (and the VL-7604A optionally) occupy only four I/O addresses with each address serving both an input and an output port.

The VL-7601/4A boards are fully compatible with the Pro-Log 7601/4A cards.

FEATURES

- Eight 8-bit I/O ports.
- 6.8 ma output drive (3.5 ma CT version).
- IOEXP supported.
- Individual 8-bit I/O connectors.
- Extended temperature version available.
- Universal STD Bus processor compatible.
- Plug-in replacement for Pro-Log 7601/4A.

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications

Storage Temperature:
- VL-7601/4A: -40^{o} to $+75^{o}$ C
- VL-76CT01/4A: -40^{o} to $+85^{o}$ C

Free Air Operating Temperature:
- VL-7601/4A: 0^{o} to $+65^{o}$ C
- VL-76CT01/4A: -40^{o} to $+85^{o}$ C

Power Requirements:
- VL-7601A: 5V $\pm$5% @ 230 ma typ. (all inputs high)
  5V $\pm$5% @ 270 ma typ. (all inputs low)
- VL-7602A: 5V $\pm$5% @ 185 ma typ. (all outputs high)
  5V $\pm$5% @ 215 ma typ. (all outputs low)
- VL-7603A: 5V $\pm$5% @ 280 ma typ. (all inputs high)
  5V $\pm$5% @ 355 ma typ. (all inputs low)
- VL-7604A: 5V $\pm$5% @ 450 ma typ. (all outputs high)
  5V $\pm$5% @ 540 ma typ. (all outputs low)

Power Requirements:

- VL-76CT01: 5V ±10% @ 5.5 ma typ. (all inputs high)
  5V ±10% @ 21.5 ma typ. (all inputs low)

- VL-76CT02: 5V ±10% @ 5.5 ma typ. (all outputs high)
  5V ±10% @ 5.5 ma typ. (all outputs low)

- VL-76CT03: 5V ±10% @ 5.5 ma typ. (all inputs high)
  5V ±10% @ 38.5 ma typ. (all inputs low)

- VL-76CT04: 5V ±10% @ 5.5 ma typ. (all outputs high)
  5V ±10% @ 38.5 ma typ. (all outputs low)

I/O Port Interface:

- VL-7601/4A: Low level output drive: 6.8 ma @ .35V
  High level output drive: .9 ma @ 2.7V
  Input load: 1.2 ma @ .35V (4.7K ohm pull-up)

- VL-76CT01/4A: Low level output drive: 3.5 ma @ .1V
  High level output drive: 4.0 ma @ 4.9V
  Input load .5 ma @ .1V (10K ohm pull-up)

Section 2
CONFIGURATION

JUMPER SUMMARY

Various options available on the VL-7601/4A cards are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

The function of each jumper block is detailed in Figure 2-1. Figure 2-2 shows the jumper block locations on the VL-7601/4A boards.

Note that jumpers V2 and V3 are normally not used on the VL-7601A, '02A and '03A and are hard wired (wire jumpered) on these boards.

Jumper Block	Description	As Shipped
V1	Board address. See Board Address.	Hex 00
V2	Addressing control. See Board Address.	
	a - A2 control (4-port mode only).	Ignore A2*
	b - IOEXP control.	Ignore IOEXP
V3	4 or 8-port mapping. See Mapping Mode.	
		VL-7601A: 4-port mode
		VL-7602A: 8-port mode
		VL-7603A: 8-port mode
		VL-7604A: 8-port mode

* Except VL-7601A which is jumpered to use A2.

Figure 2-1. Jumper Functions

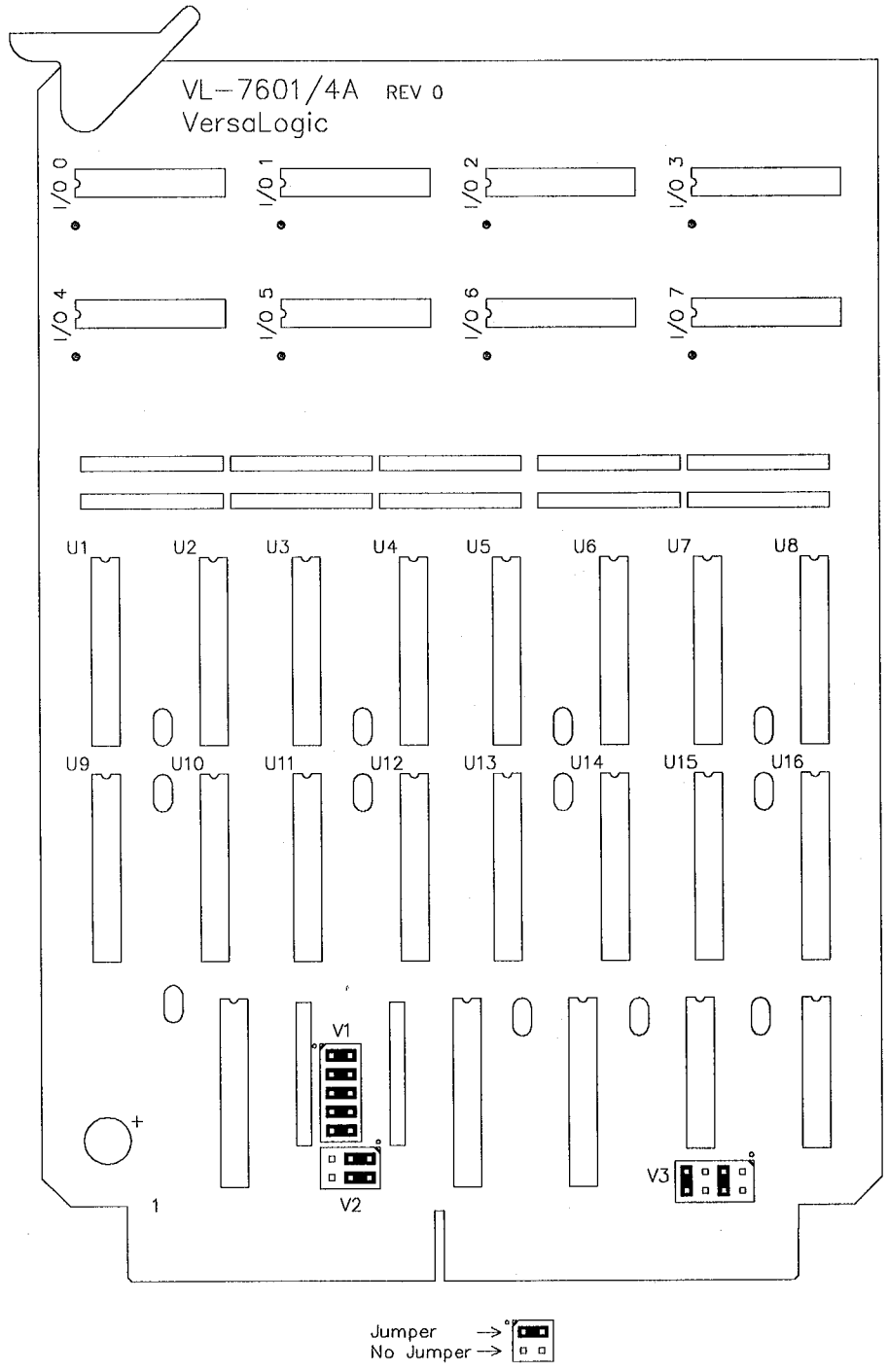


Figure 2-2. Jumper Block Locations

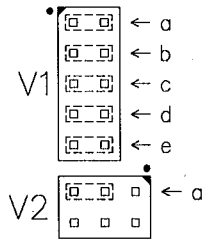
BOARD ADDRESS

The VL-7601/4A uses standard 8-bit I/O addressing to accommodate up to 32 VL-7602/4A boards (64 '01A boards) per system. The number of addressable boards can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7601/4A.

As shipped the boards are configured for a board address of hex 00. A VL-7602/4A board normally occupies eight consecutive I/O addresses (i.e. 00-07). A VL-7601A (and VL-7604A optionally) occupy four consecutive I/O addresses (i.e. 00-03).

8-Bit Address

Configure the board for the desired I/O address by referring to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e. "3" and "0" = hex address 30).



----- V1 ----				Upper
a	b	c	d	Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

V1	V2	Lower
e	a*	Digit
X	X	0
X	-	4
-	X	8
-	-	C

X = Jumper installed.
- = Jumper removed.
* Jumper V2a is used only with optional 4-port mapping on the VL-7604 board. Otherwise the lower hex digit will be 0 or 8 (per the position of V1e).

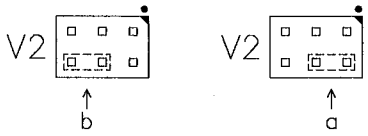
Figure 2-3. 8-Bit Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown in Figure 2-5.



Jumper Block	Description	As Shipped
V2	a - Ignore IOEXP (enable high or low).	a - IN
	b - Enable on IOEXP low.	b - out
	None - Enable on IOEXP high (no jumpers).	

Figure 2-5. IOEXP Options

MAPPING MODE (VL-7604A ONLY)

The VL-7604A normally occupies eight I/O port addresses. In this mode the I/O ports can be configured in any way desired (all inputs, all outputs, or any mix).

Optionally the board can be configured to occupy only four I/O port addresses. In this mode the I/O ports must be configured as four input channels and four output channels. This mode is advantageous only when there are many I/O boards in the system and the I/O map is becoming full. This mode can also be used to simulate a VL-7601A board which operates in the four port mode.

Unless system I/O addresses are very scarce, or a VL-7601A is being simulated, the board should be used in the 8-port mode.

8-Port Mapping

To configure the VL-7604A for 8-port mapping, jumper the board as shown below. In this mode jumper V2a is ignored when selecting the starting address for the board and should be located as shown below.

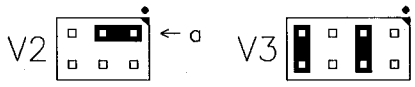


Figure 2-6. 8-Port Mapping

4-Port Mapping

To configure the VL-7604A for 4-port mapping, jumper the board as shown below. In this mode jumper V2a is used for addressing the board and should be inserted or removed from the position shown according to the addressing tables in the preceding sections.

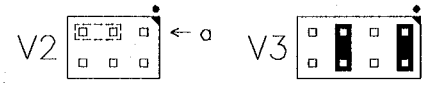


Figure 2-7. 4-Port Mapping

I/O CONFIGURATION (VL-7604A ONLY)

The I/O ports on the VL-7604A are configured for input or output by removing selected chips from the board. The board is arranged as 8 channels of 8 lines each (64 lines total). Each group of 8 lines can be configured as either input or output lines.

As shipped, with all the chips on the board, the VL-7601/4A is configured as 8 output channels. To configure any of the channels for input, the output chip (for that channel) is removed from the board.

Normally it is desirable to leave the input chip installed on channels used for output. This allows the current state of the output lines to be read if desired. If this feature is not needed, the input chips can be removed to save a small amount of power.

In the standard 8-port mode, any of the 8 channels (0-7) can be configured as inputs or outputs as desired. The figure below shows an example of a typical configuration. It shows the location of the input and output chips for each channel, and how the channels would appear on the I/O connectors.

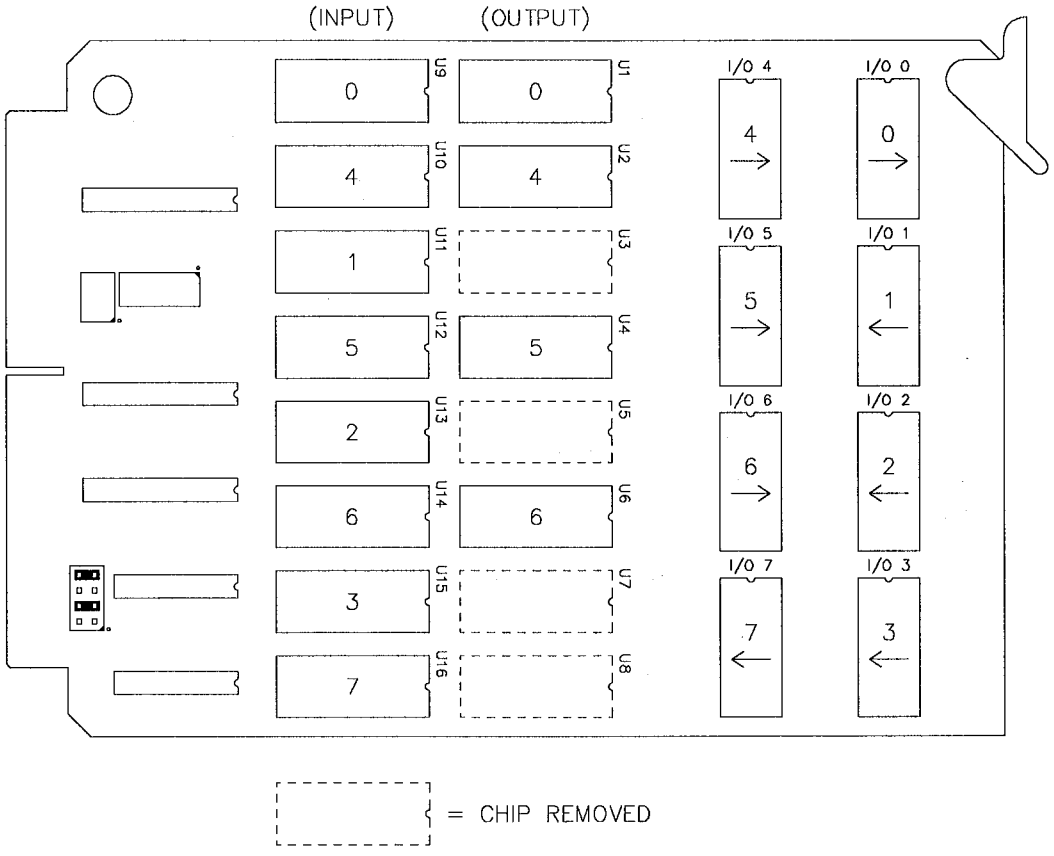


Figure 2-8. Typical I/O Configuration

Alternately the VL-7604A board can be configured as four ports (I/O addresses) with an input and an output channel at each location. This is the configuration of the VL-7601A board.

When this mode is used the the board must be configured only as shown below. Writing to channels 0 - 3 will output data on connectors I/O 0 through I/O 3. Reading channels 0 - 3 will input data from connectors I/O 4 through I/O 7.

This configuration does not allow for readback of output channel data.

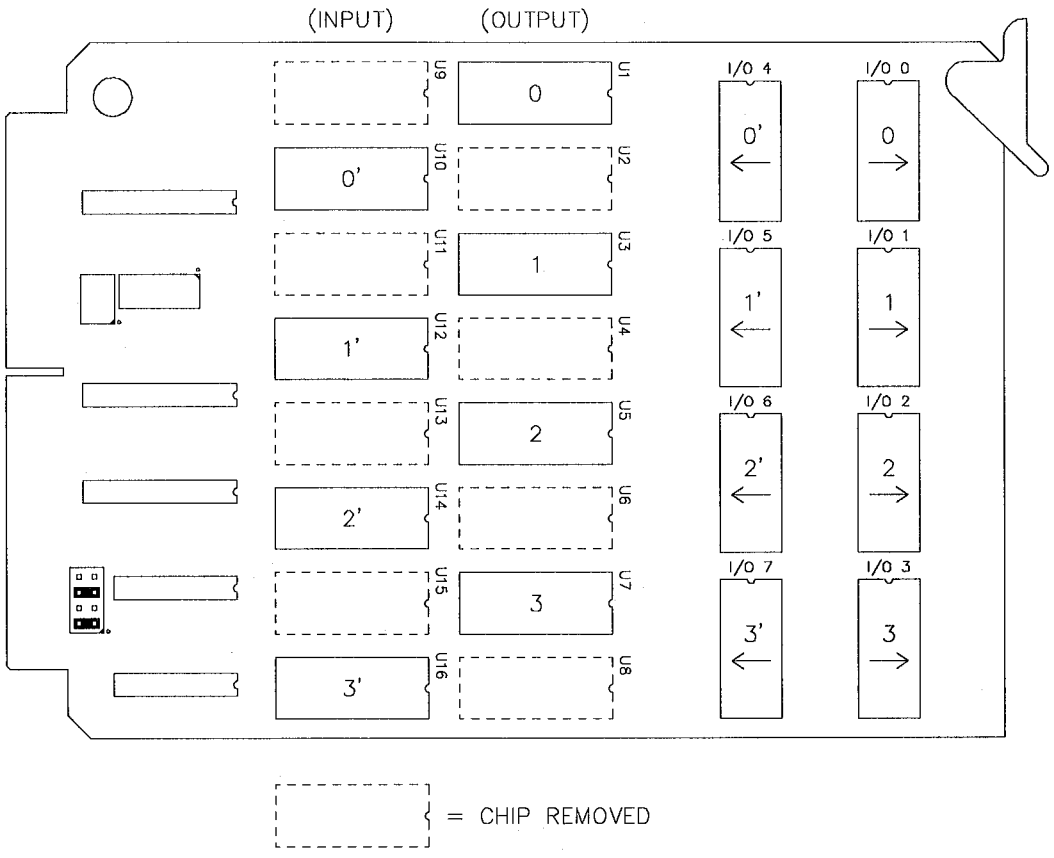


Figure 2-9. Special 4-Port Mode Configuration

Section 3
INSTALLATION

HANDLING

** CAUTION ** The VL-7601/4A cards uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The boards should also be protected during shipment or storage by placing them in a conductive bag (such as the one they were received in) or by wrapping them in metal foil.

INSTALLATION

The VL-7601/4A cards can be installed in any slot of an STD Bus card cage.

The VL-7601/4A cards do not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on these boards are connected together so that the priority chain will not be broken. They may be inserted between other boards that are using the priority chain.

** CAUTION ** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

** CAUTION ** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

EXTERNAL CONNECTIONS

Connections to the VL-7601/4A boards are made through eight 16-pin IC socket type connectors. Mating connectors for these sockets include Ansley #609-M161H, AMP #746612-3, Robinson Nugent #IDP-C163, and 3M #3416-0000.

The pinout for these connectors is shown below.

Pin	Bit
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9-16	Ground

Figure 3-1. I/O Connector Pinout

For the VL-7602A, '03A and '04A boards the connectors I/O 0 through I/O 7 correspond to I/O ports 0 through 7.

For the VL-7601A (and the VL-7604A operating in 4-port mode), connectors I/O 0 through I/O 3 correspond to output ports 0 through 3. Connectors I/O 4 through I/O 7 correspond to input ports 0 through 3.

Section 4
OPERATION

INTRODUCTION

This section includes information about the use and operation (software interface) of the VL-7601/4A cards.

RESET

All output channels are cleared (outputs set low) at power-up and whenever a system reset occurs.

I/O PORT MAPPING

The VL-7602A, '03A and '04A boards normally occupy eight I/O port addresses. Each I/O address can read or write to one 8-bit input or output channel.

The VL-7601A (and VL-7604A in optional 4-port mode) occupies four I/O port addresses. Each I/O address can read from one 8-bit input channel and write to one 8-bit output channel.

The locations of the I/O port addresses is determined by the board address, which is jumper selectable. As shipped, the board is jumpered for hex address 00.

Once the board's I/O address has been determined, the addresses of the other I/O ports can be determined as shown in Figures 4-1 and 4-2.

Port Address	Read/ Write	Chan.#	Connector
Board Address + 0	W	0	I/O 0
Board Address + 0	R	4	I/O 4
Board Address + 1	W	1	I/O 1
Board Address + 1	R	5	I/O 5
Board Address + 2	W	2	I/O 2
Board Address + 2	R	6	I/O 6
Board Address + 3	W	3	I/O 3
Board Address + 3	R	7	I/O 7

Figure 4-1. VL-7601A I/O Port Locations

Port Address	Chan.#	Connector
Board Address + 0	0	I/O 0
Board Address + 1	1	I/O 1
Board Address + 2	2	I/O 2
Board Address + 3	3	I/O 3
Board Address + 4	4	I/O 4
Board Address + 5	5	I/O 5
Board Address + 6	6	I/O 6
Board Address + 7	7	I/O 7

Figure 4-2. VL-7602A/03A/04A I/O Port Locations

READING AND WRITING DATA

The I/O buffers on the VL-7601/4A boards are non-inverting (to set an output pin low, write a zero, etc.).

Reading a VL-7601/4A port (data byte) is straightforward and requires no special considerations. Each read will transfer 8 bits of data, corresponding to 8 data lines at the port address, into the CPU. Single data bits (I/O lines) can then be tested using the AND or bit test instructions of the processor.

When writing to an I/O line, care must be taken not to change the current state of the seven other bits which appear at the same I/O port. This is usually done by keeping a copy of each port's current data in a byte of RAM. Each time a bit needs to be changed it can be ANDed or ORd into the RAM copy and the byte written out to the port. This ensures that the other lines (bits) on the output port are not inadvertently set to a new state.

SOFTWARE EXAMPLES

In systems where more than a few I/O lines are used, the task of testing or changing individual data bits at the required port can become quite cumbersome to program. The task can be made much easier with generalized subroutines that read or write to a specified I/O line. These subroutines calculate the port address and data bit involved and allow the programmer to concentrate on the decision making relating to the particular I/O line.

The routines included here allow reading of a single input line, and writing to a single output line, based on an I/O line number. This scheme numbers all the I/O lines on the board (from 0 through 63) as shown in Figure 4-3 and 4-4.

Examples of such routines are shown below. Note: These examples are supplied for general information only and may not be tested or appropriate for use in any specific application.

Port Address	Chan.#	Bit Number	Connector
Board Address + 0	0	0-7	I/O 0
Board Address + 1	1	8-15	I/O 1
Board Address + 2	2	16-23	I/O 2
Board Address + 3	3	24-31	I/O 3
Board Address + 4	4	32-39	I/O 4
Board Address + 5	5	40-47	I/O 5
Board Address + 6	6	48-56	I/O 6
Board Address + 7	7	57-63	I/O 7

Figure 4-3. I/O Port Bit Numbering

Channel Number	Data Bit D7	D6	D5	D4	D3	D2	D1	D0
00 -	7	6	5	4	3	2	1	0
01 -	15	14	13	12	11	10	9	8
02 -	23	22	21	20	19	18	17	16
03 -	31	30	29	28	27	26	25	24
04 -	39	38	37	36	35	34	33	32
05 -	47	46	45	44	43	42	41	40
06 -	55	54	53	52	51	50	49	48
07 -	63	62	61	60	59	58	57	56

Figure 4-4. Bit Numbering Detail

Assembly Language Examples

The following Z80 program example illustrates how the VL-7602/4A boards can be used in an assembly language environment. It uses subroutines to read or write to a specified line, freeing the programmer from unnecessary calculations during program construction.

When only a few I/O lines, or byte-oriented data is used, the board can be written to directly. This requires that the programmer determine the address and bit value of each I/O line used.

```
                        ;Accessing the VL-7602/03/04A by channel #.
                        ;
        0000            DIOADDR  EQU 00H            ;Board address = hex 00.
                        ;
0020                            ORG 20H
                        ;Copies of output port data, must be located in RAM
0020    00 00 00        COPY     DB  00,00,00,00,00,00,00,00   ;eight bytes
0023    00 00 00
0026    00 00

0100                            ORG  100H           ;Start of code.

                        ;Read an I/O line (state of input or output).
0100    3E 0C                   LD   A,12           ;Specify I/O line #12
0102    CD 15 01                CALL READ           ;Read it (result in A)
0105    C2 46 01                JP   NZ,ON_ACTION ;Jump somewhere if it is ON.
0108    CA 47 01                JP   Z,OFF_ACTION ;Jump somewhere if it is OFF.
                        ;
                        ;
                        ;Set an I/O line ON (output pin high).
010B    3E 09                   LD   A,9            ;Specify line #9
010D    CD 1F 01                CALL ON             ;Turn it ON
                        ;
                        ;
                        ;Set an I/O line OFF (output pin low).
0110    3E 28                   LD   A,40           ;Specify line #40
0112    CD 28 01                CALL OFF            ;Turn it OFF
                        ;
                        ;
                        ;** SUBROUTINES **
                        ;Reads a line.  Chan.# (0-63) is in A.
                        ;Returns the state of the line (0 or 1) in reg. A.
0115    CD 34 01        READ    CALL FIND           ;Convert the line #.
0118    ED 78                   IN   A,(C)          ;Read the port.
011A    A0                      AND  A,B            ;Mask for desired bit.
011B    C8                      RET  Z              ;Return if 0.
011C    3E 01                   LD   A,1            ;Or else plug with a 1
011E    C9                      RET                 ;and return.
                        ;
                        ;Sets an output line ON. Chan.# (0-63) is in reg. A.
011F    CD 34 01        ON      CALL FIND           ;Convert the line #.
0122    7E                      LD   A,(HL)         ;Get copy of output bits.
0123    B0                      OR   B              ;Set line on.
0124    77                      LD   (HL),A         ;Save copy in RAM.
0125    ED 79                   OUT  (C),A          ;Write it to the port.
0127    C9                      RET                 ;Return.
```

```
                        ;Sets an output line off. Chan.# (0-63) is in reg. A.
0128   CD 34 01   OFF     CALL FIND          ;Convert the line #.
012B   78                 LD   A,B           ;Complement B (bit mask).
012C   2F                 CPL
012D   47                 LD   B,A
012E   7E                 LD   A,(HL)        ;Get copy of output bits.
012F   A0                 AND  B             ;Set line off.
0130   77                 LD   (HL),A        ;Save copy in RAM.
0131   ED 79              OUT  (C),A         ;Write it to the port.
0133   C9                 RET                ;Return
                        ;
                        ;Computes the port address and bit mask for the
                        ;requested line # (in register A).
                        ;Returns A=0, B=bit mask, C=I/O port, HL=RAM copy addr.
0134   3C         FIND    INC  A             ;Offset line # by 1.
0135   06 01              LD   B,1           ;Initialize B for line #0.
0137   0E 00              LD   C,DIOADDR     ;Initialize C for line #0.
0139   21 20 00           LD   HL,COPY       ;Initialize HL for line #0.
013C   3D         L1      DEC  A             ;Decrement line #.
013D   C8                 RET  Z             ;Done when A=0.
013E   CB 00              RLC  B             ;Rotate bit mask.
0140   30 FA              JR   NC,L1         ;Loop if no carry.
0142   0C                 INC  C             ;Adjust port address.
0143   23                 INC  HL            ;Adjust RAM pointer.
0144   18 F6              JR   L1            ;Continue.
                        ;

0146   00         ON_ACTION  NOP             ;Dummy user routine
0147   00         OFF_ACTION NOP             ;Dummy user routine
```

BASIC Language Examples

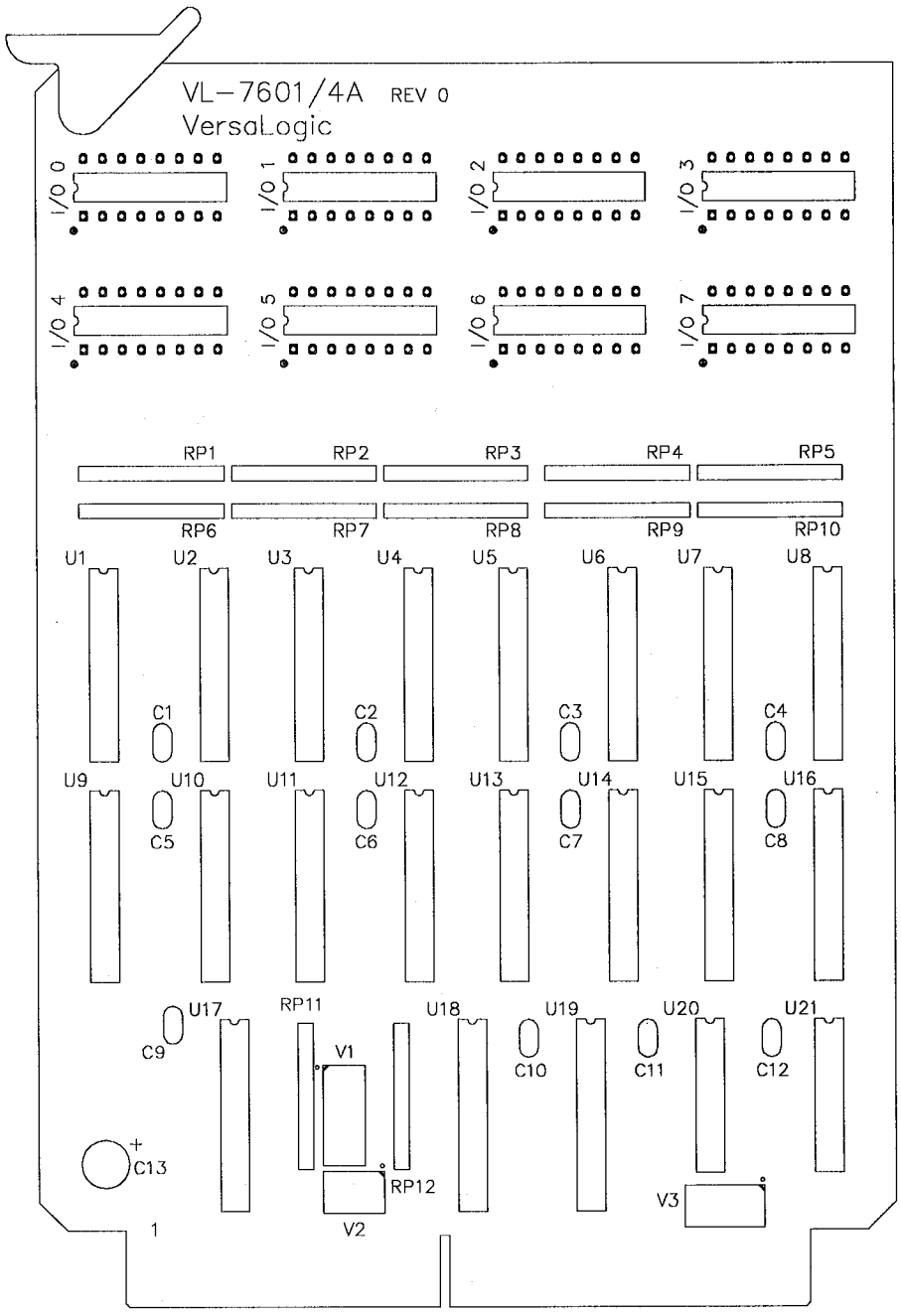
The subroutines and program fragments in the first listing below illustrate how the VL-7602/4A board can be used with standard BASICs (or other high level languages) that include logical AND, OR, and XOR functions. Microsoft's BASIC-80 is used in this example.

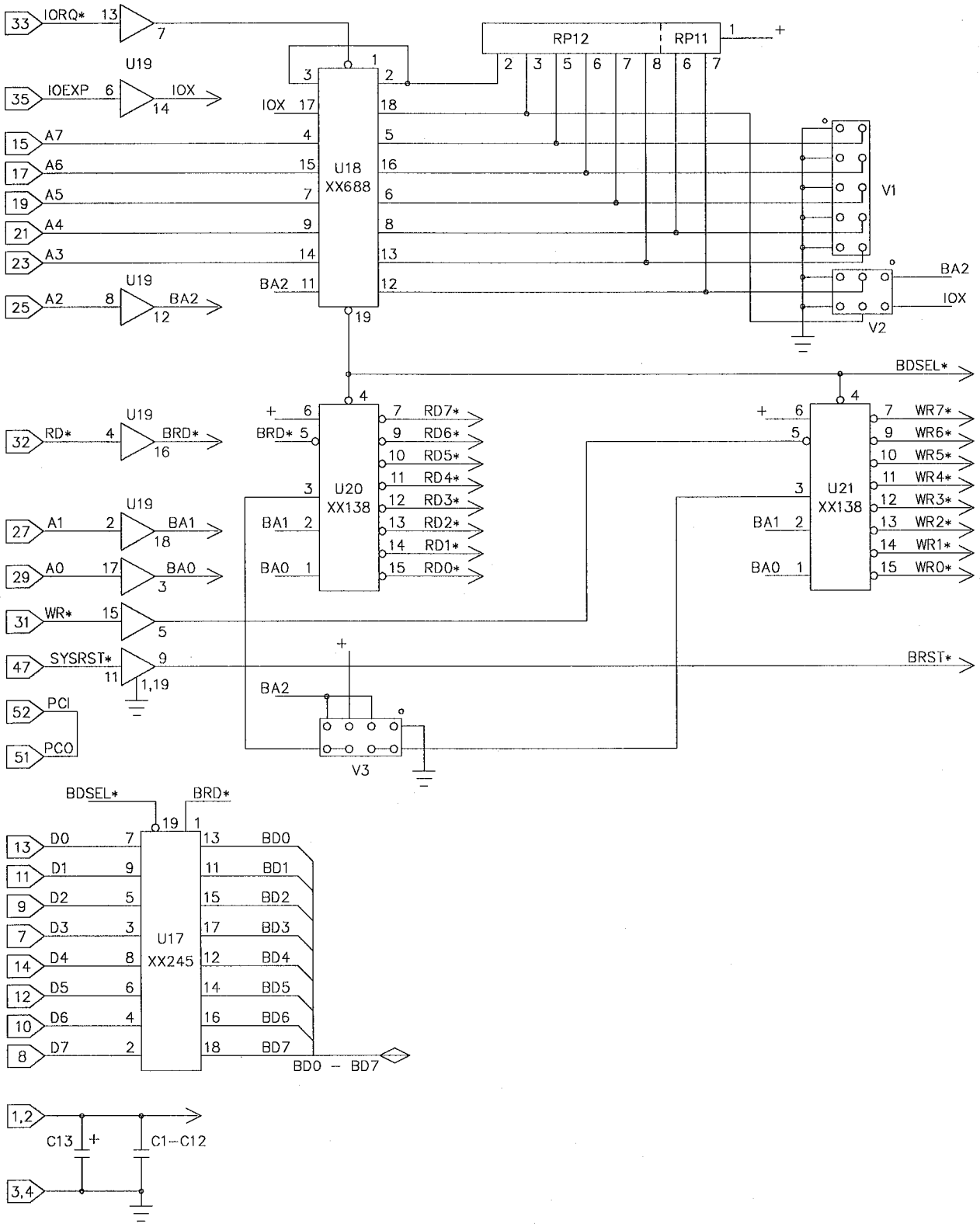
Users of VersaLogic's C4 BASIC language should refer to the second listing which shows these same functions written in C4 BASIC.

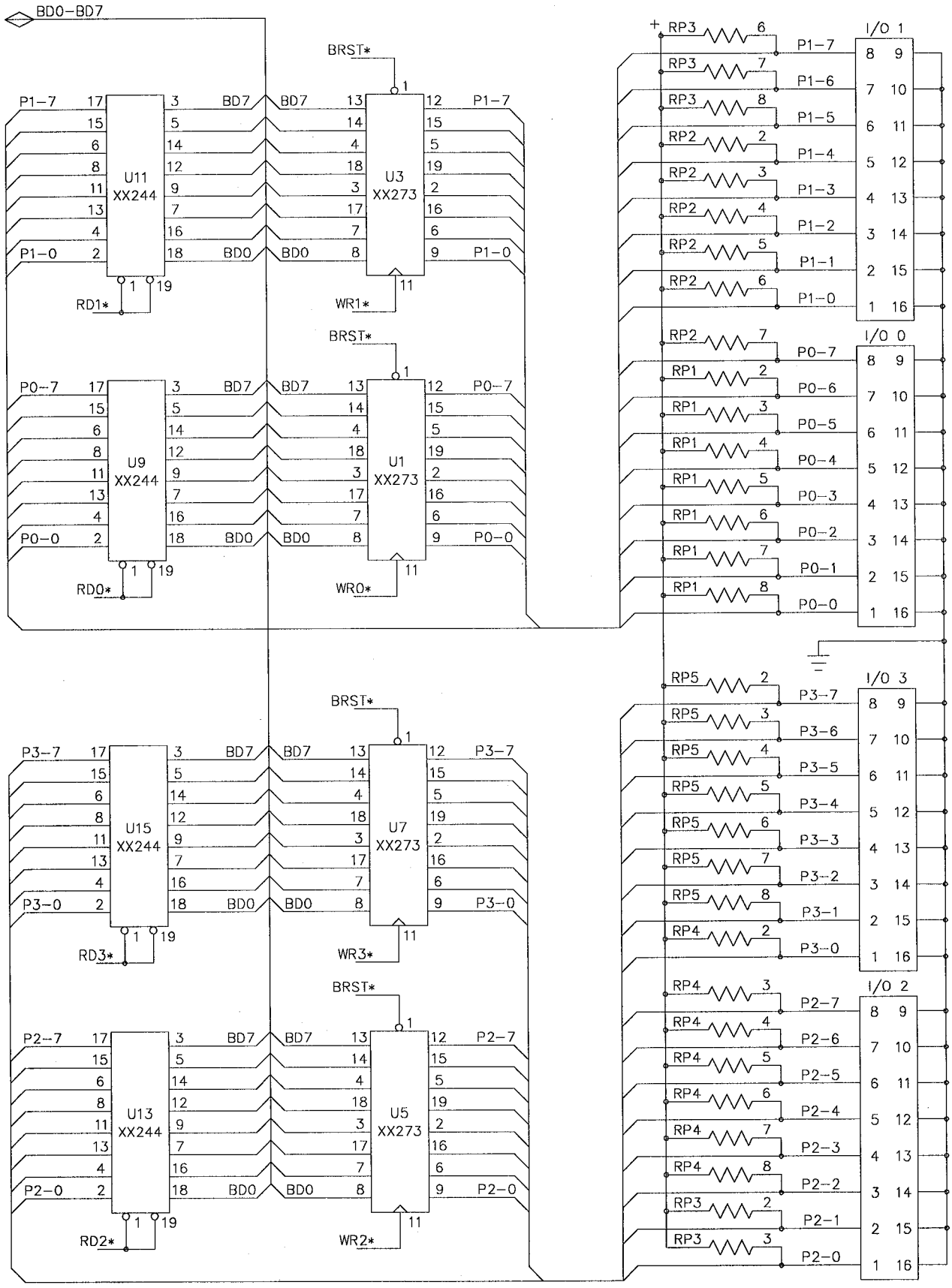
Note: These routines may not operate correctly with some BASICs or be suitable for your application.

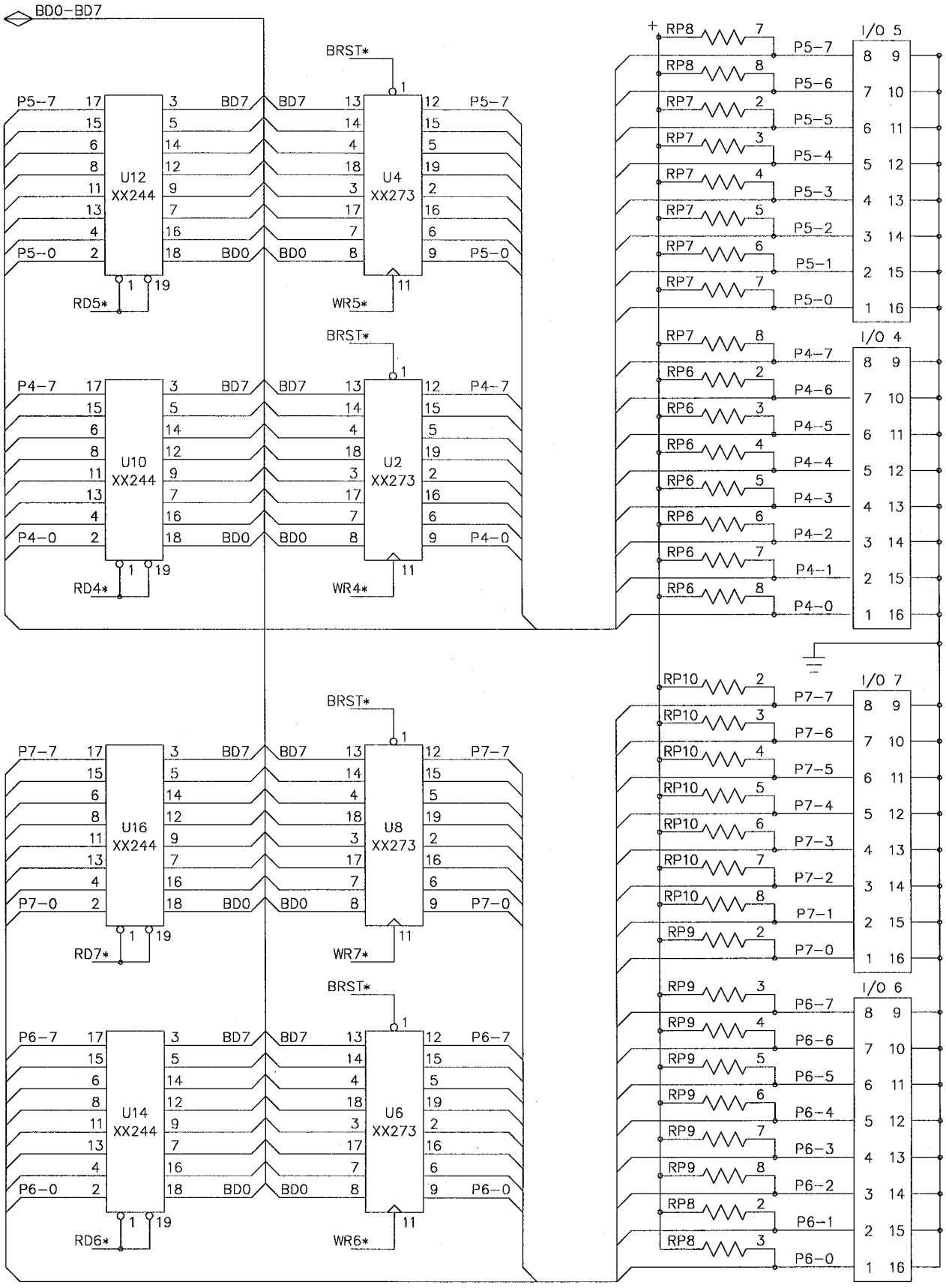
```
10 REM Microsoft BASIC-80 language example for the VL-7602/4A boards.
20 REM To read or write to single I/O lines (#0-63).
30 REM
50 REM Set address of Digital Interface (DI) board (00 hex = 00 decimal)
51 DI = 0
55 REM Initialize the output channel bytes
56 FOR I=1 to 8 : OUTBYT(I)=0 : NEXT I
 .
 .
100 REM Read line #0 and do something if it's ON.
110 LINE=0: GOSUB 510
120 IF STATE = 1 THEN GOTO 1000
 .
 .
150 REM Turn ON line #11
155 LINE=11: GOSUB 570
 .
 .
170 REM Turn line #8 OFF
171 LINE=8: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7602/4A BOARDS.
501 REM These routines are called with the line # (0-63) in "LINE".
502 REM Input data is returned in "STATE" (1=ON, 0=OFF).

510 REM Read the line in "LINE" (0-63)
520 GOSUB 600 : STATE=INP(ADDR) AND MASK : IF STATE > 0 THEN STATE=1
530 RETURN

540 REM Turn OFF line "LINE" (0-63)
550 GOSUB 600 : OUT ADDR,(OUTBYT(X) AND (255 XOR MASK)
560 RETURN

570 REM Turn ON line "LINE" (0-63)
580 GOSUB 600 : OUT ADDR,(OUTBYT(X) OR MASK))
590 RETURN

600 REM Computes port address and bit mast for routines above.
610 X=INT(LINE/8) : ADDR=DI+X : MASK=2^(LINE-8*X) : X=X+1 : RETURN
```

```
10 REM VersaLogic C4 BASIC language example for the VL-7602/4A boards.
20
50 REM Set address of Digital Interface (D1) board (00 hex)
51 D1 = &00
55 REM Initialize the output channel bytes
56 FOR I=1 to 8 : O(I)=0 : NEXT I

 .
 .
100 REM Read line 0 and do something if it's ON.
110 N=0: GOSUB 510
120 IF S = 1 GOTO 1000
 .
 .
150 REM Turn ON line 11
155 N=11: GOSUB 570
 .
 .
170 REM Turn line 31 OFF.
171 N=31: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7602/4A BOARDS.
501 REM These routines are called with the line # in "N" (0-63).
502 REM Input data is returned in "S" (1=ON, 0=OFF).

510 REM Read the line in "N"
520 GOSUB 595 : S=IN(X) AND X1 : If S>0 S=1
530 RETURN

540 REM Turn OFF line "N"
550 GOSUB 595 : OUT X,(O(X4) AND NOT (X1))
560 RETURN

570 REM Turn ON line "N"
580 GOSUB 595 : OUT X,(O(X4) OR X1)
590 RETURN

594 REM Computes port addr (X), bit mask (X1) and offset (X4) for above
595 X=(N/8)+D1 : X1=1: X2=MOD(N,8): X4=X-D1+1 : IF X2=0 RETURN
596 FOR X3 = 1 TO X2 : X1=X1*2 : NEXT X3 : RETURN
```


VL-7601/4A REV 0
VersaLogic
I/O 0
I/O 1
I/O 2
I/O 3
I/O 4
I/O 5
I/O 6
I/O 7
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
RP9
RP10
U1
U2
U3
U4
U5
U6
U7
U8
C1
C2
C3
C4
U9
U10
U11
U12
U13
U14
U15
U16
C5
C6
C7
C8
U17
RP11
U18
U19
U20
U21
C9
V1
C10
C11
C12
C13
RP12
V3
V2
1


33 IORQ* 13
7
U19
35 IOEXP 6
IOX
14
15 A7
17 A6
19 A5
21 A4
23 A3
U19
25 A2 8
BA2
12
U18
XX688
IOX 17
BA2 11
3
1
2
18
4
5
15
16
7
6
9
8
14
13
11
12
19
RP12
RP11
1
+
2 3 5 6 7 8 6 7
V1
V2
BA2
IOX
BDSEL*
4
U19
32 RD* 4
BRD*
16
U20
XX138
+ 6
BRD* 5
3
BA1 2
BA0 1
7 RD7*
9 RD6*
10 RD5*
11 RD4*
12 RD3*
13 RD2*
14 RD1*
15 RD0*
U21
XX138
+ 6
5
3
BA1 2
BA0 1
7 WR7*
9 WR6*
10 WR5*
11 WR4*
12 WR3*
13 WR2*
14 WR1*
15 WR0*
U19
27 A1 2
BA1
18
29 A0 17
BA0
3
31 WR* 15
5
47 SYSRST* 9
11
1,19
52 PCI
51 PCO
+
BA2
V3
BRST*
BDSEL*
BRD*
19
1
U17
XX245
13 D0 7
11 D1 9
9 D2 5
7 D3 3
14 D4 8
12 D5 6
10 D6 4
8 D7 2
13 BD0
11 BD1
15 BD2
17 BD3
12 BD4
14 BD5
16 BD6
18 BD7
BD0 - BD7
1,2
C13
+
C1-C12
3,4


BD0-BD7
BRST*
U11 XX244
U3 XX273
U9 XX244
U1 XX273
U15 XX244
U7 XX273
U13 XX244
U5 XX273
RD1*
WR1*
RD0*
WR0*
RD3*
WR3*
RD2*
WR2*
RP3
RP2
RP1
RP5
RP4
I/O 1
I/O 0
I/O 3
I/O 2
P1-7
P1-6
P1-5
P1-4
P1-3
P1-2
P1-1
P1-0
P0-7
P0-6
P0-5
P0-4
P0-3
P0-2
P0-1
P0-0
P3-7
P3-6
P3-5
P3-4
P3-3
P3-2
P3-1
P3-0
P2-7
P2-6
P2-5
P2-4
P2-3
P2-2
P2-1
P2-0


BD0-BD7
BRST*
U12 XX244
U4 XX273
U10 XX244
U2 XX273
U16 XX244
U8 XX273
U14 XX244
U6 XX273
RD5*
WR5*
RD4*
WR4*
RD7*
WR7*
RD6*
WR6*
RP8
RP7
RP6
RP10
RP9
I/O 5
I/O 4
I/O 7
I/O 6
P5-7
P5-6
P5-5
P5-4
P5-3
P5-2
P5-1
P5-0
P4-7
P4-6
P4-5
P4-4
P4-3
P4-2
P4-1
P4-0
P7-7
P7-6
P7-5
P7-4
P7-3
P7-2
P7-1
P7-0
P6-7
P6-6
P6-5
P6-4
P6-3
P6-2
P6-1
P6-0

VL-7601A PARTS LIST
32 Input + 32 Output TTL Interface

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1, U3, U5, U7,	74LS273
U2, U4, U6, U8, U9, U11, U13, U15	(not used)
U10, U12, U14, U16, U19	74LS244
U17	74LS245
U18	74HCT688
U20, U21	74LS138

Resistors

RP1-RP5	(not used)
RP6-RP10	4K7 ohm, 7 resistor SIP
RP11, RP12	10K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

VL-7602A PARTS LIST
64 Line TTL Output Board

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	74LS273
U9-U16	(not used)
U17	74LS245
U18	74HCT688
U19	74LS244
U20, U21	74LS138

Resistors

RP1-RP10	(not used)
RP11, RP12	10K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

VL-7603A PARTS LIST
64 Line TTL Input Board

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	(not used)
U9-U16, U19	74LS244
U17	74LS245
U18	74HCT688
U20, U21	74LS138

Resistors

RP1-RP10	4K7 ohm, 7 resistor SIP
RP11, RP12	10K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

VL-7604A PARTS LIST
64 Line TTL Interface

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	74LS273
U9-U16, U19	74LS244
U17	74LS245
U18	74HCT688
U20, U21	74LS138

Resistors

RP1-RP10	4K7 ohm, 7 resistor SIP
RP11, RP12	10K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

VL-76CT01A PARTS LIST
32 Input + 32 Output TTL Interface (Extended Temperature Version)

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1, U3, U5, U7,	74HCT273
U2, U4, U6, U8, U9, U11, U13, U15	(not used)
U10, U12, U14, U16, U19	74ACT244
U17	74ACT245
U18	74HCT688
U20, U21	74HCT138

Resistors

RP1-RP5	(not used)
RP6-RP10	10K ohm, 7 resistor SIP
RP11, RP12	100K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

VL-76CT02A PARTS LIST
64 Line TTL Output Board (Extended Temperature Version)

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	74HCT273
U9-U16	(not used)
U17	74ACT245
U18	74HCT688
U19	74ACT244
U20, U21	74HCT138

Resistors

RP1-RP10	(not used)
RP11, RP12	100K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

VL-76CT03A PARTS LIST
64 Line TTL Input Board (Extended Temperature Version)

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	(not used)
U9-U16, U19	74ACT244
U17	74ACT245
U18	74HCT688
U20, U21	74HCT138

Resistors

RP1-RP10	10K ohm, 7 resistor SIP
RP11, RP12	100K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

VL-76CT04A PARTS LIST
64 Line TTL Interface (Extended Temperature Version)

Capacitors

C1-C12	.01 uf ceramic
C13	22 uf electrolytic, radial

Integrated Circuits

U1-U8	74HCT273
U9-U16, U19	74ACT244
U17	74ACT245
U18	74HCT688
U20, U21	74HCT138

Resistors

RP1-RP10	10K ohm, 7 resistor SIP
RP11, RP12	100K ohm, 7 resistor SIP

Miscellaneous

I/O 0 - I/O 7	16 pin DIP socket, pin socket contacts

STD BUS PINOUT

Connections from the VL-7601/4A board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7601/4A.

COMPONENT SIDE				SOLDER SIDE			
PIN	**SIGNAL**	**FLOW**	**DESCRIPTION**	**PIN**	**SIGNAL**	**FLOW**	**DESCRIPTION**
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	-	-5V or bat. backup	6	-5V	-	-5V power
7	D3/A19	I/O	Data bus	8	D7	I/O	Data bus
9	D2/A18	I/O	Data bus	10	D6	I/O	Data bus
11	D1/A17	I/O	Data bus	12	D5/A21	I/O	Data bus
13	D0/A16	I/O	Data bus	14	D4/A20	I/O	Data bus
15	A7	In	Address bus	16	A15	-	Address bus
17	A6	In	Address bus	18	A14	-	Address bus
19	A5	In	Address bus	20	A13	-	Address bus
21	A4	In	Address bus	22	A12	-	Address bus
23	A3	In	Address bus	24	A11	-	Address bus
25	A2	In	Address bus	26	A10	-	Address bus
27	A1	In	Address bus	28	A9	-	Address bus
29	A0	In	Address bus	30	A8	-	Address bus
31	WR*	In	Write strobe	32	RD*	In	Read strobe
33	IORQ*	In	I/O addr. select	34	MEMRQ*	-	Memory addr. select
35	IOEXP*	In	I/O expansion	36	MEMEX*	-	Memory expansion
37	REFRESH*	-	Refresh timing	38	MCSYNC*	-	Machine cycle sync.
39	STATUS1*	-	CPU status	40	STATUS0*	-	CPU status
41	BUSAK*	-	Bus acknowledge	42	BUSRQ*	-	Bus request
43	INTAK*	-	Interrupt acknowl.	44	INTRQ*	-	Interrupt request
45	WAITRQ*	-	Wait request	46	NMIRQ*	-	Non-maskable interrupt
47	SYSRESET*	In	System reset	48	PBRESET*	-	Push button reset
49	CLOCK*	-	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	-	±12 volt ground	54	AUXGND	-	±12 volt ground
55	AUX+V	-	+12 volt input	56	AUX-V	-	-12 volt input

Notes:
* Denotes an active low signal.

DECIMAL / HEX / ASCII CONVERSION CHART

The chart below is useful for both ASCII and decimal/hex conversion. The "^" symbol denotes control characters. "^A" represents control A, etc.

Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL	32	20		64	40	@	96	60	`
1	01	^A SOH	33	21	!	65	41	A	97	61	a
2	02	^B STX	34	22	"	66	42	B	98	62	b
3	03	^C ETX	35	23	#	67	43	C	99	63	c
4	04	^D EOT	36	24	$	68	44	D	100	64	d
5	05	^E ENQ	37	25	%	69	45	E	101	65	e
6	06	^F ACK	38	26	&	70	46	F	102	66	f
7	07	^G BEL	39	27	'	71	47	G	103	67	g
8	08	^H BS	40	28	(	72	48	H	104	68	h
9	09	^I HT	41	29	)	73	49	I	105	69	i
10	0A	^J LF	42	2A	*	74	4A	J	106	6A	j
11	0B	^K VT	43	2B	+	75	4B	K	107	6B	k
12	0C	^L FF	44	2C	,	76	4C	L	108	6C	l
13	0D	^M CR	45	2D	-	77	4D	M	109	6D	m
14	0E	^N SO	46	2E	.	78	4E	N	110	6E	n
15	0F	^O SI	47	2F	/	79	4F	O	111	6F	o
16	10	^P DLE	48	30	0	80	50	P	112	70	p
17	11	^Q DC1	49	31	1	81	51	Q	113	71	q
18	12	^R DC2	50	32	2	82	52	R	114	72	r
19	13	^S DC3	51	33	3	83	53	S	115	73	s
20	14	^T DC4	52	34	4	84	54	T	116	74	t
21	15	^U NAK	53	35	5	85	55	U	117	75	u
22	16	^V SYN	54	36	6	86	56	V	118	76	v
23	17	^W ETB	55	37	7	87	57	W	119	77	w
24	18	^X CAN	56	38	8	88	58	X	120	78	x
25	19	^Y EM	57	39	9	89	59	Y	121	79	y
26	1A	^Z SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL