Reference Manual

VL-7508
VL-75CT08

48-Line Opto 22 Interface
Card for the STD Bus

VERSALOGIC
CORPORATION

VL-7508
VL-75CT08

48-Line Opto 22 Interface Card
for the STD Bus

Model VL-7508

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REFERENCE MANUAL

VL-7508	Rev. 0.00
VL-75CT08	Rev. 0.00
Doc. Rev.	8/27/93

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M7508

Model VL-7508
General Purpose 48-Line Interface Card

REFERENCE MANUAL

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Section 1
OVERVIEW

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7508 interface card. This card is designed to interface directly with modular solid state relay rack systems available from Opto 22, Gordos, Motorola, and others. With high power output drivers and filtered input lines, this board is also ideal for many general purpose TTL interfacing applications.

The card is available in standard (VL-7508) and extended temperature (VL-75CT08) versions. Throughout this manual "VL-7508" will be used to refer to both versions of these boards, unless specifically noted otherwise.

OVERVIEW

The VL-7508 provides 48 I/O lines that are compatible with I/O rack type control modules, or general TTL interfacing. It is configured as two 24-channel groups which are connected through two 50-pin I/O connectors. The VL-7508 occupies eight consecutive I/O addresses and uses two latching 50-pin headers for its I/O connections.

The board is plug compatible with industry standard 4, 8, 16, and 24-position modular I/O racks. It is also ideal for general purpose I/O interfacing with TTL type signals.

Each input channel is individually filtered to minimize noise induced errors at the input buffer. Reading a channel that is currently programmed as an output, reads the current state of the output line (output readback).

Each open collector output line provides 20 ma of drive (sink) to interface directly with solid state AC or DC control modules, or other TTL devices. The outputs are latched, fully buffered, and are automatically cleared during system reset.

Each VL-7508 I/O line is individually programmable as an input or an output. This allows mixing of input and output type modules in any combination desired. All of the channels will interface directly with standard AC or DC input or output modules.

Two on-board rack power controls can be used to turn two modular I/O racks on or off under software control. Each rack power output provides up to 500 ma at 4.70 VDC (typical). The state of the rack power lines is indicated by on-board LEDs.

The VL-7508 features 8 and 10-bit addressing, and is compatible with all common STD Bus processor types. The IOEXP line is also supported.

The board is fully compatible with the Pro-Log 7508 card.

FEATURES

- 48 fully buffered bidirectional I/O lines.
- Plug compatible with standard I/O racks.
- Controls up to 48 AC or DC I/O modules.
- 8 and 10-bit address decoding.
- Noise filtered input lines.
- Software controlled I/O rack power sources.
- Dual latching header connectors.
- Extended temperature version available.
- Universal STD Bus processor compatible.
- Plug-in replacement for Pro-Log 7508.

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications

Storage Temperature:
- VL-7508: -40° to +75° C
- VL-75CT08: -40° to +85° C

Free Air Operating Temperature:
- VL-7508: 0° to +65° C
- VL-75CT08: -40° to +85° C

Power Requirements:

- VL-7508: 5V ±5% @ 375 ma typ. (rack off, all outputs high)
  5V ±5% @ 660 ma typ. (rack off, all outputs low)

- VL-75CT08: 5V ±10% @ 36 ma typ. (rack off, all outputs high)
  5V ±10% @ 89 ma typ. (rack off, 24 outputs low)
  5V ±10% @ 139 ma typ. (rack off, 48 outputs low)

I/O Port Interface:

- VL-7508: Output Drive: 20 ma min. @ .7V max.
  Input Load: 4.8 ma @ .4V (1K ohm pullup)
  Rack Power Output: 500 ma min. @ 4.7V typ.

- VL-75CT08: Output Drive: 20 ma min. @ .7V max.
  Input Load: .5 ma @ .4V (10K ohm pullup)
  Rack Power Output: 500 ma min. @ 4.7V typ.

Section 2
CONFIGURATION

JUMPER SUMMARY

Various options available on the VL-7508 card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 2-1 shows the jumper block locations on the VL-7508 board. It indicates the position of the jumper plugs as shipped from the factory. The function of each jumper block is detailed in Figure 2-2.

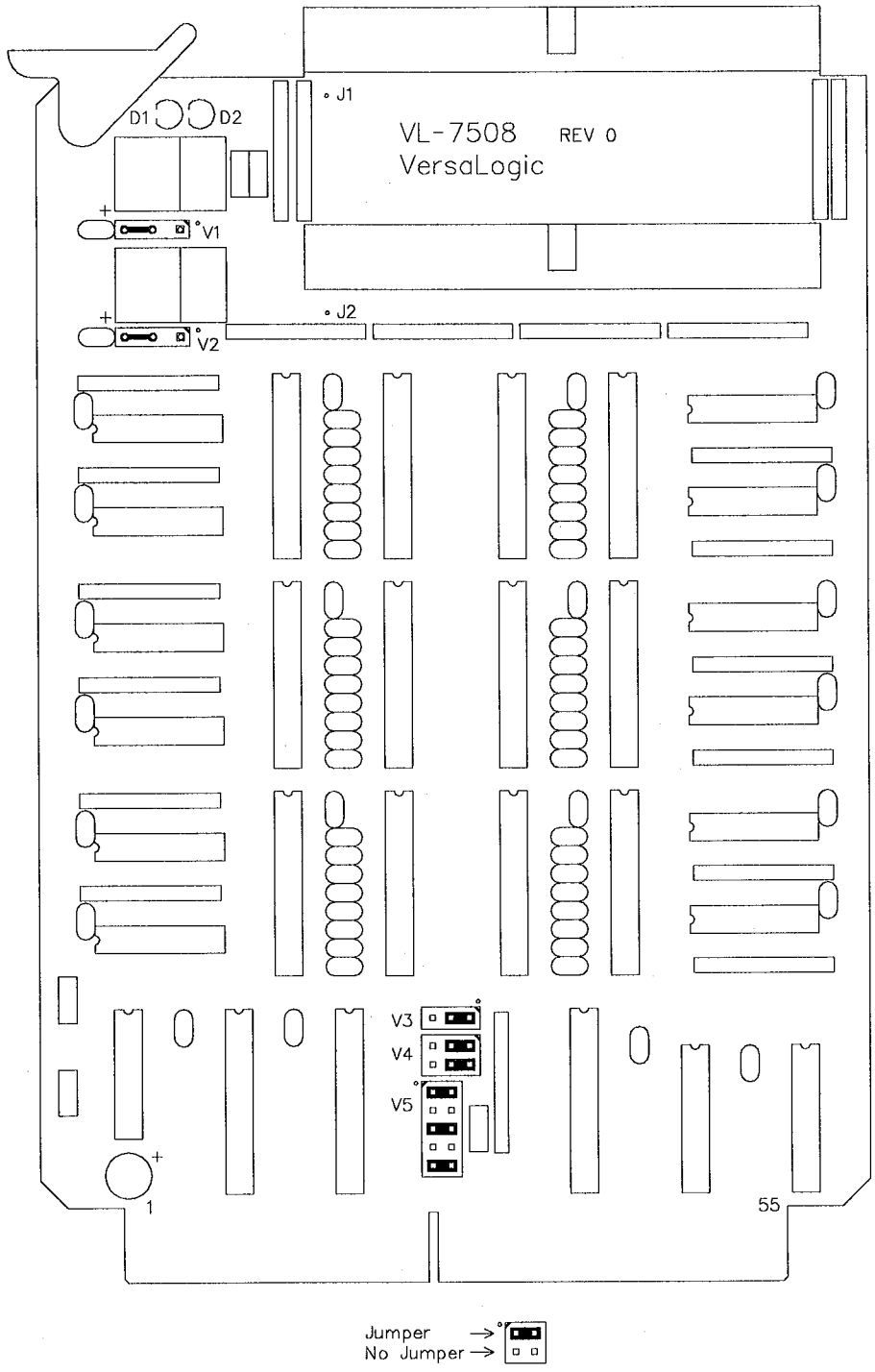


Figure 2-1. Jumper Block Locations

Jumper Block	Description	As Shipped
V1	Rack power source, connector J1.	
	a - Always on.	a - out
	b - Software controlled.	b - IN
V2	Rack power source, connector J2.	
	a - Always on.	a - out
	b - Software controlled.	b - IN
V3	IOEXP select. See Board Address.	
	a - Don't care.	a - IN
	b - Active low.	b - out
	- - Active high (both jumpers out).	
V4	Address mode selector. See Board Address.	
	a - A9 control.	a - ignore A9
	b - A8 control.	b - ignore A8
V5	Board Address. See Board Address.	Hex 50

Figure 2-2. Jumper Functions

BOARD ADDRESS

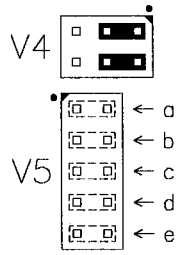
The VL-7508 supports both 8 and 10-bit I/O addressing. 8-bit addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10-bit addressing can be used with 16-bit processors (i.e. 8088) to decode up to 1024 I/O port addresses.

Both 8 and 10-bit addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7508.

As shipped the board is configured for 8-bit addressing with a board address of hex 50. The VL-7508 occupies eight consecutive I/O addresses (i.e. 50-57).

8-Bit Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired address (i.e. "3" & "0" = hex address 30).



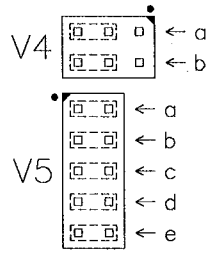
----- V5 ----				Upper	V5	Lower
a	b	c	d	Digit	e	Digit
X	X	X	X	0	X	0
X	X	X	-	1	-	8
X	X	-	X	2		
X	X	-	-	3		
X	-	X	X	4		
X	-	X	-	5		
X	-	-	X	6		
X	-	-	-	7		
-	X	X	X	8		
-	X	X	-	9		
-	X	-	X	A		
-	X	-	-	B		
-	-	X	X	C		
-	-	X	-	D		
-	-	-	X	E		
-	-	-	-	F		

X = Jumper installed.
- = Jumper removed.

Figure 2-3. 8-Bit Address Jumpers

10-Bit Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e. "1" & "3" & "0" = hex address 130).



V4 a	V4 b	Upper Digit
X	X	0
X	-	1
-	X	2
-	-	3

V5 a	V5 b	V5 c	V5 d	Middle Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

V5 e	Lower Digit
X	0
-	8

X = Jumper installed.
- = Jumper removed.

Figure 2-4. 10-Bit Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown in Figure 2-5.

Jumper Block	Description	As Shipped
V3	a - Ignore IOEXP (enable high or low).	a - IN
	b - Enable on IOEXP low.	b - out
	None - Enable on IOEXP high (no jumpers).	

Figure 2-5. IOEXP Options

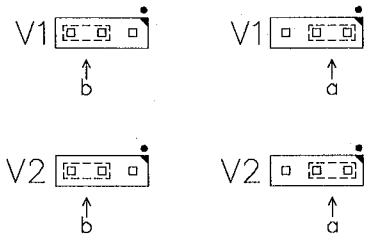
RACK POWER CONTROL

The VL-7508 board includes provisions for powering the external I/O rack assemblies with +5 volts. In addition, these power output lines can be controlled by the system software to turn an entire rack on or off as desired.

Jumpers V1 and V2 allow the rack power control circuitry to be bypassed. In jumper position "a" the I/O rack power line (pin 49) is connected directly to +5 volts on the STD Bus and the rack can not be turned off through software commands. This jumper option is detailed below.

If the I/O rack is powered by a separate external supply then a jumper must be removed from the I/O rack (see THE I/O RACK below), or both the "a" and "b" jumpers should be removed from the rack power jumper block on the VL-7508 board.

The current state of the I/O rack power outputs is indicated by the D1 and D2 LEDs (for connectors J1 and J2 respectively) at the edge of the board.



Jumper Block	Description	As Shipped
V1	Rack power source, connector J1.	
	a - Always on.	a - out
	b - Software controlled.	b - IN
	- - Externally powered (no jumpers).	
V2	Rack power source, connector J2.	
	a - Always on.	a - out
	b - Software controlled.	b - IN
	- - Externally powered (no jumpers).	

Figure 2-6. Rack Power Source Jumpers

THE I/O RACK

Modular I/O racks are configured by placing the desired type of interface module in each position in the rack. Although the modules can be mixed in any way desired, it generally simplifies the system software to have all the inputs and all the outputs grouped together (rather than intermingled).

The +5 volt power required by the I/O rack can be taken from an external supply or from the STD Bus (via each data interface cable). If an external supply is used then the jumper on the I/O rack must be cut so that no power connection is made to the VL-7508 rack power line. If power is to be taken from the STD Bus, then the power jumper on the I/O rack should be left in.

Note that +5 volt power outputs from the VL-7508 card can be shorted to ground if the connectors are not correctly oriented at either end of the interface cable. The use of keys in the connectors, or very clear markings on the connectors, is recommended to prevent backwards connection of the cable.

The VL-7508 connects directly to 4, 8, 16, and 24-position racks using VersaLogic cable assembly #9564.

Section 3
INSTALLATION

HANDLING

** CAUTION ** The VL-7508 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

INSTALLATION

The VL-7508 card can be installed in any slot of an STD Bus card cage.

The VL-7508 does not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on this board are connected together so that the priority chain will not be broken. This board may be inserted between other boards that are using the priority chain.

** CAUTION ** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

** CAUTION ** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

EXTERNAL CONNECTIONS

Connection to the VL-7508 can be made as noted below. Pinout listings for these connectors appear on the following pages.

Connectors J1 and J2

Connectors J1 and J2 are 50-pin header type connectors (on .1" centers). They may each be connected to an Opto 22 type I/O rack using a Versa-Logic cable assembly #9564. Mating connectors include Ansley #609-5041 and AMP #1-499933-0.

		------- VL-7508 -------		------ VL-75CT08 -------	
J1 & J2 Pin	Signal Name	Input Load (Sink ma)	Output Drive (Sink ma)	Input Load (Sink ma)	Output Drive (Sink ma)
1	MOD 23*	4.8	20	0.5	20
3	MOD 22*	4.8	20	0.5	20
5	MOD 21*	4.8	20	0.5	20
7	MOD 20*	4.8	20	0.5	20
9	MOD 19*	4.8	20	0.5	20
11	MOD 18*	4.8	20	0.5	20
13	MOD 17*	4.8	20	0.5	20
15	MOD 16*	4.8	20	0.5	20
17	MOD 15*	4.8	20	0.5	20
19	MOD 14*	4.8	20	0.5	20
21	MOD 13*	4.8	20	0.5	20
23	MOD 12*	4.8	20	0.5	20
25	MOD 11*	4.8	20	0.5	20
27	MOD 10*	4.8	20	0.5	20
29	MOD 9*	4.8	20	0.5	20
31	MOD 8*	4.8	20	0.5	20
33	MOD 7*	4.8	20	0.5	20
35	MOD 6*	4.8	20	0.5	20
37	MOD 5*	4.8	20	0.5	20
39	MOD 4*	4.8	20	0.5	20
41	MOD 3*	4.8	20	0.5	20
43	MOD 2*	4.8	20	0.5	20
45	MOD 1*	4.8	20	0.5	20
47	MOD 0*	4.8	20	0.5	20
49	RACK POWER	-	500	-	500
2-50	All even numbered pins are ground.				

Notes:
"*" Notes an inverted signal (true = low).
See Special Applications for notes about output drive.

Figure 3-1. Connector J1 and J2 Pinout

Section 4
OPERATION

INTRODUCTION

This section includes general information about the use and operation of the VL-7508 card. It focuses primarily on the software commands necessary to operate the card and includes various examples to assist you in constructing your own software routines.

I/O PORT MAPPING

The VL-7508 occupies eight I/O port addresses. Four addresses are used for each of the independent 24-line interfaces (called interface "A" and "B"). Interface "A" and "B" each use three addresses to access their 24 I/O channels (lines), while a fourth address is used to control their I/O rack power line. The "A" and "B" interfaces are each identical to one VL-7507 card (except for the exclusion of an interrupt function).

Alternately, the VL-7508 board can be viewed as one group of 48 channels (instead of two groups of 24). This simplifies software implementation when many modules are used in a system. Using this numbering system the modules in the second I/O rack (connector J2) are numbered 24-47 (rather than 0-23). The software routines included later in this section support this numbering of the I/O rack channels.

The locations of the eight ports are determined by the board address, which is jumper selectable. As shipped, the board is jumpered for hex address 50.

Once the board's I/O address has been determined, the addresses of the eight I/O ports can be determined as shown in Figure 4-1. Each I/O module port can be both read (for inputting data) and written (for outputting data).

Figure 4-2 shows how each I/O module channel corresponds to the data bits in the I/O port addresses. This example uses the default board address of hex 50.

Note that only bits M0-M7 are used with 8-position racks. Bits M0-M15 are used with 16-position racks.

Port Address	Function/ Module #	Alternate Numbering
Interface A (connector J1)		
Board Address + 3	Rack Power	Rack Power
Board Address + 2	0-7	0-7
Board Address + 1	8-15	8-15
Board Address + 0	16-23	16-23
Interface B (connector J2)		
Board Address + 7	Rack Power	Rack Power
Board Address + 6	0-7	24-31
Board Address + 5	8-15	32-39
Board Address + 4	16-23	40-47

Figure 4-1. I/O Port Locations

ADDR.	D7	D6	D5	D4	D3	D2	D1	D0
Interface B (connector J2)								
57	RACK POWER	-	-	-	-	-	-	-
56	M0	M1	M2	M3	M4	M5	M6	M7
55	M8	M9	M10	M11	M12	M13	M14	M15
54	M16	M17	M18	M19	M20	M21	M22	M23
Interface A (connector J1)								
53	RACK POWER	-	-	-	-	-	-	-
52	M0	M1	M2	M3	M4	M5	M6	M7
51	M8	M9	M10	M11	M12	M13	M14	M15
50	M16	M17	M18	M19	M20	M21	M22	M23

Mx = I/O Module channel x.
- = Don't care (ignored).

Figure 4-2. Module Channel Mapping (Dual 24-Channel Numbering)

ADDR.	D7	D6	D5	D4	D3	D2	D1	D0
Interface B (connector J2)								
57	RACK POWER	-	-	-	-	-	-	-
56	M24	M25	M26	M27	M28	M29	M30	M31
55	M32	M33	M34	M35	M36	M37	M38	M39
54	M40	M41	M42	M43	M44	M45	M46	M47
53	RACK POWER	-	-	-	-	-	-	-
Interface A (connector J1)								
52	M0	M1	M2	M3	M4	M5	M6	M7
51	M8	M9	M10	M11	M12	M13	M14	M15
50	M16	M17	M18	M19	M20	M21	M22	M23

Mx = I/O Module channel x.
- = Don't care (ignored).

Figure 4-2. Module Channel Mapping (48-Channel Numbering)

DIRECTION CONTROL

Any of the VL-7508's 48 channels may be used as an input or an output channel. The function of each channel is determined by its programming. When the system is powered-up, or a system reset occurs, all of the channels are reset to inputs. Channels connected as outputs will appear high due to the pull-up resistor on each channel.

Channels can be used as outputs by simply by writing a zero or one to it. Writing a one causes the inverting open collector buffer to go into an active low state. Writing a zero returns the buffer to an inactive (open collector) state, and the channel can be used as an input or an output.

Channels that are used as inputs may be read at any time, but they must never have a one written to them. When writing to ports which include both input and output channels, be certain to set the input channel bits to zero. A channel will act as an input as long as it is read, or zeros are written to it.

When a channel being used as an output is read, the data will reflect the current state of the output (if a one is written, a one will be read, etc.).

READING AND WRITING DATA

All of the I/O buffers on the VL-7508 board are inverting (to set an output pin low, write a one, etc.). However, I/O rack modules also use active low (inverted) signals. The resulting data interface levels between the VL-7508 and I/O rack modules are are shown in Figure 4-3.

When a one has been written to an output channel (setting the pin low), the data read from that channel will be one.

Note that the data read always reflects the actual state of the I/O pin. If an I/O pin is shorted to ground it will always read as a one. Trying to output a high or low state to the pin will have no effect on the data read.

Data Written	I/O Pin	Output Modules	Input Modules	I/O Pin	Data Read
0	(1)	Power off	Voltage absent	(1)	0
1	(0)	Power on	Voltage present	(0)	1

Figure 4-3. I/O Module Data Interface

SOFTWARE EXAMPLES

Reading a VL-7508 channel (data bit) is fairly straightforward although care must be taken to select the proper port and data bit which corresponds to the desired I/O module. Writing to a channel can also be achieved in a single operation, but provisions must be made so as to not disturb the current state of the other seven channels (bits) which appear at the same I/O port.

In systems where more than a few I/O rack modules are used, both of these operations can be made much easier with generalized subroutines that read or write to a specified channel number. These subroutines calculate the port address and data bit involved and allow the programmer to concentrate on reading or writing to the required I/O module. Subroutines of this type are shown in the examples that follow.

As mentioned earlier, the VL-7508 can be viewed as two independent 24-channel interfaces, or one 48-channel interface. The routines included here are designed to use the board as one interface of 48 channels.

The VL-7508 can be used with any language that allows direct access to system I/O ports. The examples below are shown in several programming languages. These examples have not necessarily been tested or verified for proper operation. They are supplied for general information only and may not be appropriate for any specific application.

Assembly Language Examples

The following Z80 program fragments illustrate how the VL-7508 board can be used in an assembly language environment.

The first example illustrates direct access to each desired I/O channel. This method is sometimes appropriate when there is only a small number of modules connected to the interface. It requires the programmer to determine the related port and bit of the desired channel.

The second example illustrates access by channel number. It uses subroutines to read or write to a specified channel, freeing the programmer from unnecessary calculations during program construction.

```
                    ;Example 1.  Direct access to the VL-7508.
                    ;Copyright 1986, VersaLogic, Eugene, OR
                    ;
                    ;Define all port locations.
          0050      RIOBASE   EQU   50H     ;Board address = hex 50.
          0050      RACK0     EQU   RIOBASE + 0     ;Port 0 (channels 16-23).
          0051      RACK1     EQU   RIOBASE + 1     ;Port 1 (channels 8-15).
          0052      RACK2     EQU   RIOBASE + 2     ;Port 2 (channels 0-7).
          0053      RACKPWR   EQU   RIOBASE + 3     ;Power control port.
                    ;
                    ;Define channel usage (high bits are output channels).
          0003      RACKU0    EQU   00000011B       ;Port 0 (channels 16-23).
          0000      RACKU1    EQU   00000000B       ;Port 1 (channels 8-15).
          00FC      RACKU2    EQU   11111100B       ;Port 2 (channels 0-7).
                    ;
0100                ORG       100H      ;Start of code.
                    ;
                    ;
                    ;Reading a relay channel (state of input or output channel).
0100  DB 50             IN  A,(RACK0)   ;Read the I/O port.
0102  E6 02             AND 00000010B   ;Mask out all channels except #22.
0104  20 02             JR  NZ,ON22     ;Jump to somewhere if channel is ON.
                    ;
                    ;User routine for channel on.
0106  00            ON22    NOP
                    ;
                    ;
                    ;Setting a channel ON (output pin low).
0107  DB 51             IN  A,(RACK1)   ;Read the current state of the outputs.
0109  F6 40             OR  01000000B   ;Set the channel #9 bit ON.
010B  E6 FC             AND RACKU2      ;Clear input channel bits.
010D  D3 52             OUT (RACK2),A   ;Write it to the board.
                    ;
                    ;
                    ;Setting a channel OFF (output pin high).
010F  DB 52             IN  A,(RACK2)   ;Read the current state of the outputs.
0111  E6 FB             AND 11111011B   ;Set the channel #5 bit OFF.
0113  E6 FC             AND RACKU2      ;Clear input channel bits.
0115  D3 52             OUT (RACK2),A   ;Write it to the port.
```

```
                    ;Example 2 - Accessing the VL-7508 by channel #.
                    ;Copyright 1986, VersaLogic, Eugene, OR
                    ;
                    ;Channels 0-23 = interface A (connector J1)
                    ;Channels 24-47 = interface B (connector J2)
                    ;
      0050          RACKADRA EQU 50H            ;Board address = hex 50.
      0054          RACKADRB EQU RACKADRA+4     ;Interface B base addr.
                    ;
                    ;I/O usage table.  High bits are output channels.
      00F0          RAKU0    EQU  11110000B     ;Port 0 (channels A 16-23).
      00FC          RAKU1    EQU  11111100B     ;Port 1 (channels A 8-15).
      00FF          RAKU2    EQU  11111111B     ;Port 2 (channels A 0-7).
                    ;
      00FF          RAKU4    EQU  11111111B     ;Port 4 (channels B 16-23).
      0000          RAKU5    EQU  00000000B     ;Port 5 (channels B 8-15).
      0000          RAKU6    EQU  00000000B     ;Port 6 (channels B 0-7).
                    ;
0100                         ORG  100H          ;Start of code.
                    ;
                    ;reading a relay channel (state of input or output).
0100  3E 0C                  LD   A,12          ;Specify channel 12
0102  CD 14 01               CALL READ          ;Read it (result in A)
0105  C2 09 01               JP   NZ,DUMMY      ;Jump somewhere if it is ON.
0108  00                     NOP                ;(do something else if it isn't)
0109  00                DUMMY  NOP              ;(user routine)
                    ;
                    ;
                    ;Setting a channel ON (output pin low).
010A  3E 09                  LD   A,9           ;Specify channel 9
010C  CD 1E 01               CALL ON            ;Turn it ON
                    ;
                    ;
                    ;Setting a channel OFF (output pin high).
010F  3E 28                  LD   A,40           ;Specify channel 40
0111  CD 28 01               CALL OFF            ;Turn it OFF
                    ;
                    ;
                    ;** SUBROUTINES **
                    ;Reads a channel (input or output). Chan.# (0-47) is in A.
                    ;Returns the state of the channel (0 or 1) in reg. A.
0114  CD 36 01      READ     CALL FIND          ;Convert the channel #.
0117  ED 78                  IN   A,(C)         ;Read the port.
0119  A0                    AND  A,B           ;Mask for desired bit.
011A  C8                     RET  Z             ;Return if 0.
011B  3E 01                  LD   A,1           ;Or else plug with a 1
011D  C9                     RET                ;and return.
                    ;
```

```
                        ;Sets an output channel ON. Chan.# (0-47) is in reg. A.
                        ;Note:  Won't work unless channel is defined as an
                        ;output in the usage registers.
011E   CD 36 01    ON       CALL FIND          ;Convert the channel #.
0121   ED 78                IN   A,(C)         ;Read current output states.
0123   B0                   OR   B             ;Set channel on.
0124   A2                   AND  D             ;Clear input channel bits.
0125   ED 79                OUT  (C),A         ;Write it to the port.
0127   C9                   RET                ;Return.
                        ;
                        ;Sets an output channel off. Chan.# (0-47) is in reg. A.
0128   CD 36 01    OFF      CALL FIND          ;Convert the channel #.
012B   78                   LD   A,B           ;Complement B (bit mask).
012C   EE FF                XOR  A,0FFH
012E   47                   LD   B,A
012F   ED 78                IN   A,(C)         ;Read current output states.
0131   A0                   AND  B             ;Set channel off.
0132   A2                   AND  D             ;Clear input bits.
0133   ED 79                OUT  (C),A         ;Write it to the port.
0135   C9                   RET                ;Return
                        ;
                        ;Computes the port address and bit mask for the requested
                        ;channel # (in register A).
                        ;Returns A=0, B=bit mask, C=port address, D=usage mask
0136   3C           FIND    INC  A             ;Offset channel # by 1.
0137   06 80                LD   B,80H         ;Initialize B, for channel #0.
0139   0E 50                LD   C,RACKADRA    ;Initialize C, for channel #0.
013B   21 57 01              LD   HL,UA2        ;Usage table address to HL.
013E   FE 19                 CP   25            ;Is chan. # < 25?
0140   38 05                 JR   C,J1          ;Yes, jump
0142   0E 54                 LD   C,RACKADRB    ;No, init. for group B
0144   21 5A 01              LD   HL,UB2        ;Usage table address to HL.
0147   56           J1      LD   D,(HL)        ;Initialize D, for channel #0.
0148   3D           L1      DEC  A             ;Decrement channel #.
0149   C8                   RET  Z             ;Done when A=0.
014A   CB 18                RR   B             ;Rotate bit mask.
014C   30 FA                JR   NC,L1         ;Loop if no carry.
014E   0D                   DEC  C             ;Adjust port address.
014F   2B                   DEC  HL            ;Adjust usage table pointer.
0150   56                   LD   D,(HL)        ;D=usage mask.
0151   CB 18                RR   B             ;Carry -> D7.
0153   18 F3                JR   L1            ;Continue.
                        ;
                        ;Usage table.  Note: This table MUST be six bytes long.
0155   F0           UA0     DB   RAKU0
0156   FC           UA1     DB   RAKU1
0157   FF           UA2     DB   RAKU2
0158   FF           UB0     DB   RAKU4
0159   00           UB1     DB   RAKU5
015A   00           UB2     DB   RAKU6
```

BASIC Language Examples

The subroutines and program fragments in the first listing below illustrate how the VL-7508 board can be used with standard BASICs (or other high level languages) that include logical AND, OR, and XOR functions. Microsoft's BASIC-80 is used in this example.

Users of VersaLogic's C4 BASIC language should refer to the second listing which shows these same functions written in C4 BASIC. Note that the C4 BASIC RIN and ROUT statements are compatible only with the VersaLogic MIO-24 board. They should not be used with the VL-7508.

Notice: These routines may not operate correctly with some BASICs or be suitable for your application.

```
10 REM Microsoft BASIC-80 language example for the VL-7508 board.
20 REM Note that channels 0-23 are on interface A, 24-47 on interface B
30 REM
50 REM Set address of Rack Interface (RI) board (50 hex = 80 decimal)
51 RI = 80
70 REM Set usage flags for each port (8 channels each)
71 REM Output channels are a "O", inputs are a "I"
72 U$(3)="IIIIIIII" : REM Channels 0-7 (A)
73 U$(2)="OOOOOOOO" : REM Channels 8-15 (A)
74 U$(1)="IIIIIOOO" : REM Channels 16-23 (A)
75 U$(6)="IIOOOOOO" : REM Channels 24-31 (B 0-7)
76 U$(5)="OOOOOOOO" : REM Channels 32-39 (B 8-15)
77 U$(4)="IIIIIOOO" : REM Channels 40-47 (B 16-23)
80 REM Initialize the conversion routine.
81 GOSUB 700
 .
 .
100 REM Turn ON channel 11
101 CHAN=11: GOSUB 570
 .
 .
150 REM Read channel 0 and do something if it's ON.
151 CHAN=0: GOSUB 510
152 IF STATE = 1 THEN GOTO 1000
 .
170 REM Turn channel 8 OFF.
171 CHAN=8: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7508 BOARD.
501 REM These routines are called with the channel # (0-47) in "CHAN".
502 REM Input data is returned in "STATE" (1=ON, 0=OFF).
503 REM The startup routine (at 700) must be called before the other
504 REM routines are used.

510 REM Read the channel in "CHAN" (0-47)
520 GOSUB 600 : STATE=INP(ADDR) AND MASK : IF STATE > 0 THEN STATE=1
530 RETURN

540 REM Turn OFF channel "CHAN" (0-47)
550 GOSUB 600 : OUT ADDR,(INP(ADDR) AND U(UN) AND (255 XOR MASK))
560 RETURN

570 REM Turn ON channel "CHAN" (0-47)
580 GOSUB 600 : OUT ADDR,(INP(ADDR) AND U(UN) OR MASK)
590 RETURN

600 REM Computes port address and I/O usage byte # for I/O routines.
610 IF CHAN < 24 THEN GOTO 640
620 X=INT((23-(CHAN-24))/8) : ADDR=RI+X+4
630 MASK=2^((CHAN-24)-8*X)  : UN=X+4 : RETURN
640 X=INT((23-(CHAN))/8) : ADDR=RI+X : UN=X+1 : MASK=2^(CHAN-8*X) : RETURN
```

```
700 REM Initialization routine
701 REM Converts the usage strings into decimal byte masks
710 FOR N = 1 TO 6 : U(N)=0
720 FOR X = 0 TO 7
730 IF MID$(U$(N),8-X,1) <> "I" then U(N)=U(N) + (2^X)
740 NEXT X : NEXT N
750 RETURN
```

```
10 REM VersaLogic C4 BASIC language example for the VL-7508 board.
20
50 REM Set address of Rack Interface (R1) board (50 hex)
51 R1 = &50
70 REM Set usage flags for each port (8 channels each)
71 REM Values are in HEX.  Output channels are a 1, inputs are a 0.
72 U2=&4F : REM Port 2, channels 0-7 (A)
73 U1=&C0 : REM Port 1, channels 8-15 (A)
74 U0=&FF : REM Port 0, channels 16-23 (A)
75 U6=&F0 : REM Port 6, channels 24-31 (B 0-7)
76 U5=&00 : REM Port 5, channels 32-39 (B 8-15)
77 U4=&00 : REM Port 4, channels 40-47 (B 16-23)
 .
 .
 .
100 REM Turn ON channel 11
101 C=11: GOSUB 570
 .
 .
150 REM Read channel 0 and do something if it's ON.
151 C=0: GOSUB 510
152 IF S = 1 GOTO 1000
 .
170 REM Turn channel 31 OFF.
171 C=31: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7508 BOARD.
501 REM These routines are called with the channel # in "C" (0-47).
502 REM Input data is returned in "S" (1=ON, 0=OFF).

510 REM Read the channel in "C"
520 GOSUB 595 : S=IN(R1+X) AND X1 : If S>0 S=1
530 RETURN

540 REM Turn OFF channel "C"
550 GOSUB 595 : OUT R1+X,(IN(R1+X) AND U(X) AND (NOT (X1))
560 RETURN

570 REM Turn ON channel "C"
580 GOSUB 595 : OUT R1+X,(IN(R1+X) AND U(X) OR X1)
590 RETURN

594 REM Computes port addr offset (X) and bit mask (X1) for routines above
595 IF C < 24 GOTO 598
596 X=((23-(C-24))/8)+4: X1=1: X2=MOD((23-(C-24)),8): IF X2=0 RETURN
597 GOTO 599
598 X=((23-C)/8): X1=1: X2=MOD((23-C),8): IF X2=0 RETURN
599 FOR X3 = 1 TO X2 : X1=X1*2 : NEXT X3 : RETURN
```

I/O RACK POWER CONTROL

The VL-7508 includes two software controlled outputs for supplying +5 volt power to the I/O racks (from the STD Bus). The software control may be defeated (power always on) with jumper V1 and V2 (see the Configuration section). This control has no effect if the I/O rack is powered from an external power source.

The rack power for connector J1 is controlled with data bit 7 at the board address + 3 (port address 53 as shipped). The rack power for connector J2 is controlled with data bit 7 at the board address + 7 (port address 57 as shipped). Data bits 0-6 at these ports have no function and are ignored. Writing 00 to the port will turn on the rack; writing FF to the port will turn off the rack. The rack power lines are turned on at power-up or system reset.

The I/O rack control may be used for disabling an entire rack in emergency situations (although it will be turned back on when the system is reset). It can also be used to disable an I/O rack while data is written to, and read back from each channel to verify proper operation of the VL-7508 board.

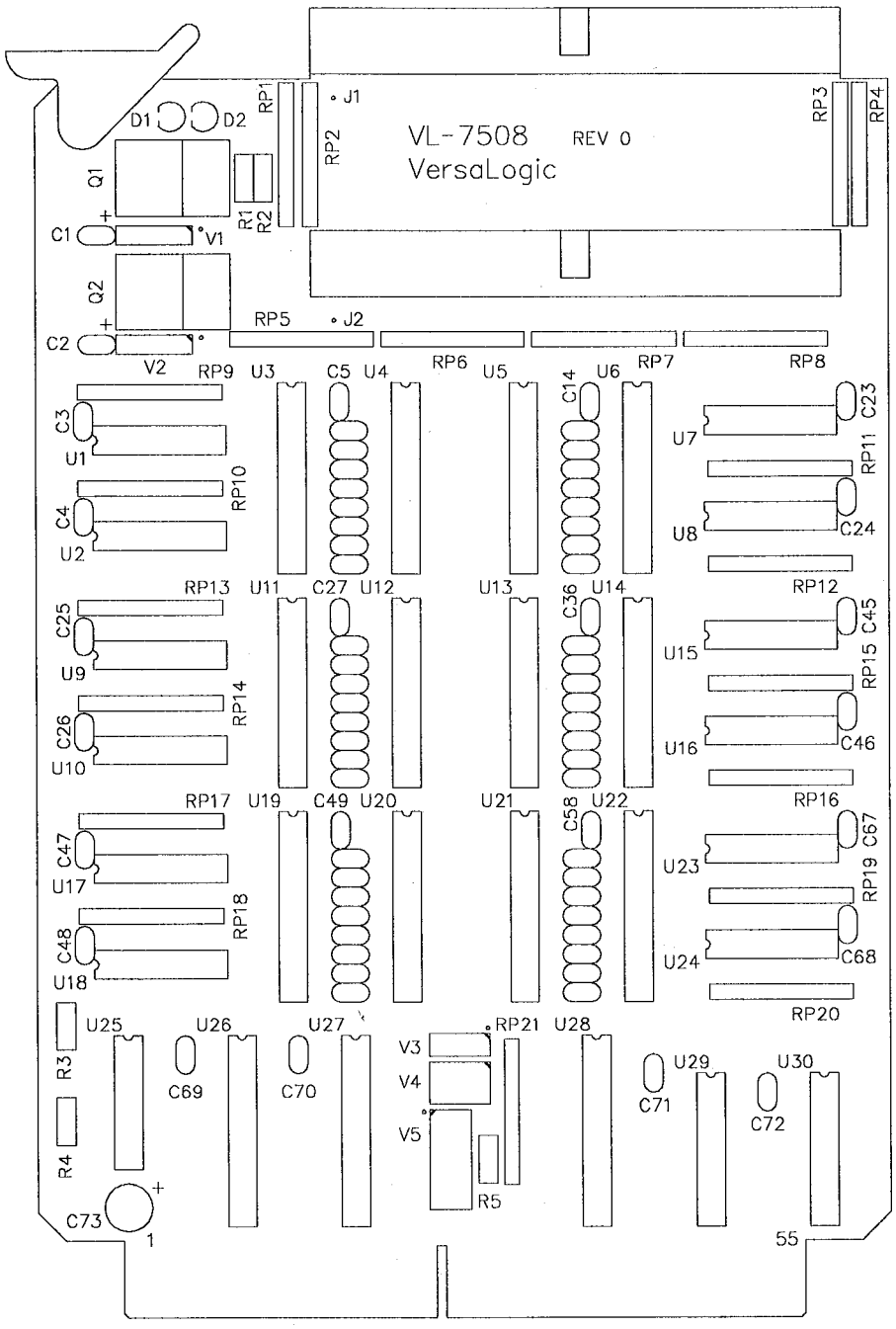
The current state of the I/O rack power lines is indicated by the LEDs D1 and D2 (for connectors J1 and J2 respectively) at the edge of the VL-7508 board.

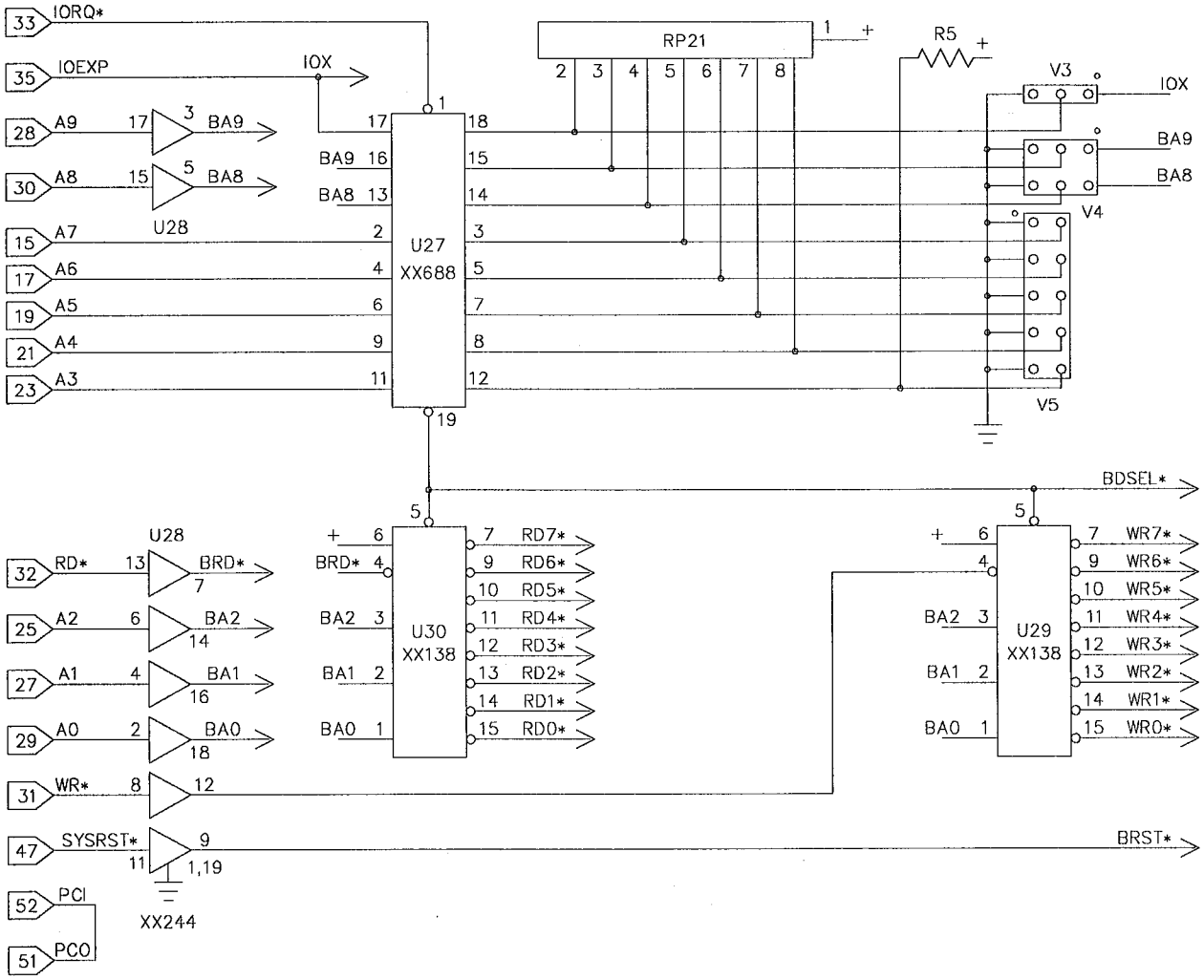
SPECIAL APPLICATIONS

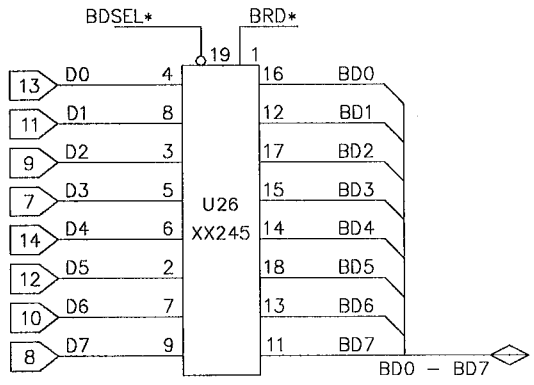
Normally the VL-7508 board is used to interface with Opto 22 type solid state I/O modules. However, it is also quite useful as a general purpose TTL I/O interface board. This section includes notes which pertain to general purpose and special applications.

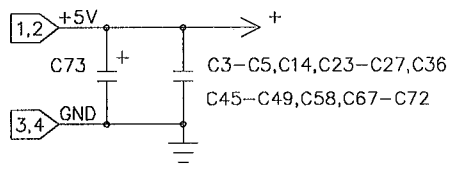
The input and output chips on the VL-7508 are socketed and may be removed or replaced for special applications. The output chips are normally open collector drivers. However, they are plug compatible with 74LS00 type chips. This allows them to be replaced with standard (non-open collector) TTL type drivers if desired. In this case the output pull-up resistors should also be removed from the board.

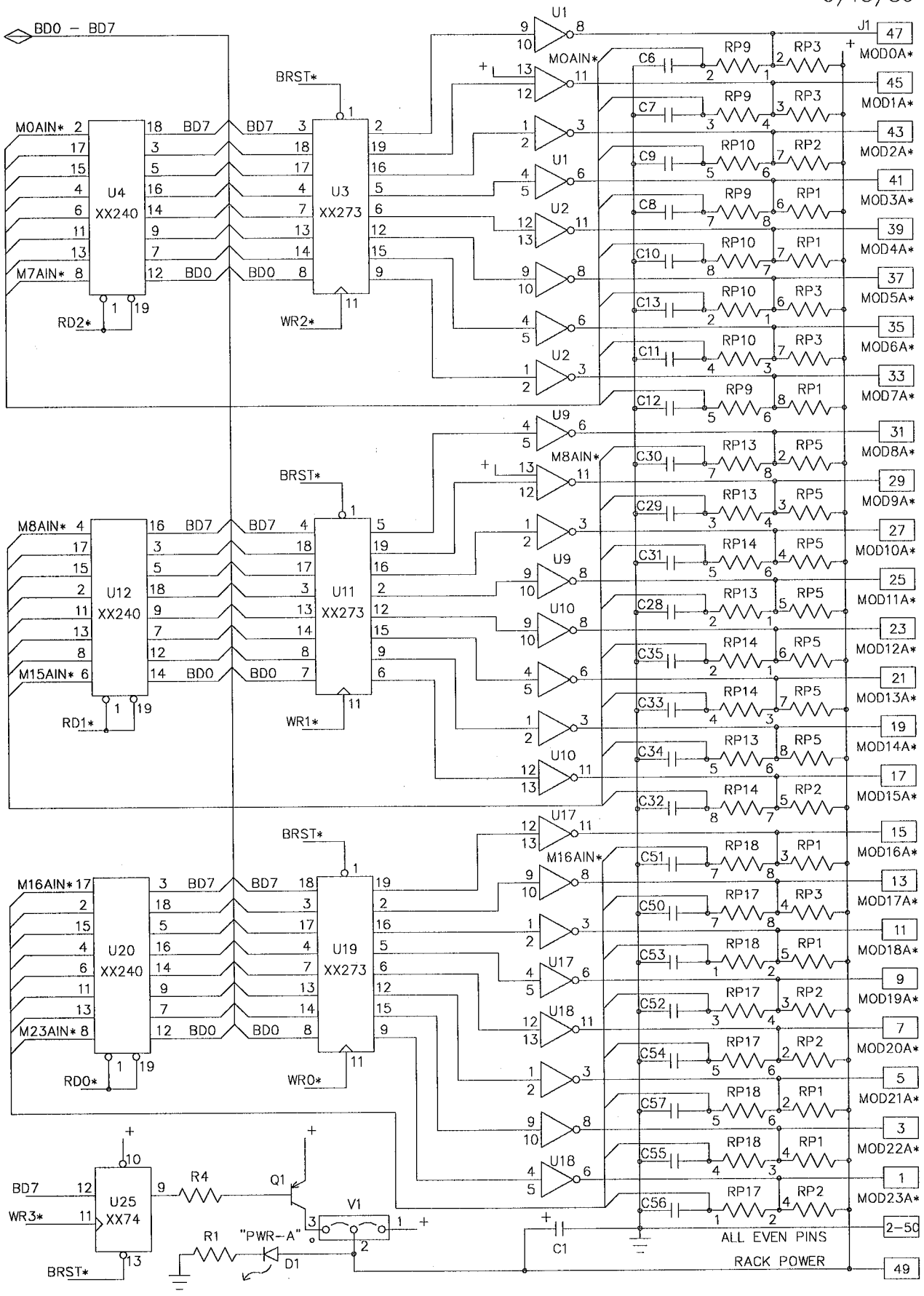
Some or all of the output driver chips may also be removed from the board completely (in 4-channel increments) to save power when some channels will be used for input only.

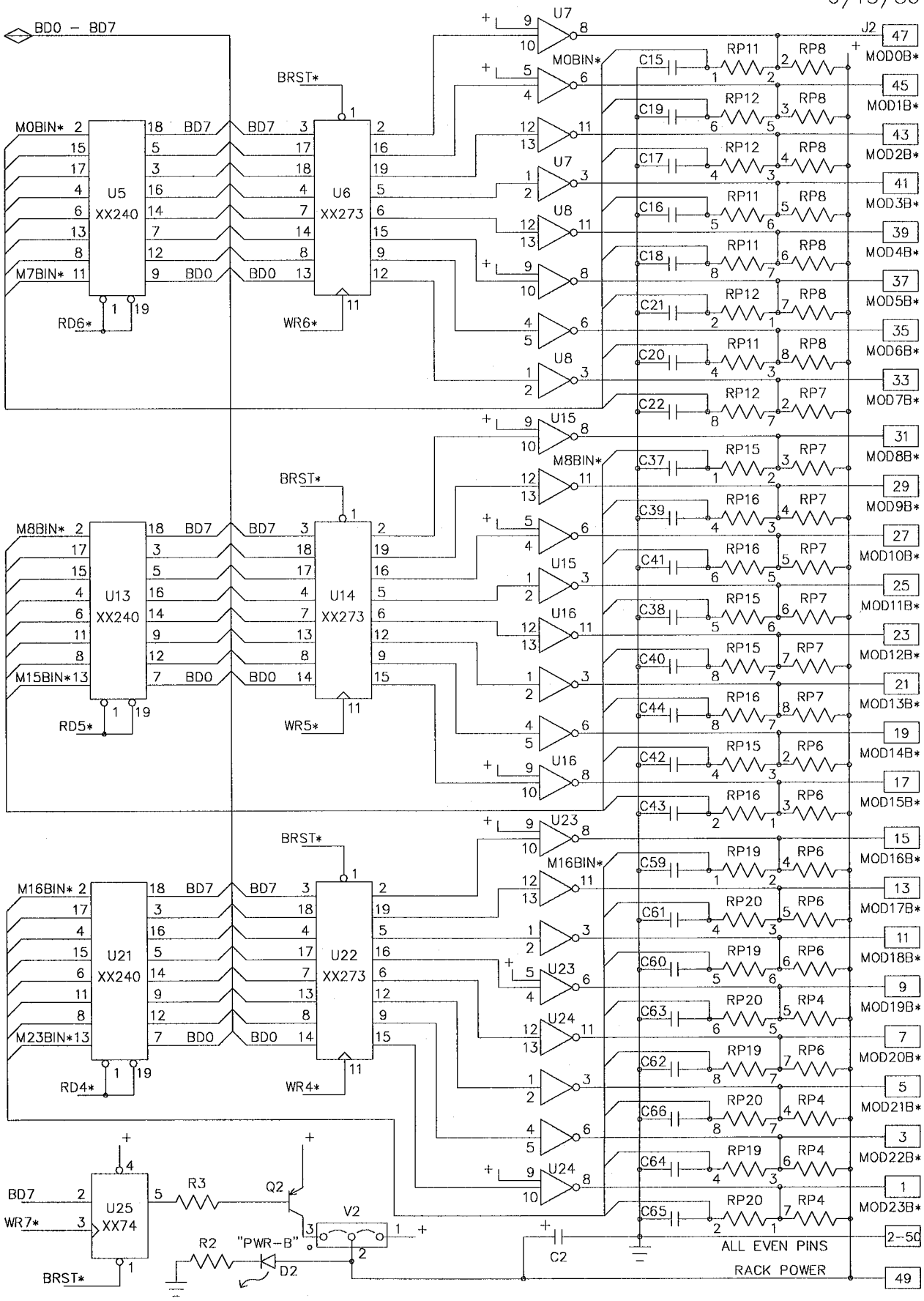

VL-7508 REV 0
VersaLogic
J1
J2
D1
D2
Q1
Q2
R1
R2
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
RP9
RP10
RP11
RP12
RP13
RP14
RP15
RP16
RP17
RP18
RP19
RP20
RP21
C1
C2
C3
C4
C5
C14
C23
C24
C25
C26
C27
C36
C45
C46
C47
C48
C49
C58
C67
C68
C69
C70
C71
C72
C73
V1
V2
V3
V4
V5
R3
R4
R5
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
1
55


33 IORQ*
35 IOEXP
IOX
28 A9
30 A8
U28
15 A7
17 A6
19 A5
21 A4
23 A3
U27
XX688
RP21
R5
V3
V4
V5
BA9
BA8
BDSEL*
U28
32 RD*
25 A2
27 A1
29 A0
31 WR*
47 SYSRST*
52 PCI
51 PCO
XX244
U30
XX138
RD7*
RD6*
RD5*
RD4*
RD3*
RD2*
RD1*
RD0*
U29
XX138
WR7*
WR6*
WR5*
WR4*
WR3*
WR2*
WR1*
WR0*
BRST*


BDSEL*
BRD*
U26
XX245
13 D0
11 D1
9 D2
7 D3
14 D4
12 D5
10 D6
8 D7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD0 – BD7


1,2 +5V
C73
3,4 GND
C3–C5,C14,C23–C27,C36
C45–C49,C58,C67–C72


BD0 – BD7
BRST*
M0AIN*
M7AIN*
U4
XX240
U3
XX273
RD2*
WR2*
M8AIN*
M15AIN*
U12
XX240
U11
XX273
RD1*
WR1*
M16AIN*
M23AIN*
U20
XX240
U19
XX273
RD0*
WR0*
U1
U2
U9
U10
U17
U18
MOAIN*
M8AIN*
M16AIN*
C6
C7
C9
C8
C10
C13
C11
C12
C30
C29
C31
C28
C35
C33
C34
C32
C51
C50
C53
C52
C54
C57
C55
C56
RP9
RP3
RP10
RP2
RP1
RP13
RP5
RP14
RP18
RP17
J1
47
MOD0A*
45
MOD1A*
43
MOD2A*
41
MOD3A*
39
MOD4A*
37
MOD5A*
35
MOD6A*
33
MOD7A*
31
MOD8A*
29
MOD9A*
27
MOD10A*
25
MOD11A*
23
MOD12A*
21
MOD13A*
19
MOD14A*
17
MOD15A*
15
MOD16A*
13
MOD17A*
11
MOD18A*
9
MOD19A*
7
MOD20A*
5
MOD21A*
3
MOD22A*
1
MOD23A*
2-50
ALL EVEN PINS
RACK POWER
49
U25
XX74
WR3*
R4
Q1
V1
R1
"PWR-A"
D1
C1


BD0 – BD7
BRST*
M0BIN*
M7BIN*
RD6*
WR6*
U5
XX240
U6
XX273
U7
U8
M8BIN*
M15BIN*
RD5*
WR5*
U13
XX240
U14
XX273
U15
U16
M16BIN*
M23BIN*
RD4*
WR4*
U21
XX240
U22
XX273
U23
U24
U25
XX74
WR7*
R3
R2
Q2
D2
"PWR-B"
V2
C2
ALL EVEN PINS
RACK POWER
J2
MOD0B*
MOD1B*
MOD2B*
MOD3B*
MOD4B*
MOD5B*
MOD6B*
MOD7B*
MOD8B*
MOD9B*
MOD10B*
MOD11B*
MOD12B*
MOD13B*
MOD14B*
MOD15B*
MOD16B*
MOD17B*
MOD18B*
MOD19B*
MOD20B*
MOD21B*
MOD22B*
MOD23B*

VL-7508 PARTS LIST
48-Line Interface Board

Capacitors

C1, C2	1 uf tantalum
C3-C72	.01 uf ceramic
C73	22 uf electrolytic, radial

Integrated Circuits

U1, U2, U7-U10, U15-U18, U23, U24	74LS38
U3, U6, U11, U14, U19, U22	74LS273
U4, U5, U12, U13, U20, U21	74LS240
U25	74LS74
U26	74LS245
U27	74HCT688
U28	74LS244
U29, U30	74LS138

Resistors

R1, R2	330 ohm, 5%, 1/4W
R3, R4	200 ohm, 5%, 1/4W
R5	10K ohm, 5%, 1/4W
RP1-RP8	1K ohm, 7 resistor SIP
RP9-RP20	1K ohm, 4 resistor SIP
RP21	10K ohm, 7 resistor SIP

Semiconductors

D1, D2	T1 LED
Q1, Q2	TIP32A transistor

Miscellaneous

J1, J2	50 pin R/A latching header

VL-75CT08 PARTS LIST
48-Line Interface Board (Extended Temperature Version)

Capacitors

C1, C2	1 uf tantalum
C3-C72	.01 uf ceramic
C73	22 uf electrolytic, radial

Integrated Circuits

U1, U2, U7-U10, U15-U18, U23, U24	54LS38
U3, U6, U11, U14, U19, U22	74HCT273
U4, U5, U12, U13, U20, U21	74ACT240
U25	74HCT74
U26	74ACT245
U27	74HCT688
U28	74ACT244
U29, U30	74HCT138

Resistors

R1, R2	470 ohm, 5%, 1/4W
R3, R4	270 ohm, 5%, 1/4W
R5	100K ohm, 5%, 1/4W
RP1-RP8	10K ohm, 7 resistor SIP
RP9-RP20	1K ohm, 4 resistor SIP
RP21	100K ohm, 7 resistor SIP

Semiconductors

D1, D2	T1 LED
Q1, Q2	TIP32A transistor

Miscellaneous

J1, J2	50 pin R/A latching header

STD BUS PINOUT

Connections from the VL-7508 board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7508.

COMPONENT SIDE				SOLDER SIDE			
PIN	**SIGNAL**	**FLOW**	**DESCRIPTION**	**PIN**	**SIGNAL**	**FLOW**	**DESCRIPTION**
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	-	-5V or bat. backup	6	-5V	-	-5V power
7	D3/A19	I/O	Data bus	8	D7	I/O	Data bus
9	D2/A18	I/O	Data bus	10	D6	I/O	Data bus
11	D1/A17	I/O	Data bus	12	D5/A21	I/O	Data bus
13	D0/A16	I/O	Data bus	14	D4/A20	I/O	Data bus
15	A7	In	Address bus	16	A15	-	Address bus
17	A6	In	Address bus	18	A14	-	Address bus
19	A5	In	Address bus	20	A13	-	Address bus
21	A4	In	Address bus	22	A12	-	Address bus
23	A3	In	Address bus	24	A11	-	Address bus
25	A2	In	Address bus	26	A10	-	Address bus
27	A1	In	Address bus	28	A9	In	Address bus
29	A0	In	Address bus	30	A8	In	Address bus
31	WR*	In	Write strobe	32	RD*	In	Read strobe
33	IORQ*	In	I/O addr. select	34	MEMRQ*	-	Memory addr. select
35	IOEXP*	In	I/O expansion	36	MEMEX*	-	Memory expansion
37	REFRESH*	-	Refresh timing	38	MCSYNC*	-	Machine cycle sync.
39	STATUS1*	-	CPU status	40	STATUS0*	-	CPU status
41	BUSAK*	-	Bus acknowledge	42	BUSRQ*	-	Bus request
43	INTAK*	-	Interrupt acknowl.	44	INTRQ*	-	Interrupt request
45	WAITRQ*	-	Wait request	46	NMIRQ*	-	Non-maskable interrupt
47	SYSRESET*	In	System reset	48	PBRESET*	-	Push button reset
49	CLOCK*	-	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	-	±12 volt ground	54	AUXGND	-	±12 volt ground
55	AUX+V	-	+12 volt input	56	AUX-V	-	-12 volt input

Notes:
* Denotes an active low signal.

DECIMAL / HEX / ASCII CONVERSION CHART

The chart below is useful for both ASCII and decimal/hex conversion. The "^" symbol denotes control characters. "^A" represents control A, etc.

Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL	32	20		64	40	@	96	60	`
1	01	^A SOH	33	21	!	65	41	A	97	61	a
2	02	^B STX	34	22	"	66	42	B	98	62	b
3	03	^C ETX	35	23	#	67	43	C	99	63	c
4	04	^D EOT	36	24	$	68	44	D	100	64	d
5	05	^E ENQ	37	25	%	69	45	E	101	65	e
6	06	^F ACK	38	26	&	70	46	F	102	66	f
7	07	^G BEL	39	27	'	71	47	G	103	67	g
8	08	^H BS	40	28	(	72	48	H	104	68	h
9	09	^I HT	41	29	)	73	49	I	105	69	i
10	0A	^J LF	42	2A	*	74	4A	J	106	6A	j
11	0B	^K VT	43	2B	+	75	4B	K	107	6B	k
12	0C	^L FF	44	2C	,	76	4C	L	108	6C	l
13	0D	^M CR	45	2D	-	77	4D	M	109	6D	m
14	0E	^N SO	46	2E	.	78	4E	N	110	6E	n
15	0F	^O SI	47	2F	/	79	4F	O	111	6F	o
16	10	^P DLE	48	30	0	80	50	P	112	70	p
17	11	^Q DC1	49	31	1	81	51	Q	113	71	q
18	12	^R DC2	50	32	2	82	52	R	114	72	r
19	13	^S DC3	51	33	3	83	53	S	115	73	s
20	14	^T DC4	52	34	4	84	54	T	116	74	t
21	15	^U NAK	53	35	5	85	55	U	117	75	u
22	16	^V SYN	54	36	6	86	56	V	118	76	v
23	17	^W ETB	55	37	7	87	57	W	119	77	w
24	18	^X CAN	56	38	8	88	58	X	120	78	x
25	19	^Y EM	57	39	9	89	59	Y	121	79	y
26	1A	^Z SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL