# Reference Manual

## VL-7507
## VL-75CT07

24-Line Opto 22 Interface Card for the STD Bus

STD

VERSALOGIC CORPORATION

# VL-7507
# VL-75CT07

24-Line Opto 22 Interface Card
for the STD Bus

# Model VL-7507

## 24-Line Opto 22 Interface Card for the STD Bus

## REFERENCE MANUAL

| | |
|---|---|
| VL-7507 | Rev. 0.00 |
| VL-75CT07 | Rev. 0.01 |
| Doc. Rev. | 8/27/93 |

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M7507

# Model VL-7507
# General Purpose 24-Line Interface Card

## REFERENCE MANUAL

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# Section 1
# OVERVIEW

## INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7507 interface card. This card is designed to interface directly with modular solid state relay rack systems available from Opto 22, Gordos, Motorola, and others. With high power output drivers and filtered input lines this board is also ideal for many general purpose TTL interfacing applications.

The card is available in standard (VL-7507) and extended temperature (VL-75CT07) versions. Throughout this manual "VL-7507" will be used to refer to both versions of these boards, unless specifically noted otherwise.

## OVERVIEW

The VL-7507 provides 24 I/O lines, four with interrupt capability. The board occupies four consecutive I/O addresses. It includes a 50-pin card edge connector, and has provisions for an optional 50-pin header assembly which may be used in place of the card edge connector.

It is plug compatible with industry standard 4, 8, 16, and 24-position modular I/O racks. It is also compatible with addressable type I/O racks from Opto 22 and Adatek which permit many racks to be daisy-chained and controlled by one VL-7507 card.

The VL-7507 is also ideal for general purpose I/O interfacing with TTL type signals.

Each input channel is individually filtered to minimize noise induced errors at the input buffer. Reading a channel that is currently programmed as an output, inputs the current state of the output line (output readback).

Each open collector output line provides 20 ma of drive (sink) to interface directly with solid state AC or DC control modules, or other TTL devices. The outputs are latched, fully buffered, and are automatically cleared during system reset.

Each VL-7507 I/O line is individually programmable as an input or an output. This allows mixing of input and output type modules in any combination desired. All of the channels will interface directly with standard AC or DC input or output modules.

An on-board rack power control can be used to turn the modular I/O rack on or off under software control. It provides up to 500 ma at 4.70 VDC (typical). The state of the rack power line is indicated by an on-board LED.

The VL-7507 features 8 and 10-bit addressing, and is compatible with all common STD Bus processor types. The IOEXP line is also supported.

The board is fully compatible with the Pro-Log 7507 card.

## FEATURES

- 24 fully buffered bidirectional I/O lines.
- Plug compatible with standard I/O racks.
- Controls up to 24 AC or DC I/O modules.
- 8 and 10-bit address decoding.
- Noise filtered input lines.
- Four edge sensitive interrupt channels.
- Software controlled I/O rack power source.
- Optional latching header.
- Extended temperature version available.
- Universal STD Bus processor compatible.
- Plug-in replacement for Pro-Log 7507.

## SPECIFICATIONS

**Size:** Meets all STD Bus mechanical specifications

**Storage Temperature:**
- VL-7507: -40° to +75° C
- VL-75CT07: -40° to +85° C

**Free Air Operating Temperature:**
- VL-7507: 0° to +65° C
- VL-75CT07: -40° to +85° C

**Power Requirements:**
- VL-7507: 5V ±5% @ 280 ma typ. (rack off, all outputs high)
  5V ±5% @ 470 ma typ. (rack on, all outputs low)

- VL-75CT07: 5V ±10% @ 22 ma typ. (rack off, all outputs high)
  5V ±10% @ 65 ma typ. (rack off, 12 outputs low)
  5V ±10% @ 100 ma typ. (rack off, 24 outputs low)

**I/O Port Interface:**
- Low level output voltage: .7V max. @ 20 ma
- Rack power output voltage: 4.7V typ. @ 500 ma

# Section 2
# CONFIGURATION

## JUMPER SUMMARY

Various options available on the VL-7507 card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 2-1 shows the jumper block locations on the VL-7507 board. It indicates the position of the jumper plugs as shipped from the factory. The function of each jumper block is detailed in Figure 2-2.

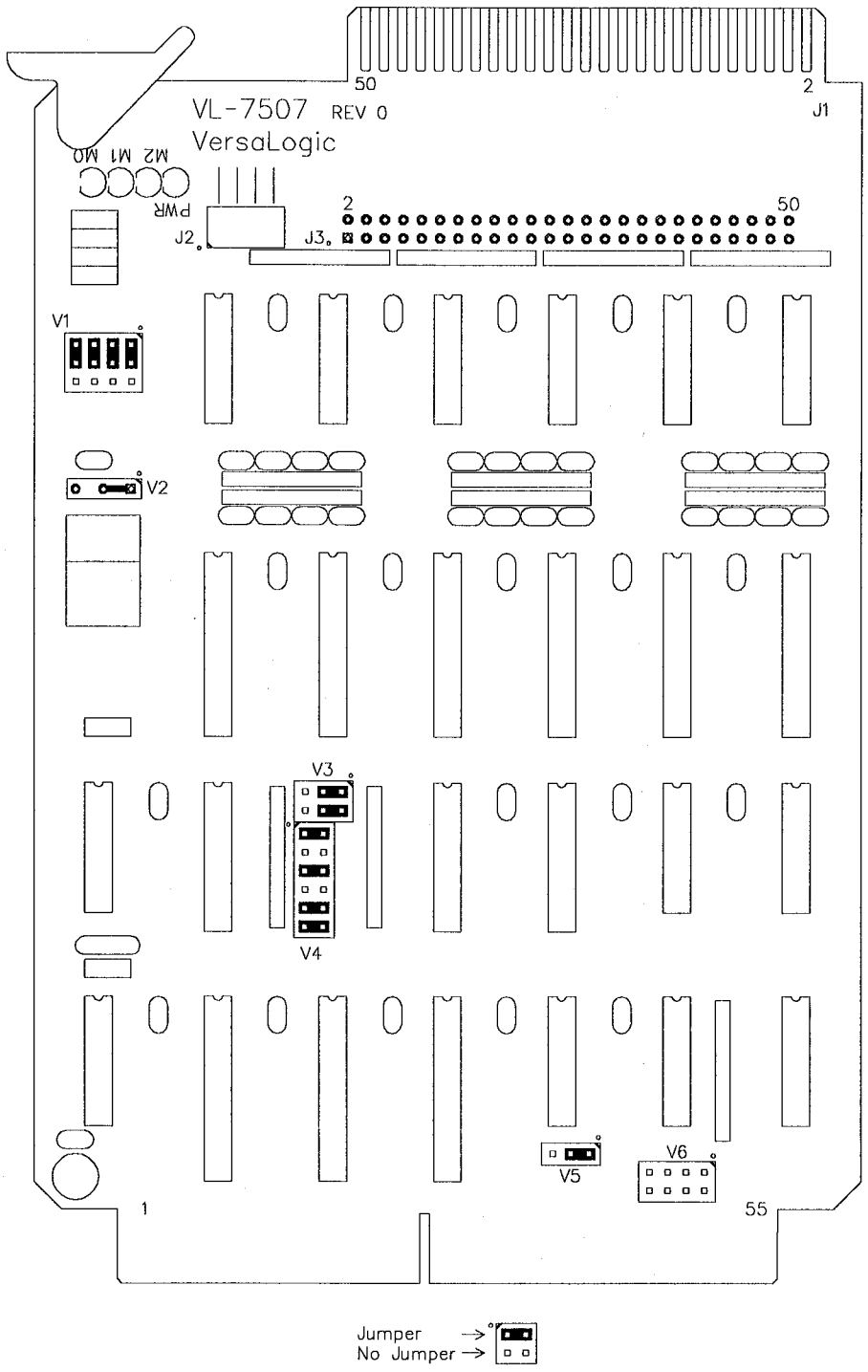



**Figure 2-1. Jumper Block Locations**

| Jumper Block | Description | As Shipped |
|---|---|---|
| V1 | Interrupt channel mode select. | (no interrupts) |
| | M0 - Module #0 mode. | M0 - I/O mode |
| | M1 - Module #1 mode. | M1 - I/O mode |
| | M2 - Module #2 mode. | M2 - I/O mode |
| | M3 - Module #3 mode. | M3 - I/O mode |
| V2 | Rack power source. | |
| | a - Software controlled. | a - IN |
| | b - Always on. | b - out |
| V3 | Address mode selector. See Board Address. | |
| | a - A9 control. | a - ignore A9 |
| | b - A8 control. | b - ignore A8 |
| V4 | Board Address. See Board Address. | Hex 50 |
| V5 | IOEXP select. See Board Address. | |
| | a - Don't care. | a - IN |
| | b - Active low. | b - out |
| | - - Active high (both jumpers out). | |
| V6 | Interrupt to INTRQ* enable. | (all disabled) |
| | M0 - Module #0 interrupt. | M0 - out |
| | M1 - Module #1 interrupt. | M1 - out |
| | M2 - Module #2 interrupt. | M2 - out |
| | M3 - Module #3 interrupt. | M3 - out |

**Figure 2-2. Jumper Functions**

## BOARD ADDRESS

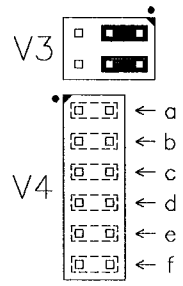
The VL-7507 supports both 8 and 10-bit I/O addressing. 8-bit addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10-bit addressing can be used with 16-bit processors (i.e. 8088) to decode up to 1024 I/O port addresses.

Both 8 and 10-bit addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7507.

As shipped the board is configured for 8-bit addressing with a board address of hex 50. The VL-7507 occupies four consecutive I/O addresses (i.e. 50-53).

## 8-Bit Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired address (i.e. "3" & "0" = hex address 30).



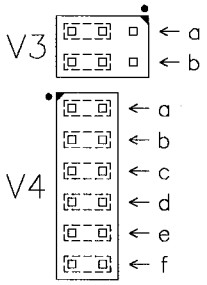

| V4 | | | | Upper Hex | V4 | | Lower Hex |
|---|---|---|---|---|---|---|---|
| a | b | c | d | Digit | e | f | Digit |
| X | X | X | X | 0 | X | X | 0 |
| X | X | X | - | 1 | X | - | 4 |
| X | X | - | X | 2 | - | X | 8 |
| X | X | - | - | 3 | - | - | C |
| X | - | X | X | 4 | | | |
| X | - | X | - | 5 | | | |
| X | - | - | X | 6 | | | |
| X | - | - | - | 7 | | | |
| - | X | X | X | 8 | | | |
| - | X | X | - | 9 | | | |
| - | X | - | X | A | | | |
| - | X | - | - | B | | | |
| - | - | X | X | C | | | |
| - | - | X | - | D | | | |
| - | - | - | X | E | | | |
| - | - | - | - | F | | | |

X = Jumper installed
- = Jumper removed

**Figure 2-3. 8-Bit Address Jumpers**

**10-Bit Addressing**

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e. "1" & "3" & "0" = hex address 130).




| V3 a | V3 b | Upper Digit | V4 a | V4 b | V4 c | V4 d | Middle Digit | V4 e | V4 f | Lower Digit |
|---|---|---|---|---|---|---|---|---|---|---|
| X | X | 0 | X | X | X | X | 0 | X | X | 0 |
| X | - | 1 | X | X | X | - | 1 | X | - | 4 |
| - | X | 2 | X | X | - | X | 2 | - | X | 8 |
| - | - | 3 | X | X | - | - | 3 | - | - | C |
| | | | X | - | X | X | 4 | | | |
| | | | X | - | X | - | 5 | | | |
| | | | X | - | - | X | 6 | | | |
| | | | X | - | - | - | 7 | | | |
| | | | - | X | X | X | 8 | | | |
| | | | - | X | X | - | 9 | | | |
| | | | - | X | - | X | A | | | |
| | | | - | X | - | - | B | | | |
| | | | - | - | X | X | C | | | |
| | | | - | - | X | - | D | | | |
| | | | - | - | - | X | E | | | |
| | | | - | - | - | - | F | | | |

X = Jumper installed
- = Jumper removed

**Figure 2-4. 10-Bit Address Jumpers**

**IOEXP Signal**

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown in Figure 2-5.


| Jumper | Setting | Description |
|---|---|---|
| V5 | a - | Ignore IOEXP (enable high or low). |
| | b - | Enable on IOEXP low. |
| | None - | Enable on IOEXP high. |

**Figure 2-5. IOEXP Options**

**INTERRUPTS**

The VL-7507 board includes four special interrupt channels which can be used with rack modules #0-3. These edge sensitive interrupts, which can be enabled and disabled under software control, will directly interrupt the system processor when the desired input line changes state. The states of the four interrupt channels may be polled (read from the card) at any time. Interrupt outputs are also available for connection to an external card for interrupt prioritization.

Two sets of jumpers control interrupt operation. The V1 jumpers configure each channel as either a standard I/O channel, or as an interrupt (input only) channel. Jumper block V6 allows each interrupt signal to be connected to the interrupt request line (INTRQ*) on the STD Bus. Normally the corresponding jumper in both block V1 and V6 must be set for the desired channel before an interrupt will occur.

As shown below each of the jumpers in blocks V1 and V6 correspond to an I/O rack module (#M0-M3). The I/O or interrupt mode may be selected individually for each of these channels.

Jumper block V1 allows each of the four channels to be jumpered for regular I/O mode operation (upper position) or for interrupt mode operation (lower jumper position).

Jumper block V6 allows each interrupt to be enabled (jumper in), or disabled (jumper out). If the interrupt outputs are connected to an external priority encoder card (via connector J2) then these jumpers should be left out.

Operation of the interrupt channels is discussed further in the Operation section.

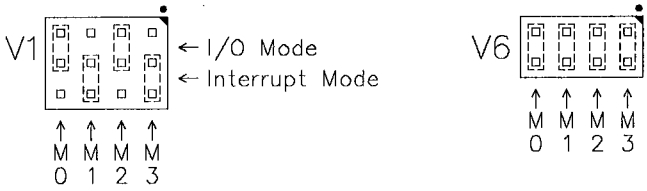



**Figure 2-6. Interrupt Mode Jumpers**

## RACK POWER CONTROL

The VL-7507 board includes provisions for powering the external I/O rack assembly with +5 volts. In addition, this power source can be controlled by the system software to turn the entire rack on or off as desired.

Jumper V2 allows the rack power control circuitry to be bypassed. In jumper position "b" the I/O rack power line (pin 49) is connected directly to +5 volts on the STD Bus and the rack can not be turned off thru software commands. This jumper option is detailed below.

If the I/O rack is powered by a separate external supply then a jumper must be removed from the I/O rack (see THE I/O RACK below), or both of the V2 jumpers should be removed from the VL-7507 board.

The current state of the I/O rack power output is indicated by the "PWR" LED at the edge of the board.


| Jumper Block | Description | As Shipped |
|---|---|---|
| V2 | Rack power source. | |
| | a - Software controlled. | a - IN |
| | b - Always on. | b - out |
| | - - Externally powered (both jumpers out). | |

**Figure 2-7. Rack Power Source Jumper**

## THE I/O RACK

Modular I/O racks are configured by placing the desired type of interface module in each position in the rack. Although the modules can be mixed in any way desired, it generally simplifies the system software to have all the inputs and all the outputs grouped together (rather than intermingled).

The +5 volt power required by the I/O rack can be taken from an external supply or from the STD Bus (via the data interface cable). If an external supply is used then the jumper on the I/O rack must be cut so that no power connection is made to the card edge connector. If power is to be taken from the STD Bus, then the power jumper on the I/O rack should be left in.

Note that +5 volt power line from the VL-7507 card can be shorted to ground if the connectors are not correctly oriented at either end of the interface cable. The use of keys in the connectors, or very clear markings on the connectors, is recommended to prevent backwards connection of the cable.

The VL-7507 connects directly to 4, 8, 16, and 24-position racks using VersaLogic cable assembly #9561. It is also compatible with addressable racks from Opto 22 and Adatek. Addressable racks permit many racks to be daisy-chained and controlled by one VL-7507 card.

# Section 3
# INSTALLATION

## HANDLING

** CAUTION ** The VL-7507 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

## INSTALLATION

The VL-7507 card can be installed in any slot of an STD Bus card cage.

The VL-7507 does not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on this board are connected together so that the priority chain will not be broken. This board may be inserted between other boards that are using the priority chain.

** CAUTION ** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

** CAUTION ** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

## EXTERNAL CONNECTIONS

Connection to the VL-7507 can be made as noted below. Pinout listings for these connectors appear on the following pages.

### Connector J1

Connector J1 is a 50-pin edge connector (on .1" centers) that is plug compatible with Opto 22 type I/O racks. It may be connected to Opto 22 type I/O racks with VersaLogic cable assembly #9561. Mating connectors include 3M #3415-0001 connector with #3439-1 keys and Ansley #609-5015M with #609-0005 keys. The use of keys with this connector is recommended since an incorrectly oriented connector can cause damage to the VL-7507 card.

### Connector J2

Connector J2 is a dual 4-pin right angle header (on .1" centers) which makes the on-board interrupt signals accessible to an external prioritizer card. Use a mating 2-pin connector such as an AMP #530554-1 + (2) #530553-5 for each of the four interrupts used.

### Connector J3

Connector J3 is an optional 50-pin right angle header (on .1" centers) that can be installed and used in place of connector J1. It may be connected directly to Opto 22 type I/O racks with VersaLogic cable assembly #9564. Mating connectors include 3M # 3425-7-50 and Ansley # 609-5041CE.

| J1 & J3 Pin | Signal Name | VL-7507 Input Load (Sink ma) | VL-7507 Output Drive (Sink ma) | VL-75CT07 Input Load (Sink ma) | VL-75CT07 Output Drive (Sink ma) |
|---|---|---|---|---|---|
| 1 | MOD 23* | 4.8 | 20 | 0.5 | 20 |
| 3 | MOD 22* | 4.8 | 20 | 0.5 | 20 |
| 5 | MOD 21* | 4.8 | 20 | 0.5 | 20 |
| 7 | MOD 20* | 4.8 | 20 | 0.5 | 20 |
| 9 | MOD 19* | 4.8 | 20 | 0.5 | 20 |
| 11 | MOD 18* | 4.8 | 20 | 0.5 | 20 |
| 13 | MOD 17* | 4.8 | 20 | 0.5 | 20 |
| 15 | MOD 16* | 4.8 | 20 | 0.5 | 20 |
| 17 | MOD 15* | 4.8 | 20 | 0.5 | 20 |
| 19 | MOD 14* | 4.8 | 20 | 0.5 | 20 |
| 21 | MOD 13* | 4.8 | 20 | 0.5 | 20 |
| 23 | MOD 12* | 4.8 | 20 | 0.5 | 20 |
| 25 | MOD 11* | 4.8 | 20 | 0.5 | 20 |
| 27 | MOD 10* | 4.8 | 20 | 0.5 | 20 |
| 29 | MOD 9* | 4.8 | 20 | 0.5 | 20 |
| 31 | MOD 8* | 4.8 | 20 | 0.5 | 20 |
| 33 | MOD 7* | 4.8 | 20 | 0.5 | 20 |
| 35 | MOD 6* | 4.8 | 20 | 0.5 | 20 |
| 37 | MOD 5* | 4.8 | 20 | 0.5 | 20 |
| 39 | MOD 4* | 4.8 | 20 | 0.5 | 20 |
| 41 | MOD 3* | 4.8 | 20 | 0.5 | 20 |
| 43 | MOD 2* | 4.8 | 20 | 0.5 | 20 |
| 45 | MOD 1* | 4.8 | 20 | 0.5 | 20 |
| 47 | MOD 0* | 4.8 | 20 | 0.5 | 20 |
| 49 | RACK POWER | - | 500 | - | 500 |
| 2-50 all even numbered pins are ground. | | | | | |

Notes:
"*" Notes an inverted signal (true = low).
VL-7507 input load (1K ohm pull up) is specified at .4 volts.
VL-75CT07 input load (10K ohm pull up) is specified at .4 volts.
Output drive (20 ma min.) is specified at .7 volts (max.).
See Special Applications for notes about output drive.

**Figure 3-1. Connector J1 and J3 (Opt.) Pinout**

| J2 Pin | Signal Name | Output Drive VL-7507 | Output Drive VL-75CT07 |
|---|---|---|---|
| 1 | GND | | |
| 2 | INT MOD0 | 20 ma | 8 ma |
| 3 | GND | | |
| 4 | INT MOD1 | 20 ma | 8 ma |
| 5 | GND | | |
| 6 | INT MOD2 | 20 ma | 8 ma |
| 7 | GND | | |
| 8 | INT MOD3 | 20 ma | 8 ma |

**Figure 3-2. Connector J2 Pinout**

# Section 4
# OPERATION

## INTRODUCTION

This section includes general information about the use and operation of the VL-7507 card. It focuses primarily on the software commands necessary to operate the card and includes various examples to assist you in constructing your own software routines.

## I/O PORT MAPPING

The VL-7507 occupies four I/O port addresses. Three addresses are used to access the 24 I/O channels (lines), while a fourth address is used to control the I/O rack power.

The locations of these four ports is determined by the board address, which is jumper selectable. As shipped, the board is jumpered for hex address 50.

Once the board's I/O address has been determined, the addresses of the four I/O ports can be determined as shown in Figure 4-1. Each I/O module port can be both read (for inputting data) and written (for outputting data).

Figure 4-2 shows how each I/O module channel corresponds to the data bits in the I/O port addresses. This example uses the default board address of hex 50.

Note that only bits M0-M7 are used with 8-position racks. Bits M0-M15 are used with 16-position racks.

| Port Address | Read/ Write | Function/ Module # |
|---|---|---|
| Board Address + 3 | R | Interrupt Status |
| Board Address + 3 | W | Rack Power |
| Board Address + 2 | R/W | 0-7 |
| Board Address + 1 | R/W | 8-15 |
| Board Address + 0 | R/W | 16-23 |

**Figure 4-1. I/O Port Locations**

| ADDR. | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 53 | W | RACK POWER | - | - | - | - | - | - | - |
| 53 | R | IS0 | IS1 | IS2 | IS3 | ? | ? | ? | ? |
| 52 | R/W | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| 51 | R/W | M8 | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| 50 | R/W | M16 | M17 | M18 | M19 | M20 | M21 | M22 | M23 |

R/W = Read, Write, or Read/Write. - = Don't care (ignored).
ISx = Interrupt Status channel x. ? = Unknown (high or low).
Mx = I/O Module channel x.

**Figure 4-2. Module Channel Mapping**

## DIRECTION CONTROL

Any of the VL-7507's 24 channels may be used as an input or an output channel. The function of each channel is determined by its programming. When the system is powered-up, or a system reset occurs, all of the channels are reset to inputs. Channels connected as outputs will appear high due to the pull-up resistor on each channel.

Channels can be used as outputs by simply by writing a zero or one to it. Writing a one causes the inverting open collector buffer to go into an active low state. Writing a zero returns the buffer to an inactive (open collector) state, and the channel can be used as an input or an output.

Channels that are used as inputs may be read at any time, but they must never have a one written to them. When writing to ports which include both input and output channels, be certain to set the input channel bits to zero. A channel will act as an input as long as it is read, or zeros are written to it.

When a channel being used as an output is read, the data will reflect the current state of the output (if a one is written, a one will be read, etc.).

## READING AND WRITING DATA

All of the I/O buffers on the VL-7507 board are inverting (to set an output pin low, write a one, etc.). However, I/O rack modules also use active low (inverted) signals. The resulting data interface levels between the VL-7507 and I/O rack modules are are shown in Figure 4-3.

When a one has been written to an output channel (setting the pin low), the data read from that channel will be one.

Note that the data read always reflects the actual state of the I/O pin. If an I/O pin is shorted to ground it will always read as a one. Trying to output a high or low state to the pin will have no effect on the data read.

| Data Written | I/O Pin | Output Modules | Input Modules | I/O Pin | Data Read |
|---|---|---|---|---|---|
| 0 | (1) | Power off | Voltage absent | (1) | 0 |
| 1 | (0) | Power on | Voltage present | (0) | 1 |

**Figure 4-3. I/O Module Data Interface**

## SOFTWARE EXAMPLES

Reading a VL-7507 channel (data bit) is fairly straightforward although care must be taken to select the proper port and data bit which corresponds to the desired I/O module. Writing to a channel can also be achieved in a single operation, but provisions must be made so as to not disturb the current state of the other seven channels which appear at the same I/O port.

In systems where more than a few I/O rack modules are used, both of these operations can be made much easier with generalized subroutines that read or write to a specified channel number. These subroutines calculate the port address and data bit involved and allow the programmer to concentrate on reading or writing to the required I/O module. Subroutines of this type are shown in the examples that follow.

The VL-7507 can be used with any language that allows direct access to system I/O ports. The examples below are shown in several programming languages. These examples have not necessarily been tested or verified for proper operation. They are supplied for general information only and may not be appropriate for any specific application.

### Assembly Language Examples

The following Z80 program fragments illustrate how the VL-7507 board can be used in an assembly language environment.

The first example illustrates direct access to each desired I/O channel. This method is sometimes appropriate when there is only a small number of modules connected to the interface. It requires the programmer to determine the related port and bit of the desired channel.

The second example illustrates access by channel number. It uses subroutines to read or write to a specified channel, freeing the programmer from unnecessary calculations during program construction.

```
                    ;Example 1.  Direct access to the VL-7507.
                    ;Copyright 1986, VersaLogic, Eugene, OR
                    ;
                    ;Define all port locations.
          0050      RIOBASE   EQU   50H     ;Board address = hex 50.
          0050      RACK0     EQU   RIOBASE + 0     ;Port 0 (channels 16-23).
          0051      RACK1     EQU   RIOBASE + 1     ;Port 1 (channels 8-15).
          0052      RACK2     EQU   RIOBASE + 2     ;Port 2 (channels 0-7).
          0053      RACKPWR   EQU   RIOBASE + 3     ;Power control port.
                    ;
                    ;Define channel usage (high bits are output channels).
          0003      RACKU0    EQU   00000011B       ;Port 0 (channels 16-23).
          0000      RACKU1    EQU   00000000B       ;Port 1 (channels 8-15).
          00FC      RACKU2    EQU   11111100B       ;Port 2 (channels 0-7).
                    ;
0100                ORG       100H      ;Start of code.
                    ;
                    ;
                    ;Reading a relay channel (state of input or output channel).
0100  DB 50             IN  A,(RACK0)   ;Read the I/O port.
0102  E6 02             AND 00000010B   ;Mask out all channels except #22.
0104  20 02             JR  NZ,ON22     ;Jump to somewhere if channel is ON.
                    ;
                    ;User routine for channel on.
0106  00            ON22    NOP
                    ;
                    ;
                    ;Setting a channel ON (output pin low).
0107  DB 51             IN  A,(RACK1)   ;Read the current state of the outputs.
0109  F6 40             OR  01000000B   ;Set the channel #9 bit ON.
010B  E6 FC             AND RACKU2      ;Clear input channel bits.
010D  D3 52             OUT (RACK2),A   ;Write it to the board.
                    ;
                    ;
                    ;Setting a channel OFF (output pin high).
010F  DB 52             IN  A,(RACK2)   ;Read the current state of the outputs.
0111  E6 FB             AND 11111011B   ;Set the channel #5 bit OFF.
0113  E6 FC             AND RACKU2      ;Clear input channel bits.
0115  D3 52             OUT (RACK2),A   ;Write it to the port.
```

```
                    ;Example 2 - Accessing the VL-7507 by channel #.
                    ;Copyright 1986, VersaLogic, Eugene, OR
                    ;
     0050           RACKADDR EQU 50H          ;Board address = hex 50.
                    ;
                    ;I/O usage table.  High bits are output channels.
     00F0           RAKU0   EQU  11110000B    ;Port 0 (channels 16-23).
     00FC           RAKU1   EQU  11111100B    ;Port 1 (channels 8-15).
     00FF           RAKU2   EQU  11111111B    ;Port 2 (channels 0-7).
                    ;
0100                        ORG  100H         ;Start of code.
                    ;
                    ;reading a relay channel (state of input or output).
0100  3E 0C                 LD   A,12         ;Specify channel 12
0102  CD 14 01              CALL READ         ;Read it (result in A)
0105  C2 09 01              JP   NZ,DUMMY     ;Jump somewhere if it is ON.
0108  00                    NOP               ;(do something else if it isn't)
0109  00             DUMMY  NOP               ;(user routine)
                    ;
                    ;
                    ;Setting a channel ON (output pin low).
010A  3E 09                 LD   A,9          ;Specify channel 9
010C  CD 1E 01              CALL ON           ;Turn it ON
                    ;
                    ;
                    ;Setting a channel OFF (output pin high).
010F  3E 16                 LD   A,22          ;Specify channel 22
0111  CD 28 01              CALL OFF           ;Turn it OFF
                    ;
                    ;
                    ;** SUBROUTINES **
                    ;Reads a channel (input or output). Chan.# (0-23) is in A.
                    ;Returns the state of the channel (0 or 1) in reg. A.
0114  CD 36 01      READ   CALL FIND          ;Convert the channel #.
0117  ED 78                IN   A,(C)        ;Read the port.
0119  A0                   AND  A,B          ;Mask for desired bit.
011A  C8                   RET  Z            ;Return if 0.
011B  3E 01                LD   A,1          ;Or else plug with a 1
011D  C9                   RET               ;and return.
                    ;
                    ;Sets an output channel ON. Chan.# (0-23) is in reg. A.
                    ;Note:  Won't work unless channel is defined as an
                    ;output in the usage registers.
011E  CD 36 01      ON     CALL FIND          ;Convert the channel #.
0121  ED 78                IN   A,(C)        ;Read current output states.
0123  B0                   OR   B            ;Set channel on.
0124  A2                   AND  D            ;Clear input channel bits.
0125  ED 79                OUT  (C),A        ;Write it to the port.
0127  C9                   RET               ;Return.
                    ;
                    ;Sets an output channel off. Chan.# (0-23) is in reg. A.
0128  CD 36 01      OFF    CALL FIND          ;Convert the channel #.
012B  78                   LD   A,B          ;Complement B (bit mask).
012C  EE FF                XOR  A,0FFH
```

```
012E  47              LD   B,A
012F  ED 78           IN   A,(C)        ;Read current output states.
0131  A0              AND  B            ;Set channel off.
0132  A2              AND  D            ;Clear input bits.
0133  ED 79           OUT  (C),A        ;Write it to the port.
0135  C9              RET               ;Return
                    ;
                    ;Computes the port address and bit mask for the requested
                    ;channel # (in register A).
                    ;Returns A=0, B=bit mask, C=port address, D=usage mask
0136  3C        FIND  INC  A            ;Offset channel # by 1.
0137  06 80           LD   B,80H        ;Initialize B, for channel #0.
0139  0E 50           LD   C,RACKADDR   ;Initialize C, for channel #0.
013B  21 4E 01        LD   HL,U2        ;Usage table address to HL.
013E  56              LD   D,(HL)       ;Initialize D, for channel #0.
013F  3D        L1    DEC  A            ;Decrement channel #.
0140  C8              RET  Z            ;Done when A=0.
0141  CB 18           RR   B            ;Rotate bit mask.
0143  30 FA           JR   NC,L1        ;Loop if no carry.
0145  0D              DEC  C            ;Adjust port address.
0146  2B              DEC  HL           ;Adjust usage table pointer.
0147  56              LD   D,(HL)       ;D=usage mask.
0148  CB 18           RR   B            ;Carry -> D7.
014A  18 F3           JR   L1           ;Continue.
                    ;
                    ;Usage table.  Note: This table MUST be three bytes long.
014C  F0        U0    DB   RAKU0
014D  FC        U1    DB   RAKU1
014E  FF        U2    DB   RAKU2
                    ;
```

**BASIC Language Examples**

The subroutines and program fragments in the first listing below illustrate how the VL-7507 board can be used with standard BASICs (or other high level languages) that include logical AND, OR, and XOR functions. Microsoft's BASIC-80 is used in this example.

Users of VersaLogic's C4 BASIC language should refer to the second listing which shows these same functions written in C4 BASIC. Note that the C4 BASIC RIN and ROUT statements are compatible with VersaLogic's MIO-24 board only. They should not be used with the VL-7507.

Notice: These routines may not operate correctly with some BASICs or be suitable for your application.

```
10 REM Microsoft BASIC-80 language example for the VL-7507 board.
20 REM
50 REM Set address of Rack Interface (RI) board (50 hex = 80 decimal)
51 RI = 80
70 REM Set usage flags for each port (8 channels each)
71 REM Output channels are a "O", inputs are a "I"
72 U$(2)="IIOOOOOO" : REM Port 2, channels 0-7
73 U$(1)="OOOOOOOO" : REM Port 1, channels 8-15
74 U$(0)="IIIIIOOO" : REM Port 0, channels 16-23
80 REM And initialize the conversion routine.
81 GOSUB 600
 .
 .
100 REM Turn ON channel 11
101 CHAN=11: GOSUB 570
 .
 .
150 REM Read channel 0 and do something if it's ON.
151 CHAN=0: GOSUB 510
152 IF STATE = 1 THEN GOTO 1000
 .
170 REM Turn channel 8 OFF.
171 CHAN=8: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7507 BOARD.
501 REM These routines are called with the channel # in "CHAN".
502 REM Input data is returned in "STATE" (1=ON, 0=OFF).
503 REM The startup routine (at 600) must be called before the other
504 REM routines are used.

510 REM Read the channel in "CHAN" (0-23)
520 X=INT((23-CHAN)/8): STATE=INP(RI+X) AND 2^(CHAN-8*X)
525 IF STATE > 0 THEN STATE=1
530 RETURN

540 REM Turn OFF channel "CHAN" (0-23)
550 X=INT((23-CHAN)/8)
555 OUT RI+X,(INP(RI+X) AND U(X) AND (255 XOR 2^(CHAN-8*X)))
560 RETURN

570 REM Turn ON channel "CHAN" (0-23)
580 X=INT((23-CHAN)/8): OUT RI+X,(INP(RI+X) AND U(X) OR 2^(CHAN-8*X)
590 RETURN

600 REM Initialization routine
601 REM Converts the usage strings into decimal byte masks
610 FOR N = 0 TO 2 : U(N)=0
620 FOR X = 0 TO 7
630 IF MID$(U$(N),8-X,1) <> "I" then U(N)=U(N) + (2^X)
640 NEXT X : NEXT N
650 RETURN
```

```
10 REM VersaLogic C4 BASIC language example for the VL-7507 board.
20
50 REM Set address of Rack Interface (R1) board (50 hex)
51 R1 = &50
70 REM Set usage flags for each port (8 channels each)
71 REM Values are in HEX.  Output channels are a 1, inputs are a 0.
72 U2=&4F : REM Port 2, channels 0-7
73 U1=&C0 : REM Port 1, channels 8-15
74 U0=&FF : REM Port 0, channels 16-23
 .
 .
 .
100 REM Turn ON channel 11
101 C=11: GOSUB 570
 .
 .
150 REM Read channel 0 and do something if it's ON.
151 C=0: GOSUB 510
152 IF S = 1 GOTO 1000
 .
170 REM Turn channel 8 OFF.
171 C=8: GOSUB 540
 .
 .

500 REM SUBROUTINES FOR VL-7507 BOARD.
501 REM These routines are called with the channel # in "C".
502 REM Input data is returned in "S" (1=ON, 0=OFF).

510 REM Read the channel in "C" (0-23)
520 GOSUB 595 : S=IN(R1+X) AND X1 : If S>0 S=1
530 RETURN

540 REM Turn OFF channel "C" (0-23)
550 GOSUB 595 : OUT R1+X,(IN(R1+X) AND U(X) AND (NOT (X1))
560 RETURN

570 REM Turn ON channel "C" (0-23)
580 GOSUB 595 : OUT R1+X,(IN(R1+X) AND U(X) OR X1)
590 RETURN

594 REM Computes port addr offset and bit mask for routines above
595 X=((23-C)/8): X1=1: X2=MOD((23-C),8): IF X2=0 RETURN
596 FOR X3 = 1 TO X2 : X1=X1*2 : NEXT X3
597 RETURN
```

## I/O RACK POWER CONTROL

The VL-7507 includes a software controlled output for supplying +5 volt power to the I/O rack (from the STD Bus). The software control may be defeated (power always on) with jumper V2 (see the Configuration section). This control has no effect if the I/O rack is powered from an external power source.

The rack power is controlled with data bit 7 at the board address + 3 (port address 53 as shipped). Data bits 0-6 at this port have no function and are ignored. Writing 00 to the port will turn on the rack; writing FF to the port will turn off the rack. The rack power is turned on at power-up or system reset.

The I/O rack control may be used for disabling the entire rack in emergency situations (although it will be turned back on when the system is reset). It can also be used to disable the I/O rack while data is written to, and read back from each channel to verify proper operation of the VL-7507 board.

The current state of the power to the I/O rack is indicated by the "PWR" LED at the edge of the VL-7507 board.

## LED INDICATORS

Four LED indicators are available at the edge of the board, primarily for use during development and troubleshooting of the system. LEDs "M0"-"M2" are on when channels 0-2 are active (a 1 written to the channel for a low output). The "M0"-"M2" LEDs will also turn on when channels 0-2 are jumpered for interrupt mode and the interrupt is enabled. The "PWR" LED is on whenever the rack power line is on.

## INTERRUPTS

The VL-7507 board includes four special channels (channels 0-3) which can optionally be used as system interrupt inputs. They can be programmed to interrupt the system processor whenever the input to the module changes from OFF to ON (the I/O pin changes from high to low). These edge sensitive interrupts are latching and will maintain the interrupt status until serviced (reset) by the processor. This allows the interrupt event to be identified, even if the cause of the interrupt has gone away (is no longer active).

If interrupts are not required for system operation this section can be ignored.

As noted in the Configuration section, two jumper blocks control interrupt operation. Jumper V1 selects between I/O and interrupt mode for each of the channels, while jumper V6 connects each interrupt output line to the INTRQ* pin on the STD Bus. Normally both of these jumpers

must be set to the interrupt position (for the desired channels) before interrupts will occur.

Interrupts are available on any (or all) of channels 0-3 (from modules 0-3 on the I/O rack board). Either AC or DC input modules may be used for interrupt input. Channels jumpered for interrupt use may still have their data read directly at the regular I/O port address.

In use, each interrupt channel can be enabled or disabled by a software command as desired. When disabled the channel can be used as a normal input channel, but it will not cause interrupts to the system. Its interrupt status bit will never be set.

When enabled, an interrupt will occur and the corresponding bit will be set in the interrupt status register whenever the input module changes from OFF to ON.

Interrupts are controlled by writing a 0 (disable) or a 1 (enable) to the corresponding I/O bit at the board address + 2. The interrupt channels are initially disabled and are reset to a disabled state when a system reset occurs.

The interrupt status of all four channels is available at board address + 3. The interrupt status is latched and will remain active (even if the input causing the interrupt turns off) until the status is read. The interrupt status register is automatically cleared immediately after it is read.

When any interrupt channels are used it is recommended that the remaining channels on port 2 (channels 0-7) be used as inputs. This will prevent inadvertent enabling/disabling of the interrupt channels while writing to output channels on this same port.

When interrupts are used the output routine examples shown elsewhere in this section (e.g. for setting channel #n ON or OFF) should not be used with this port (channels 0-7). Enabling and disabling the interrupts must be done directly, not with the output subroutines provided.

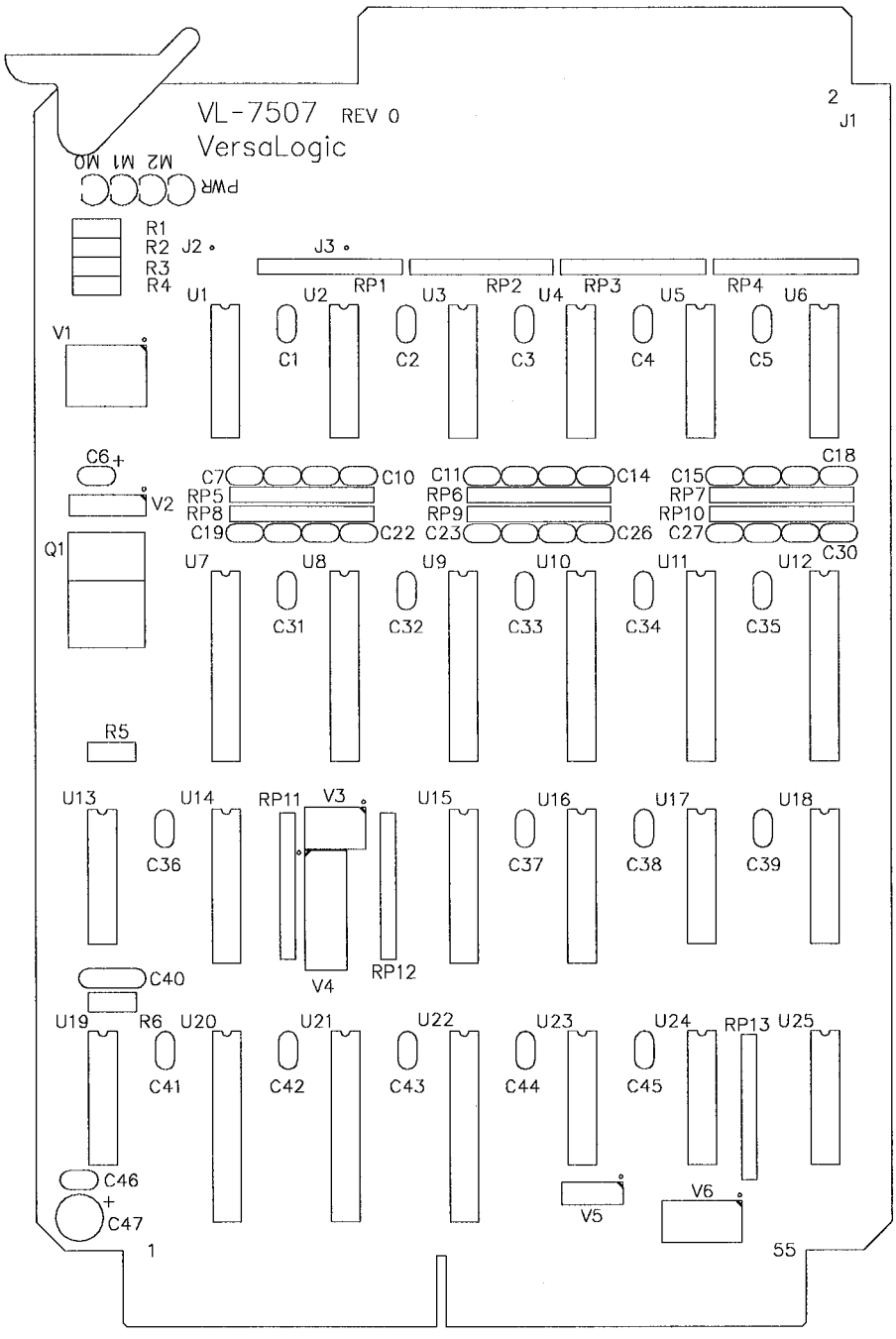
For special applications, interrupt status output lines are available at connector J2 for connection to an interrupt priority encoder card. If the outputs on J2 are used to handle the interrupts, then the jumpers on block V6 should be removed so that the interrupts are no longer connected to the system INTRQ* line. When a priority encoder card is used, the VL-7507 interrupts may still be enabled or disabled with the commands described above.

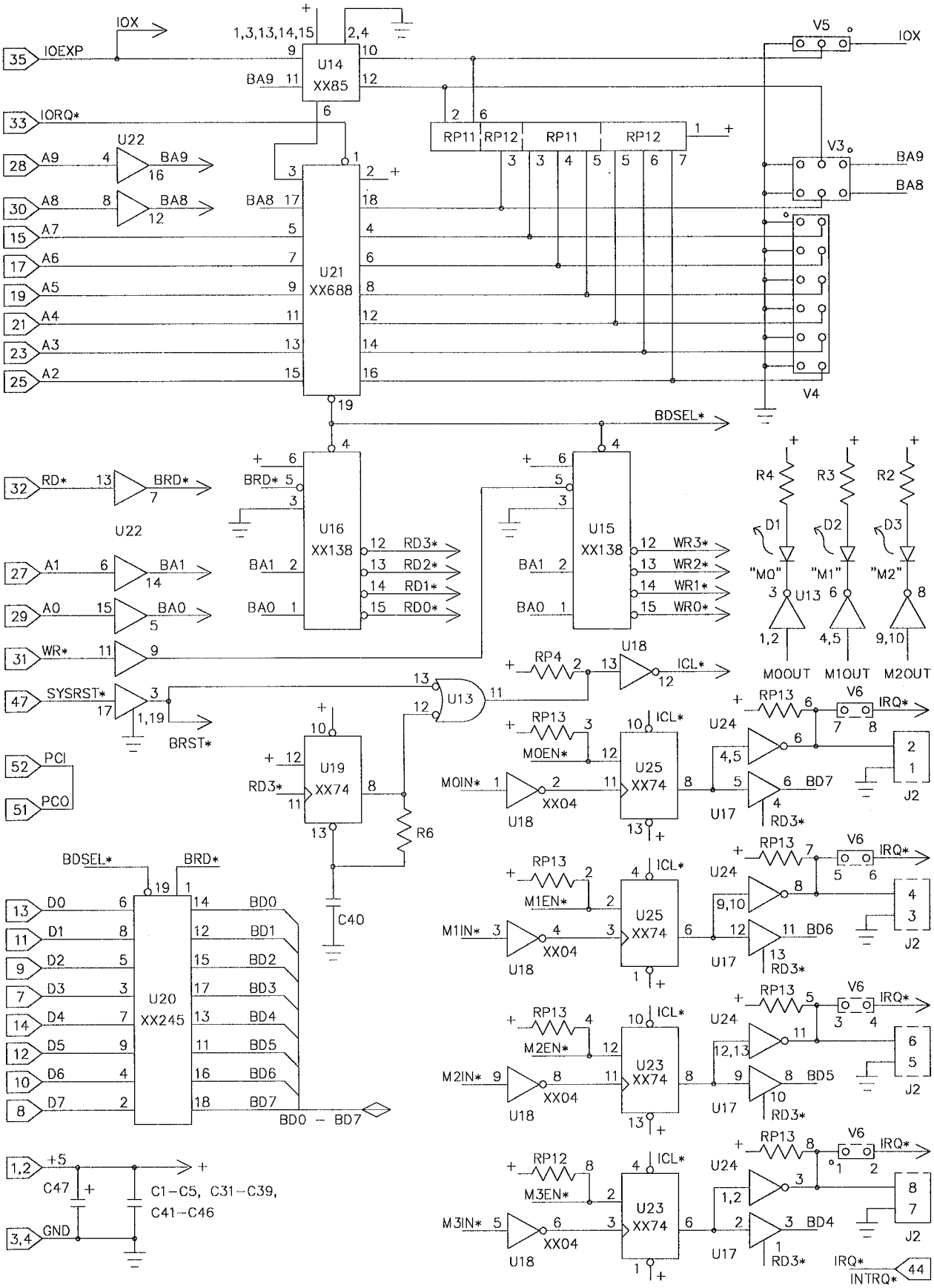
**SPECIAL APPLICATIONS**

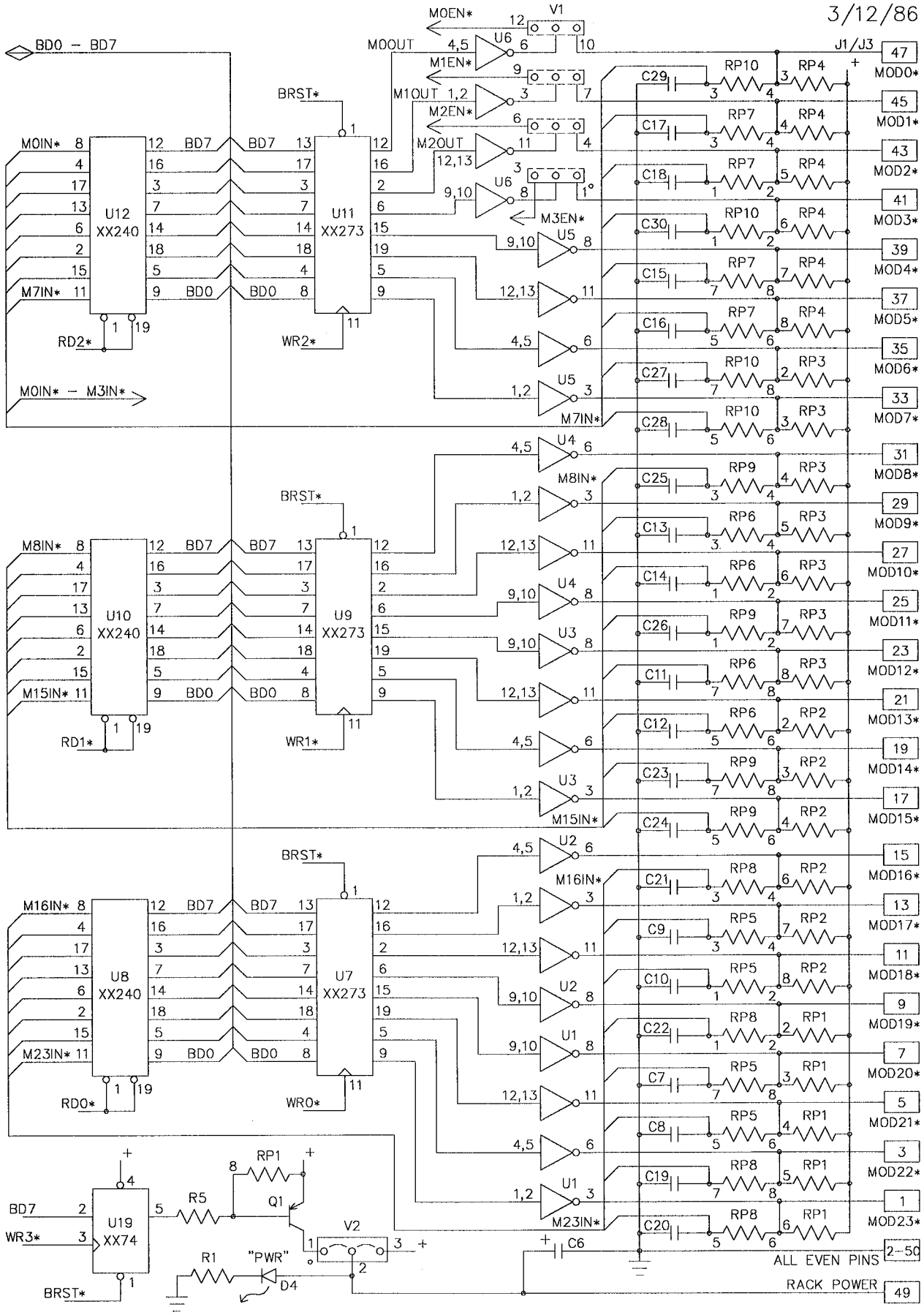
Normally the VL-7507 board is used to interface with Opto 22 type solid state I/O modules. However, it is also quite useful as a general purpose TTL I/O interface board. This section includes notes which pertain to general purpose and special applications.

The input and output chips on the VL-7507 are socketed and may be removed or replaced for special applications. The output chips (U1-U6) are normally open collector drivers. However, they are plug compatible with 74LS00 type chips. This allows them to be replaced with standard (non-open collector) TTL type drivers if desired. In this case the pull-up resistors (RP1-RP4) should also be removed from the board.

Some or all of the output driver chips may also be removed from the board completely (in 4 channel increments) to save power when some channels will be used for input only.


VL-7507 REV 0
VersaLogic
2
J1
M2 M1 M0
PWR
R1
R2
R3
R4
J2
J3
RP1
RP2
RP3
RP4
U1
U2
U3
U4
U5
U6
C1
C2
C3
C4
C5
V1
C6
C7
C10
C11
C14
C15
C18
V2
RP5
RP6
RP7
RP8
RP9
RP10
C19
C22
C23
C26
C27
C30
Q1
U7
U8
U9
U10
U11
U12
C31
C32
C33
C34
C35
R5
U13
U14
RP11
V3
U15
U16
U17
U18
C36
C37
C38
C39
C40
V4
RP12
U19
R6
U20
U21
U22
U23
U24
RP13
U25
C41
C42
C43
C44
C45
C46
C47
V5
V6
1
55


IOX
35 IOEXP
1,3,13,14,15
2,4
U14
XX85
BA9
33 IORQ*
U22
28 A9
30 A8
15 A7
17 A6
19 A5
21 A4
23 A3
25 A2
BA8
U21
XX688
RP11 RP12 RP11 RP12
V5
V3
V4
BA9
BA8
BDSEL*
32 RD*
BRD*
U16
XX138
RD3*
RD2*
RD1*
RD0*
U15
XX138
WR3*
WR2*
WR1*
WR0*
27 A1
29 A0
31 WR*
47 SYSRST*
BA1
BA0
BRST*
R4
R3
R2
D1
D2
D3
"M0"
"M1"
"M2"
U13
M0OUT
M1OUT
M2OUT
RP4
U18
ICL*
U19
XX74
R6
C40
52 PCI
51 PCO
U20
XX245
D0
D1
D2
D3
D4
D5
D6
D7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD0 – BD7
RP13
M0EN*
M0IN*
U25
XX74
XX04
U17
RD3*
V6
IRQ*
J2
M1EN*
M1IN*
M2EN*
M2IN*
M3EN*
M3IN*
RP12
1,2 +5
C47
3,4 GND
C1–C5, C31–C39,
C41–C46
IRQ*
INTRQ*
44


BD0 – BD7
M0EN*
M1EN*
M2EN*
M3EN*
M0OUT
M1OUT 1,2
M2OUT 12,13
9,10
V1
U6
U5
U4
U3
U2
U1
BRST*
M0IN*
M7IN*
M8IN*
M15IN*
M16IN*
M23IN*
U12 XX240
U11 XX273
U10 XX240
U9 XX273
U8 XX240
U7 XX273
RD2*
WR2*
RD1*
WR1*
RD0*
WR0*
M0IN* – M3IN*
J1/J3
MOD0*
MOD1*
MOD2*
MOD3*
MOD4*
MOD5*
MOD6*
MOD7*
MOD8*
MOD9*
MOD10*
MOD11*
MOD12*
MOD13*
MOD14*
MOD15*
MOD16*
MOD17*
MOD18*
MOD19*
MOD20*
MOD21*
MOD22*
MOD23*
ALL EVEN PINS
RACK POWER
U19 XX74
WR3*
R5
R1
"PWR"
D4
Q1
V2
C6

**VL-7507 (REV 0) PARTS LIST**
General Purpose 24-Line I/O Board

**Capacitors**

| | |
|---|---|
| C1-C5, C7-C39, C41-C46 | .01 uf ceramic |
| C6 | 1 uf tantalum |
| C40 | 22 pf ceramic |
| C47 | 22 uf electrolytic, radial |

**Integrated Circuits**

| | |
|---|---|
| U1-U6, U13, U24 | 74LS38 |
| U7, U9, U11 | 74LS273 |
| U8, U10, U12 | 74LS240 |
| U14 | 74LS85 |
| U15, U16 | 74LS138 |
| U17 | 74LS125 |
| U18 | 74LS04 |
| U19 | 74HCT74 |
| U20 | 74LS245 |
| U21 | 74HCT688 |
| U22 | 74LS244 |
| U23, U25 | 74LS74 |

**Resistors**

| | |
|---|---|
| R1-R4 | 330 ohm, 5%, 1/4W |
| R5 | 270 ohm, 5%, 1/4W |
| R6 | 3K3 ohm, 5%, 1/4W |
| RP1-RP4 | 1K ohm, 7 resistor SIP |
| RP5-RP10 | 1K ohm, 4 resistor SIP |
| RP11-RP13 | 10K ohm, 7 resistor SIP |

**Semiconductors**

| | |
|---|---|
| D1-D4 | T1 LED |
| Q1 | TIP32A transistor |

**Miscellaneous**

| | |
|---|---|
| J2 | 8 pin R/A header |
| J3 (optional) | 50 pin R/A header |

VL-75CT07 (REV 0.01) PARTS LIST
General Purpose 24-Line I/O Board (Extended Temperature Version)

Capacitors

| | |
|---|---|
| C1-C5, C7-C39, C41-C46 | .01 uf ceramic |
| C6 | 1 uf tantalum |
| C40 | 22 pf ceramic |
| C47 | 22 uf electrolytic, radial |

Integrated Circuits

| | |
|---|---|
| U1-U6 | 54LS38 |
| U7, U9, U11 | 74HCT273 |
| U8, U10, U12 | 74ACT240 |
| U13, U24 | 74LS38 |
| U14 | 74HCT85 |
| U15, U16 | 74HCT138 |
| U17 | 74HCT125 |
| U18 | 74HCT04 |
| U19, U23, U25 | 74HCT74 |
| U20 | 74ACT245 |
| U21 | 74HCT688 |
| U22 | 74ACT244 |

Resistors

| | |
|---|---|
| R1-R4 | 470 ohm, 5%, 1/4W |
| R5 | 270 ohm, 5%, 1/4W |
| R6 | 27K ohm, 5%, 1/4W |
| RP1-RP4, RP13 | 10K ohm, 7 resistor SIP |
| RP5-RP10 | 1K ohm, 4 resistor SIP |
| RP11, RP12 | 100K ohm, 7 resistor SIP |

Semiconductors

| | |
|---|---|
| D1-D4 | T1 LED |
| Q1 | TIP32A transistor |

Miscellaneous

| | |
|---|---|
| J2 | 8 pin R/A header |
| J3 (optional) | 5Ø pin R/A header |

**STD BUS PINOUT**

Connections from the VL-7507 board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7507.

| COMPONENT SIDE | | | | SOLDER SIDE | | | |
|---|---|---|---|---|---|---|---|
| **PIN** | **SIGNAL** | **FLOW** | **DESCRIPTION** | **PIN** | **SIGNAL** | **FLOW** | **DESCRIPTION** |
| 1 | +5V | In | +5 volt power | 2 | +5V | In | +5 volt power |
| 3 | GND | In | Digital ground | 4 | GND | In | Digital ground |
| 5 | VBB/VBAT | - | -5V or bat. backup | 6 | -5V | - | -5V power |
| 7 | D3/A19 | I/O | Data bus | 8 | D7 | I/O | Data bus |
| 9 | D2/A18 | I/O | Data bus | 10 | D6 | I/O | Data bus |
| 11 | D1/A17 | I/O | Data bus | 12 | D5/A21 | I/O | Data bus |
| 13 | D0/A16 | I/O | Data bus | 14 | D4/A20 | I/O | Data bus |
| 15 | A7 | In | Address bus | 16 | A15 | - | Address bus |
| 17 | A6 | In | Address bus | 18 | A14 | - | Address bus |
| 19 | A5 | In | Address bus | 20 | A13 | - | Address bus |
| 21 | A4 | In | Address bus | 22 | A12 | - | Address bus |
| 23 | A3 | In | Address bus | 24 | A11 | - | Address bus |
| 25 | A2 | In | Address bus | 26 | A10 | - | Address bus |
| 27 | A1 | In | Address bus | 28 | A9 | In | Address bus |
| 29 | A0 | In | Address bus | 30 | A8 | In | Address bus |
| 31 | WR* | In | Write strobe | 32 | RD* | In | Read strobe |
| 33 | IORQ* | In | I/O addr. select | 34 | MEMRQ* | - | Memory addr. select |
| 35 | IOEXP* | In | I/O expansion | 36 | MEMEX* | - | Memory expansion |
| 37 | REFRESH* | - | Refresh timing | 38 | MCSYNC* | - | Machine cycle sync. |
| 39 | STATUS1* | - | CPU status | 40 | STATUS0* | - | CPU status |
| 41 | BUSAK* | - | Bus acknowledge | 42 | BUSRQ* | - | Bus request |
| 43 | INTAK* | - | Interrupt acknowl. | 44 | INTRQ* | Out | Interrupt request |
| 45 | WAITRQ* | - | Wait request | 46 | NMIRQ* | - | Non-maskable interrupt |
| 47 | SYSRESET* | In | System reset | 48 | PBRESET* | - | Push button reset |
| 49 | CLOCK* | - | CPU clock | 50 | CNTRL* | - | AUX timing |
| 51 | PCO | Out | Priority chain out | 52 | PCI | In | Priority chain in |
| 53 | AUXGND | - | ±12 volt ground | 54 | AUXGND | - | ±12 volt ground |
| 55 | AUX+V | - | +12 volt input | 56 | AUX-V | - | -12 volt input |

Notes:
* Denotes an active low signal.

**DECIMAL / HEX / ASCII CONVERSION CHART**

The chart below is useful for both ASCII and decimal/hex conversion. The "^" symbol denotes control characters. "^A" represents control A, etc.

| Dec. | Hex | ASCII | Dec. | Hex | ASCII | Dec. | Hex | ASCII | Dec. | Hex | ASCII |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 00 | NUL | 32 | 20 | | 64 | 40 | @ | 96 | 60 | ` |
| 1 | 01 | ^A SOH | 33 | 21 | ! | 65 | 41 | A | 97 | 61 | a |
| 2 | 02 | ^B STX | 34 | 22 | " | 66 | 42 | B | 98 | 62 | b |
| 3 | 03 | ^C ETX | 35 | 23 | # | 67 | 43 | C | 99 | 63 | c |
| 4 | 04 | ^D EOT | 36 | 24 | $ | 68 | 44 | D | 100 | 64 | d |
| 5 | 05 | ^E ENQ | 37 | 25 | % | 69 | 45 | E | 101 | 65 | e |
| 6 | 06 | ^F ACK | 38 | 26 | & | 70 | 46 | F | 102 | 66 | f |
| 7 | 07 | ^G BEL | 39 | 27 | ' | 71 | 47 | G | 103 | 67 | g |
| 8 | 08 | ^H BS | 40 | 28 | ( | 72 | 48 | H | 104 | 68 | h |
| 9 | 09 | ^I HT | 41 | 29 | ) | 73 | 49 | I | 105 | 69 | i |
| 10 | 0A | ^J LF | 42 | 2A | * | 74 | 4A | J | 106 | 6A | j |
| 11 | 0B | ^K VT | 43 | 2B | + | 75 | 4B | K | 107 | 6B | k |
| 12 | 0C | ^L FF | 44 | 2C | , | 76 | 4C | L | 108 | 6C | l |
| 13 | 0D | ^M CR | 45 | 2D | - | 77 | 4D | M | 109 | 6D | m |
| 14 | 0E | ^N SO | 46 | 2E | . | 78 | 4E | N | 110 | 6E | n |
| 15 | 0F | ^O SI | 47 | 2F | / | 79 | 4F | O | 111 | 6F | o |
| 16 | 10 | ^P DLE | 48 | 30 | 0 | 80 | 50 | P | 112 | 70 | p |
| 17 | 11 | ^Q DC1 | 49 | 31 | 1 | 81 | 51 | Q | 113 | 71 | q |
| 18 | 12 | ^R DC2 | 50 | 32 | 2 | 82 | 52 | R | 114 | 72 | r |
| 19 | 13 | ^S DC3 | 51 | 33 | 3 | 83 | 53 | S | 115 | 73 | s |
| 20 | 14 | ^T DC4 | 52 | 34 | 4 | 84 | 54 | T | 116 | 74 | t |
| 21 | 15 | ^U NAK | 53 | 35 | 5 | 85 | 55 | U | 117 | 75 | u |
| 22 | 16 | ^V SYN | 54 | 36 | 6 | 86 | 56 | V | 118 | 76 | v |
| 23 | 17 | ^W ETB | 55 | 37 | 7 | 87 | 57 | W | 119 | 77 | w |
| 24 | 18 | ^X CAN | 56 | 38 | 8 | 88 | 58 | X | 120 | 78 | x |
| 25 | 19 | ^Y EM | 57 | 39 | 9 | 89 | 59 | Y | 121 | 79 | y |
| 26 | 1A | ^Z SUB | 58 | 3A | : | 90 | 5A | Z | 122 | 7A | z |
| 27 | 1B | ESC | 59 | 3B | ; | 91 | 5B | [ | 123 | 7B | { |
| 28 | 1C | FS | 60 | 3C | < | 92 | 5C | \ | 124 | 7C | \| |
| 29 | 1D | GS | 61 | 3D | = | 93 | 5D | ] | 125 | 7D | } |
| 30 | 1E | RS | 62 | 3E | > | 94 | 5E | ^ | 126 | 7E | ~ |
| 31 | 1F | US | 63 | 3F | ? | 95 | 5F | _ | 127 | 7F | DEL |