Reference Manual

VL-7304a
VL-7304b
VL-73CT04a

Dual Serial Interface
Card for the STD Bus

STD

VERSALOGIC CORPORATION

VL-7304a
VL-7304b
VL-73CT04a

Dual Serial Interface
Card for the STD Bus

Model VL-7304a, VL-7304b & VL-73CT04a

Dual Serial Interface Card for the STD Bus

REFERENCE MANUAL

VL-7304a Rev. 0.00
VL-7304b Rev. 0.00
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M7304

Model VL-7304
Dual Serial Interface Card

REFERENCE MANUAL

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Section 1
OVERVIEW

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7304 interface card. This card provides two serial I/O channels. Versions with RS-232C and RS-422/485 interfaces are available.

The VL-7304 is available in standard (TTL) and extended temperature (VL-73CT04) STD Bus versions. Versions are available with two RS-232C channels (VL-7304a, VL-73CT04a) or with one RS-232/RS-422 and one RS-422 channel (VL-7304). Throughout this manual "VL-7304" will be used to refer to all versions of the board, unless specifically noted otherwise.

OVERVIEW

The VL-7304 card provides two independent serial I/O channels with either RS-232C or RS-422/485 type interfaces. It operates in both asynchronous and synchronous serial modes.

Two independent 8251A type serial controller chips can be programmed for common communications formats. Programmable functions include 5, 6, 7, or 8 bits per character; 1, 1.5, or 2 stop bits; and even, odd, or no parity bit.

A programmable baud rate generator allows independent software selection of the baud rate for each channel. Baud rates of 75, 150, 300, 600, 1200, 2400, 4800, 9600, and 19,200 can be software selected without jumper or hardware changes.

In synchronous mode, baud rates from 1200 to 38.4K baud are software selectable. Clock input/output lines are provided on the serial I/O connectors for both RS-232C and RS-422/485 synchronous operation.

Each serial channel can be operated in polled or interrupt mode. For interrupt operation two modes are available. Polled (non-vectored) interrupts are supported, as well as externally prioritized interrupts using the interrupt output connector.

Standard RS-232C interfaces on each channel allow easy interfacing with standard communication devices. On-board jumpers allow each channel to be configured for DTE or DCE pinouts.

The VL-7304b version provides dual serial capabilities with one RS-422 channel and one jumper selectable RS-232C/RS-422 channel. RS-422 transmission allows high speed (to 38.4K baud), long run (to 4000 feet), high noise immunity communication. The VL-7304b can be used to upgrade existing designs using 8251A type serial boards with little change to existing software.

The RS-422 channels (on the VL-7304b) can also be jumper configured for RS-485 multidrop operation. RS-485 operation uses a single cable (with one or two twisted wire pairs) to connect up to 32 devices on a high speed serial link.

For RS-232 channels the latching 26-pin header connectors are plug compatible with standard DB-25 type connectors using mass terminated cables. RS-422 channels are connected through latching 10-pin headers.

The VL-7304 includes both 8 and 10-bit addressing, and is compatible with all common STD Bus processor types. The IOEXP line is also supported. The board occupies 8 consecutive I/O locations.

The board is compatible with the Pro-Log 7304 card, except for the TTY interface which is not available on the VL-7304.

FEATURES

- Two RS-232C serial ports.
- Optional RS-422 ports (VL-7304b).
- 75 to 19.2K baud asynchronous operation.
- 1200 to 38.4K baud synchronous operation.
- DTE / DCE jumper selectable pinout.
- Polled and externally prioritized interrupts.
- 8251A type serial chip.
- Latching I/O connectors.
- Extended temperature version available.
- Universal STD Bus processor compatible.
- Pro-Log 7304 plug-in replacement (except TTY interface).

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications

Storage Temperature:
- VL-7304: -40° to +75° C
- VL-73CT04: -40° to +85° C

Free Air Operating Temperature:
- VL-7304: 0° to +65° C
- VL-73CT04: -40° to +85° C

Power Requirements:
- VL-7304a: 5V ±5% @ 290 ma typ.
  ±12V ±10% @ 35 ma typ.
- VL-7304b: 5V ±5% @ 460 ma typ.
  ±12V ±10% @ 18 ma typ. (if RS-232C used)
- VL-73CT04a: 5V ±10% @ 28 ma typ.
  ±12V ±10% @ 8 ma typ.

Section 2
VL-7304a CONFIGURATION

INTRODUCTION

The VL-7304 is available in "a" and "b" versions depending on the type of interface required. Since these versions differ considerably, both in the chips and the jumper options that are present on the board, the configuration of each board is detailed in a separate section.

This section discusses only the "a" version of the board (dual RS-232C ports). See Section 3 for configuration information on the "b" version of the board (RS-422 and RS-232/RS-422 ports).

Note: The board version can be easily identified by the number of connectors on the board edge. The "a" version has two 26-pin connectors; the "b" version has three connectors (one 26-pin and two 10-pin).

JUMPER SUMMARY

Various options available on the VL-7304a card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 2-1 shows the jumper block locations on the VL-7304a board. It indicates the position of the jumper plugs as shipped from the factory. The function of each jumper block is detailed in Figure 2-2.

Note: There are a number of permanently installed wire jumpers on the VL-7304 board. These are used in the production of the "a" and "b" versions of the board and are not additional user options.

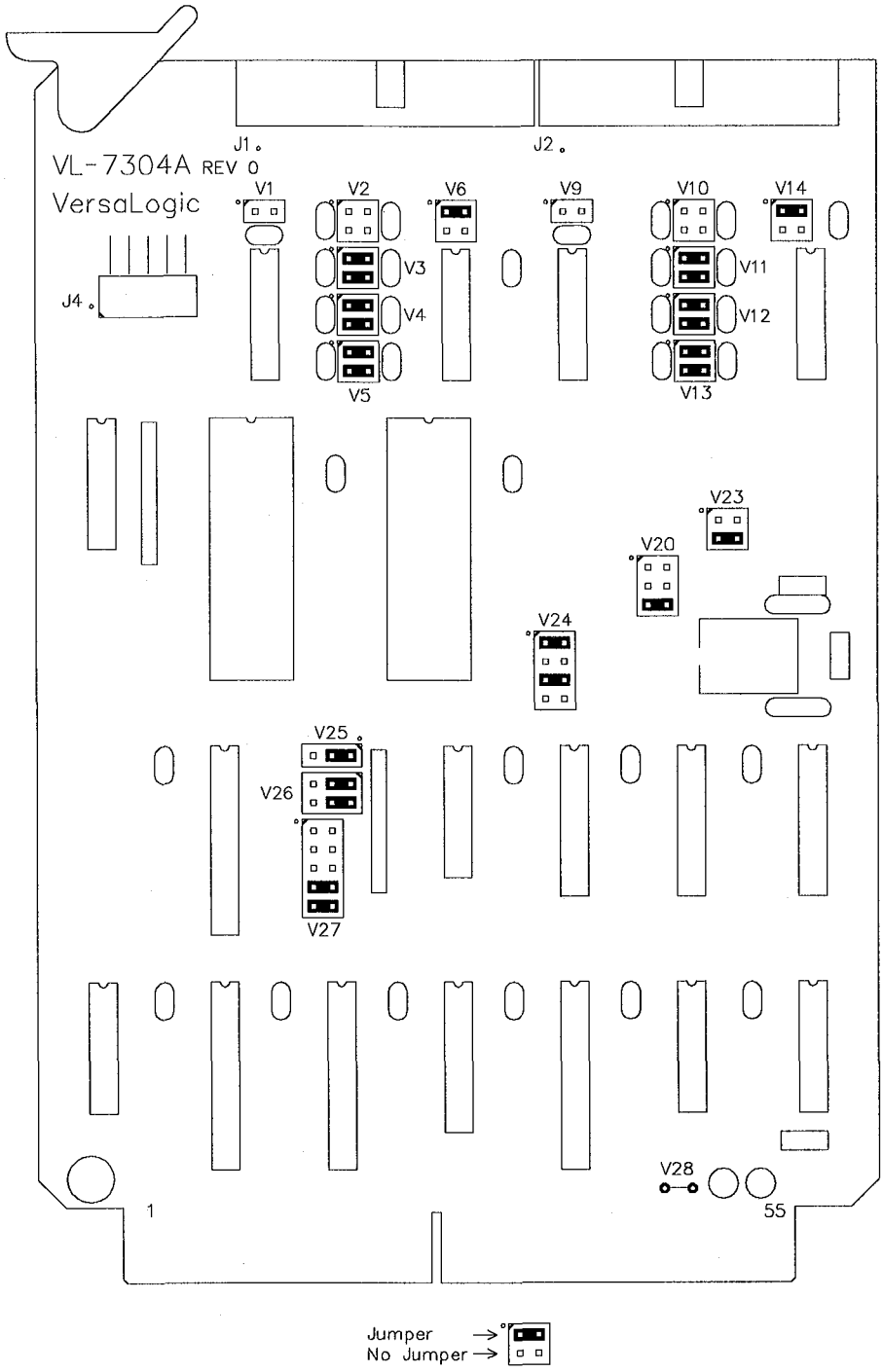


Figure 2-1. VL-7304a Jumper Block Locations

Jumper Block	Description	As Shipped
V1-V5	Channel A DCE/DTE options. See Connector Pinouts.	
V6	Channel A ready input.	
	a - CTS from external input.	a - IN
	b - CTS held always ready.	b - out
V7-V8	Not used.	
V9-V13	Channel B DCE/DTE options. See Connector Pinouts.	
V14	Channel B ready input.	
	a - CTS from external input.	a - IN
	b - CTS held always ready.	b - out
V15-V19	Not used.	
V20	Channel A receive baud rate source.	
	a - From external input.	a - out
	b - Not used.	b - out
	c - From baud rate generator.	c - IN
V21-V22	Not used.	
V23	Channel B receive baud rate source.	
	a - From external input.	a - out
	b - From baud rate generator.	b - IN
V24	Baud rate generator options. See Baud Rates.	
V25	IOEXP select. See Board Address.	Ignore IOEXP
	a - Don't Care.	a - IN
	b - Active low.	b - out
	- - Active high (no jumpers).	
V26	Address mode selector. See Board Address.	
	a - A9 control.	a - ignore A9
	b - A8 control.	b - ignore A8
V27	Board Address. See Board Address.	Hex E0
V28	Digital Ground (+5V) to AUX GND (±12V).	IN

Figure 2-2. VL-7304a Jumper Functions

BOARD ADDRESS

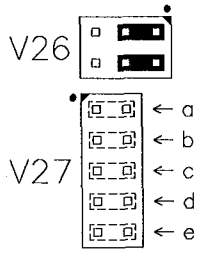
The VL-7304 supports both 8 and 10-bit I/O addressing. 8-bit addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10-bit addressing can be used with 16-bit processors (i.e. 8088) to decode up to 1024 I/O port addresses.

Both 8 and 10-bit addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7304.

As shipped the board is configured for 8-bit addressing with a board address of hex E0. The VL-7304 normally occupies eight consecutive I/O addresses (i.e. E0-E7). If it is configured as four input ports and four output ports it can optionally be mapped into only four I/O ports.

8-Bit Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e. "3" and "0" = hex address 30).



---- V27 ----				Upper
a	b	c	d	Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

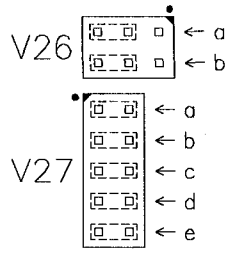
V27	Lower
e	Digit
X	0
-	8

X = Jumper installed
- = Jumper removed

Figure 2-3. 8-Bit Address Jumpers

10-Bit Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e. "1" and "3" and "0" = hex address 130).



V26 a	V26 b	Upper Digit	V27 a	V27 b	V27 c	V27 d	Middle Digit	V27 e	Lower Digit
X	X	0	X	X	X	X	0	X	0
X	-	1	X	X	X	-	1	-	8
-	X	2	X	X	-	X	2		
-	-	3	X	X	-	-	3		
			X	-	X	X	4		
			X	-	X	-	5		
			X	-	-	X	6		
			X	-	-	-	7		
			-	X	X	X	8		
			-	X	X	-	9		
			-	X	-	X	A		
			-	X	-	-	B		
			-	-	X	X	C		
			-	-	X	-	D		
			-	-	-	X	E		
			-	-	-	-	F		

X = Jumper installed
- = Jumper removed

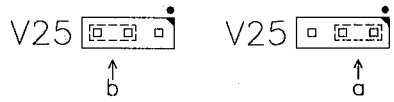
Figure 2-4. 10-Bit Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown in Figure 2-5.



Jumper Block	Description	As Shipped
V25	a - Ignore IOEXP (enable high or low).	a - IN
	b - Enable on IOEXP low.	b - out
	None - Enable on IOEXP high (no jumpers).	

Figure 2-5. IOEXP Jumper

BAUD RATES

The baud rate at which each channel operates is subject to several software controls and one hardware jumper. These are covered in detail in the Operation section. The jumper option that effects baud rates is shown below.

Baud Rate Table

Baud rates are selected by software commands. A clock division factor (either 16 or 64 for async., or 1 for sync.) is programmed into the serial controller chip. Then a baud rate is selected by number (0-7) from the appropriate table below.

A jumper option allows the use of Baud Rate Table 1 or 2. As shipped Table 1 is selected. Table 2 is included only for compatibility with older systems and should not be used for new designs.

Software Select#	(As shipped) Table 1	Table 2
0	2400	2400
1	600	600
2	300	300
3	1200	1200
4	19200	19200
5	2400	2400
6	4800	19200
7	9600	19200

Figure 2-6. 16X Async. Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	600	600
1	150	150
2	75	75
3	300	300
4	4800	4800
5	600	600
6	1200	4800
7	2400	4800

Figure 2-7. 64X Async. Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	38400	38400
1	9600	9600
2	4800	4800
3	19200	19200
4	N/A*	N/A*
5	38400	38400
6	N/A*	N/A*
7	N/A*	N/A*

* Not available. Higher than the 60K baud limit of the serial chip (76.8K baud).

Figure 2-8. Sync. Mode Baud Rate Options

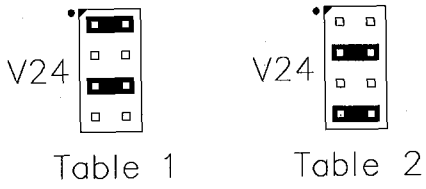
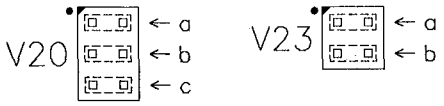


Figure 2-9. Baud Rate Table Jumper

Baud Rate Clock Inputs

The baud rate clock input for receiving data on each channel can be connected to the on-board baud rate generator, or to the I/O connector (for external input of the baud rate). The external baud rate option is primarily applicable to synchronous operation.

The transmit clock inputs for both channels are permanently connected to the on-board baud rate generator.



Jumper Block	Description	As Shipped
V20	Channel A receive baud rate source.	
	a - From external input.	a - out
	b - Not used.	b - out
	c - From baud rate generator.	c - IN
V23	Channel B receive baud rate source.	
	a - From external input.	a - out
	b - From baud rate generator.	b - IN

Figure 2-10. Baud Rate Clock Jumpers

CONNECTOR PINOUTS

As shipped, the RS-232 interfaces are jumpered as data communications equipment (DCE) for connection to a video terminal or printer. They can also be jumpered as data terminal equipment (DTE) for connection to another computer.

The jumper blocks that control the RS-232 port configuration are shown below. Two standard configurations are shown along with the resulting RS-232 signal connections. Note that with either of these configurations, RS-232 pin 17 (TCLK) can also be connected to RS-232 pin 15 using jumper V3. For special applications jumpering refer to the VL-7304a schematic.

Note: The pin numbers included below are at the RS-232 (DB-25) connector as connected to the board with a standard interface cable (VersaLogic #9560 or similar). These are NOT identical to the pin numbers at the J1 or J2 connectors. See External Connections in the Installation section

for complete pinout information.

VL-7304a Signal		DCE (to Terminal) External RS-232 Device (Pin#)	DTE (to Computer) External RS-232 Device (Pin#)
TXD (Xmit. Data)	---->	RD(3)	TD(2)
RXD (Recv. Data)	<----	TD(2)	RD(3)
RTS (Recv. Handshake)	---->	CTS(5)	RTS(4)
CTS (Xmit. Handshake)	<----	RTS(4)	CTS(5)
DTR (Xmit. Eqpt. Stat.)	---->	DSR(6)	DTR(20)
DCD (Recv. Eqpt. Stat.)	<----	DTR(20)	DSR(6)
TCLK (Xmit. Clock)	---->	TCLK(24)	RCLK(17/15)
RCLK (Recv. Clock)	<----	RCLK(17/15)	TCLK(24)

Jumper Setting for Channel A	Channel B	DCE (to Terminal)	DTE (to Computer)
V5	V13		
V4	V12		
V3	V11		
V2	V10		

Figure 2-11. RS-232 Port Pinout Jumpers

READY LINE (CTS)

The 8251A serial chip requires that the CTS (Clear To Send) input signal be true (high) for transmitting to occur. Connection of this line to the external device is usually desirable as it allows the device to halt the flow of transmitted data when it is not ready to receive it.

In some applications, such as where the external device does not provide a ready signal to connect to CTS, the VL-7304a can be jumpered to hold the CTS signal always ready. This allows the board to transmit data even if the external device does not provide a ready signal.

Jumper Block	Description	As Shipped
V6	Channel A ready option. a - CTS from external input. b - CTS held always ready.	 a - IN b - out
V14	Channel B ready option. a - CTS from external input. b - CTS held always ready.	 a - IN b - out

Figure 2-12. CTS Ready Jumpers

GROUND OPTION

Jumper V28 connects the system digital (+5V) ground line to the "auxiliary" ($\pm$12V) ground line. Although the $\pm$12V power supply ground may need to be independent from the +5V supply when it is connected to an analog I/O board, it must be grounded in common when used to power the RS-232C ports on the VL-7304 board. It is recommended that these grounds also be connected together at the power supply or motherboard connection.

This jumper is IN when shipped. It should not be removed for proper operation of the VL-7304a.

Section 3
VL-7304b CONFIGURATION

INTRODUCTION

The VL-7304 is available in "a" and "b" versions depending on the type of interface required. Since these versions differ considerably, the configuration of each board is detailed in a separate section.

This section discusses only the "b" version of the board (one RS-422 and one RS-232/RS-422 port). See Section 2 for configuration information on the "a" version of the board (dual RS-232C ports).

Note: The boards can be identified by the number of connectors on the board edge. The "a" version has two 26-pin connectors; the "b" version has three connectors (one 26-pin and two 10-pin).

JUMPER SUMMARY

Various options available on the VL-7304b card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 3-1 shows the jumper block locations on the VL-7304b board. It indicates the position of the jumper plugs as shipped from the factory. The function of each jumper block is detailed in Figure 3-2.

Note: There are a number of permanently installed wire jumpers on the VL-7304 board. These are used in the production of the "a" and "b" versions of the board and are not additional user options.

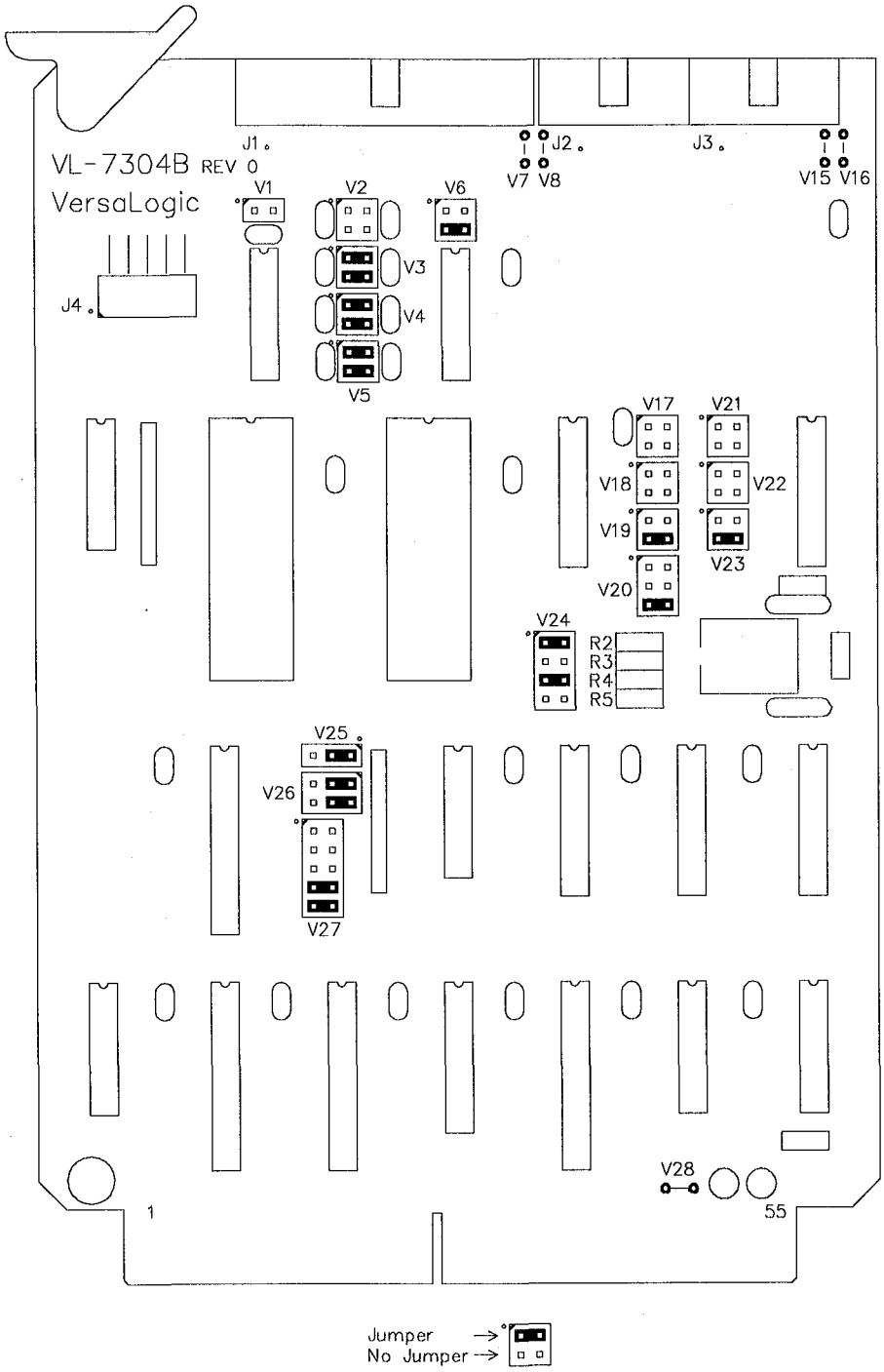


Figure 3-1. VL-7304b Jumper Block Locations

Jumper Block	Description	As Shipped
V1-V5	Channel A DCE/DTE Options. See Connector Pinouts.	
V6	Channel A ready input.	
	a - CTS from external input.	a - out
	b - CTS held always ready.	b - IN
V7-V16	Not used.	
V17-V18	Channel A RS-422 or RS-485 select.	RS-422 mode
V19	Channel A interface select.	
	a - RS-232 interface	a - out
	b - RS-422/485 interface	b - IN
V20	Channel A receive baud rate source.	
	a - From connector J1 (RS-232).	a - out
	b - From connector J2 (RS-422/485).	b - out
	c - From baud rate generator.	c - IN
V21-V22	Channel B RS-422 or RS-485 select.	RS-422 mode
V23	Channel B receive baud rate source.	
	a - From external input.	a - out
	b - From baud rate generator.	b - IN
V24	Baud rate generator options. See Baud Rates.	
V25	IOEXP select. See Board Address.	Ignore IOEXP
	a - Don't Care.	a - IN
	b - Active low.	b - out
	- - Active high (no jumpers).	
V26	Address mode selector. See Board Address.	
	a - A9 control.	a - ignore A9
	b - A8 control.	b - ignore A8
V27	Board Address. See Board Address.	Hex E0
V28	Digital Ground (+5V) to AUX GND (±12V).	IN

Figure 3-2. VL-7304b Jumper Functions

BOARD ADDRESS

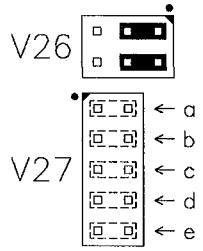
The VL-7304 supports both 8 and 10-bit I/O addressing. 8-bit addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10-bit addressing can be used with 16-bit processors (i.e. 8088) to decode up to 1024 I/O port addresses.

Both 8 and 10-bit addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7304.

As shipped the board is configured for 8-bit addressing with a board address of hex E0. The VL-7304 normally occupies eight consecutive I/O addresses (i.e. E0-E7). If it is configured as four input ports and four output ports it can optionally be mapped into only four I/O ports.

8-Bit Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e. "3" and "0" = hex address 30).



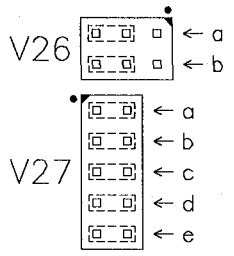
---- V27 ----				Upper	V27	Lower
a	b	c	d	Digit	e	Digit
X	X	X	X	0	X	0
X	X	X	-	1	-	8
X	X	-	X	2		
X	X	-	-	3		
X	-	X	X	4		
X	-	X	-	5		
X	-	-	X	6		
X	-	-	-	7		
-	X	X	X	8		
-	X	X	-	9		
-	X	-	X	A		
-	X	-	-	B		
-	-	X	X	C		
-	-	X	-	D		
-	-	-	X	E		
-	-	-	-	F		

X = Jumper installed
- = Jumper removed

Figure 3-3. 8-Bit Address Jumpers

10-Bit Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e. "1" and "3" and "0" = hex address 130).



V26 a	V26 b	Upper Digit
X	X	0
X	-	1
-	X	2
-	-	3

---- V27 ---- a	b	c	d	Middle Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

V27 e	Lower Digit
X	0
-	8

X = Jumper installed
- = Jumper removed

Figure 3-4. 10-Bit Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown in Figure 3-5.

Jumper Block	Description	As Shipped
V25	a - Ignore IOEXP (enable high or low).	a - IN
	b - Enable on IOEXP low.	b - out
	None - Enable on IOEXP high (no jumpers).	

Figure 3-5. IOEXP Jumper

BAUD RATES

The baud rate at which each channel operates is subject to several software controls and one hardware jumper. These are covered in detail in the Operation section. The jumper option that effects baud rates is shown below.

Baud Rate Table

Baud rates are selected by software commands. A clock division factor (either 16 or 64 for async., or 1 for sync.) is programmed into the serial controller chip. Then a baud rate is selected by number (0-7) from the appropriate table below.

A jumper option allows the use of Baud Rate Table 1 or 2. As shipped Table 1 is selected. Table 2 is included only for compatibility with older systems and should not be used for new designs.

Software Select#	(As shipped) Table 1	Table 2
0	2400	2400
1	600	600
2	300	300
3	1200	1200
4	19200	19200
5	2400	2400
6	4800	19200
7	9600	19200

Figure 3-6. 16X Async. Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	600	600
1	150	150
2	75	75
3	300	300
4	4800	4800
5	600	600
6	1200	4800
7	2400	4800

Figure 3-7. 64X Async. Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	38400	38400
1	9600	9600
2	4800	4800
3	19200	19200
4	N/A*	N/A*
5	38400	38400
6	N/A*	N/A*
7	N/A*	N/A*

* Not available. Higher than the 60K baud limit of the serial chip (76.8K baud).

Figure 3-8. Sync. Mode Baud Rate Options

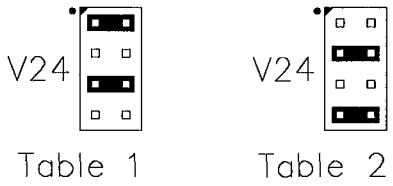
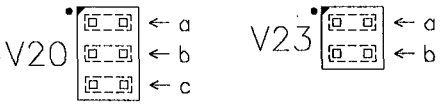


Figure 3-9. Baud Rate Table Jumper

Baud Rate Clock Inputs

The baud rate clock input for receiving data on each channel can be connected to the on-board baud rate generator, or to the I/O connector (for external input of the baud rate). The external baud rate option is primarily applicable to synchronous operation.

The transmitter clock inputs for both channels are permanently connected to the on-board baud rate generator.



Jumper Block	Description	As Shipped
V20	Channel A receive baud rate source.	
	a - From connector J1 (RS-232).	a - out
	b - From connector J2 (RS-422/485).	b - out
	c - From baud rate generator.	c - IN
V23	Channel B receive baud rate source.	
	a - From external input.	a - out
	b - From baud rate generator.	b - IN

Figure 3-10. Baud Rate Clock Jumper

CHANNEL A INTERFACE SELECTION

Channel A on the VL-7304b can be configured with either an RS-232C or an RS-422/485 interface. As shipped it is jumpered for the RS-244/485 interface. The selection is made using jumpers V6 and V19 as shown below.

Jumper Block	Description	As Shipped
V6	Channel A ready input.	
	a - CTS from external input (RS-232).	a - out
	b - CTS held always ready (RS-244).	b - IN
V19	Channel A interface select.	
	a - RS-232 interface.	a - out
	b - RS-422/485 interface.	b - IN

Figure 3-11. Channel A Interface Selection

RS-232 CONFIGURATION

When the RS-232 interface is used on Channel A, the following jumper options are available.

Connector Pinout

When the RS-232 interface is used on Channel A, it can be jumpered for several different pinout configurations. As shipped, it is jumpered as data communications equipment (DCE) for connection to a video terminal or printer. It can also be jumpered as data terminal equipment (DTE) for connection to another computer.

The jumper blocks that control the RS-232 port configuration are shown below. Two standard configurations are shown along with the resulting RS-232 signal connections. Note that with either of these configurations, RS-232 pin 17 (TCLK) can also be connected to RS-232 pin 15 using jumper V3. For special applications jumpering refer to the VL-7304b schematic.

Note: The pin numbers included below are at the RS-232 (DB-25) connector as connected to the board with a standard interface cable (VersaLogic #9560 or similar). These are NOT the pin numbers at the J1 connector.

See External Connections in section 4 for complete pinout information.

VL-7304b Signal		DCE (to Terminal) External RS-232 Device (Pin#)	DTE (to Computer) External RS-232 Device (Pin#)
TXD (Xmit. Data)	---->	RD(3)	TD(2)
RXD (Recv. Data)	<----	TD(2)	RD(3)
RTS (Recv. Handshake)	---->	CTS(5)	RTS(4)
CTS (Xmit. Handshake)	<----	RTS(4)	CTS(5)
DTR (Xmit. Eqpt. Stat.)	---->	DSR(6)	DTR(20)
DCD (Recv. Eqpt. Stat.)	<----	DTR(20)	DSR(6)
TCLK (Xmit. Clock)	---->	TCLK(24)	RCLK(17/15)
RCLK (Recv. Clock)	<----	RCLK(17/15)	TCLK(24)

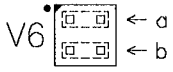
Jumper Setting for the Mode Shown	DCE (to Terminal)	DTE (to Computer)
V5		
V4		
V3		
V2		

Figure 3-12. RS-232 Port Pinout Jumpers

Ready Line (CTS)

The 8251A serial chip requires that the CTS (Clear To Send) input signal be true (high) for transmitting to occur. Connection of this line to an external RS-232 device is usually desirable as it allows the device to halt the flow of transmitted data when it is not ready to receive it. RS-422 interfaces do not use hardware handshaking (the CTS line).

In some applications, such as where the external RS-232 device does not provide a ready signal to connect to CTS, or when channel A is jumpered for RS-422 operation, the VL-7304b should be jumpered to hold the CTS signal always ready. This allows the board to transmit data without a ready signal being available from the external device.



Jumper Block	Description	As Shipped
V6	Channel A ready input.	
	a - CTS from external input (RS-232).	a - out
	b - CTS held always ready (RS-232 or 244).	b - IN

Figure 3-13. CTS Ready Input

RS-422 PORTS

The RS-422 high speed serial ports allow data to be dependably transmitted over long distances (to 4000 feet) using twisted pair wire. There are no jumper options associated with the RS-422 interfaces except for converting them to RS-485 multidrop operation as noted below.

Refer to the Operation section for more information on the connection and operation of the RS-422 ports.

RS-485 MULTIDROP

Using the jumpers shown in Figure 3-14 the RS-422 ports can be configured for RS-485 multidrop operation. This allows up to 32 driver/receivers to be connected to a single communications line. When the VL-7304b is used in multidrop applications, the 100 ohm terminating resistors should be removed from all stations except for the two farthest line locations (i.e. the start and end of the line).

Refer to the Operation section for information on connection and operation of the RS-485 interfaces.

Channel	Multidrop Jumpers*	Terminators
A	V17a, V17b, V18a, V18b	R2, R3
B	V21a, V21b, V22a, V22b	R4, R5

* The jumpers listed for each channel should be IN for RS-485 multidrop operation and OUT for RS-422 operation.

Figure 3-14. Multidrop (RS-485) Mode Jumpers

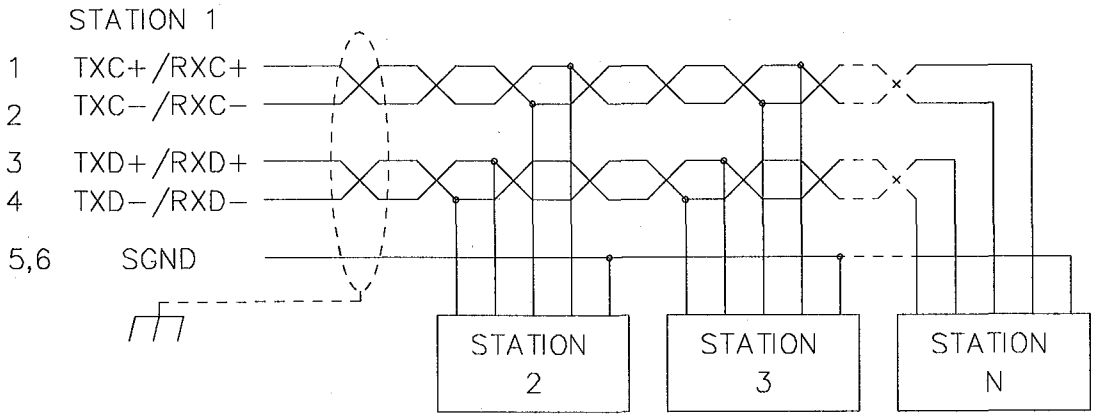


Figure 3-15. Typical Multidrop (RS-485) Connection

POWER SUPPLY GROUNDS

Jumper V28 connects the system digital (+5V) ground line to the "auxiliary" (±12V) ground line. Although the ±12V power supply ground may need to be independent from the +5V supply when it is used to power an analog I/O board, it must be grounded in common if the RS-232 port on the VL-7304b board is used. It is recommended that these grounds also be connected together at the power supply or motherboard connection.

As shipped jumper V28 is IN. It may be cut (taken out) if the RS-232 port on Channel A is not being used and the ±12V ground needs to be isolated from the noise on the +5V ground. Since most STD Bus analog I/O boards contain their own on-board DC/DC supplies this should not be necessary in most applications.

Section 4
INSTALLATION

HANDLING

** CAUTION ** The VL-7304 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

INSTALLATION

The VL-7304 card can be installed in any slot of an STD Bus card cage.

The VL-7304 does not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on this board are connected together so that the priority chain will not be broken. This board may be inserted between other boards that are using the priority chain.

** CAUTION ** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

** CAUTION ** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

EXTERNAL CONNECTIONS

Connection to the VL-7304 can be made as noted below. Pinout listings for these connectors appear on the following pages. A pinout of the STD Bus connector appears in Section 6.

RS-232 Connectors

26-pin latching header type connectors are used for the RS-232 I/O connectors. These are connectors J1 and J2 on the VL-7304a, and connector J1 on the VL-7304b. These connectors are normally converted to DB-25 type connectors using VersaLogic cable #9560 or similar mass terminated cable assembly. Figure 4-4 lists the pin numbers for these connectors. Pinouts are included for both the on-board connector and for the DB-25 connector after the port has been converted to this format.

Direct connection to these headers can be made using mating connectors such as 3M #3399-7026, AMP #499505-7, or Ansley #609-2641. These connectors should include a strain relief in order to use the built-in latch bars.

RS-422 Connectors

10-pin latching header type connectors are used for the RS-244/485 interfaces. Mating connectors include 3M #3473-7010, AMP #499505-1 or Ansley #609-1041. These connectors should include a strain relief in order to use the built-in latch bars.

Interrupt Connector (J4)

Four interrupt signals are available at connector J4 for connection to an external prioritizer. These interrupts can also be read directly from the card under software control. Connection to the the 10-pin header can be made using 2-pin mating connectors (one for each interrupt line and ground) such as as AMP #530554-1.

J1/J2 Pin	Signal Name	RS-232C Pin
1	-	1
2	-	14
3	TD	2
4	(RCLK)	15
5	RD	3
6	-	16
7	RTS	4
8	RCLK	17
9	CTS	5
10	-	18
11	DSR	6
12	-	19
13	GND	7
14	DTR	20
15	-	8
16	-	21
17	-	9
18	-	22
19	-	10
20	-	23
21	-	11
22	TCLK	24
23	-	12
24	-	25
25	-	13
26	-	-

Note: These connectors can be converted to the RS-232C pinout using VersaLogic cable #9560.

Figure 4-1. RS-232C Connector Pinouts

J2/J3 Pin	Signal Name	Direction
1	TXC+	OUT
2	TXC-	OUT
3	TXD+	OUT
4	TXD-	OUT
5	SGND	-
6	SGND	-
7	RXD-	IN
8	RXD+	IN
9	RXC-	IN
10	RXC+	IN

Figure 4-2. RS-422 Connector Pinouts

J4 Pin	Signal Name	Output Drive (Sink ma)
1	GND	
2	Chan. A Xmit Int.	20
3	GND	
4	Chan. A Recv Int.	20
5	GND	
6	Chan. B Xmit Int.	20
7	GND	
8	Chan. B Recv Int.	20
9	GND	
10	-	

Figure 4-3. Interrupt Connector J4

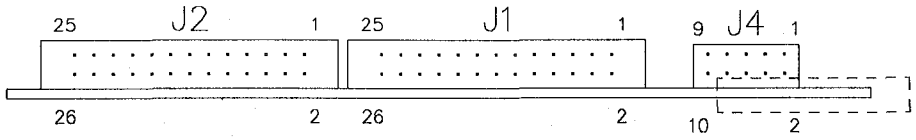


Figure 4-4. VL-7304a Connector Pin Locations

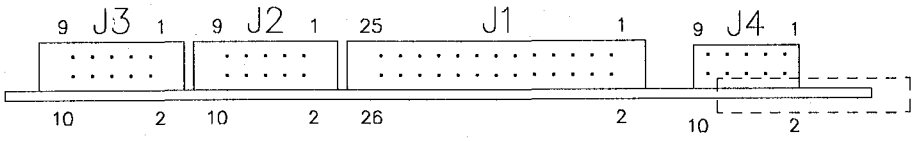


Figure 4-5. VL-7304b Connector Pin Locations

Section 5
OPERATION

INTRODUCTION

This section includes general information about the use and operation of the VL-7304 card. It focuses primarily on the software commands necessary to operate the card and includes examples to assist you in constructing your own software routines.

The end of this section includes information about connecting and using the three interface types (RS-232C, RS-422, and RS-485) available on the VL-7304.

I/O PORT MAPPING

The VL-7304 occupies eight I/O port addresses. The locations of the eight ports is determined by the board address, which is jumper selectable. As shipped, the board is jumpered for hex address E0.

Once the board's I/O address has been determined, the addresses of the eight I/O ports can be determined as shown in Figure 5-1.

I/O Port Address	As Shipped	Read Function	Write Function
Board Address + 0	E0	-	Baud Rate Reg.
Board Address + 1	E1	Ch. B Data	Ch. B Data
Board Address + 2	E2	Ch. B Status	Ch. B Command
Board Address + 3	E3	Ch. A Data	Ch. A Data
Board Address + 4	E4	Ch. A Status	Ch. A Command
Board Address + 5	E5	-	-
Board Address + 6	E6	-	-
Board Address + 7	E7	-	-

Figure 5-1. I/O Port Locations

CONTROL REGISTERS

With the exception of the Baud Rate register, each channel of the VL-7304 has its own separate and independent set of command, data, and status registers. The Baud Rate register allows setting of an independent baud rate for each channel, but both rates are contained in the same 8-bit register.

Baud Rate Register

The Baud Rate register contains the baud rate selection and interrupt enable bits for both channels on the board. It is located at the board address plus 0 (location E0 as shipped).

The baud rate for each channel is selected from a table of eight possible rates. The resulting rate depends on several factors.

First there are two possible baud rate tables that may be used (Table 1 and Table 2). Table 1 should be used for all new applications. Table 2 is included only for compatibility with older designs. The baud rate table used is jumper selectable. Refer to the Configuration section for further information. The board is jumpered for Table 1 when shipped.

Second, in asynchronous mode the serial chip can be programmed to divide the incoming baud rate clock by 16 or 64. Normally the 16X mode is used. In synchronous mode only one set of rates (1X) is available.

Once these factors are known the desired baud rate can be selected by number (0-7) from the appropriate table. The baud rates and interrupt enables can be changed at any time by writing to this register.

The format of the Baud Rate register and listings of the baud rate tables are shown below.

Baud Rate Register							
D7	D6	D5	D4	D3	D2	D1	D0
INT. CH.A	---	BAUD RATE CHANNEL A	----	INT CH.B	---	BAUD RATE CHANNEL B	----

Bit	Description
D7	Channel A Interrupt Enable 0 - Disable interrupts 1 - Enable interrupts
D6-D4	Channel A Baud Rate Select 0-7 - Per the baud rate table
D3	Channel B Interrupt Enable 0 - Disable interrupts 1 - Enable interrupts
D2-D0	Channel B Baud Rate Select 0-7 - Per the baud rate table

Figure 5-2. Baud Rate Register Format

Software Select#	(As shipped) Table 1	Table 2
0	2400	2400
1	600	600
2	300	300
3	1200	1200
4	19200	19200
5	2400	2400
6	4800	19200
7	9600	19200

Figure 5-3. 16X Async. Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	600	600
1	150	150
2	75	75
3	300	300
4	4800	4800
5	600	600
6	1200	4800
7	2400	4800

Figure 5-4. 64X Async. Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	38400	38400
1	9600	9600
2	4800	4800
3	19200	19200
4	N/A*	N/A*
5	38400	38400
6	N/A*	N/A*
7	N/A*	N/A*

* Not available. Higher than the 60K baud limit of the serial chip (76.8K baud).

Figure 5-5. Sync. Mode Baud Rate Options

Command Register

The Command registers (one for each channel) allow the transmitter and receiver to be enabled/disabled, control of the RTS and DTR lines, and several other primary functions.

They are located at the board address plus 2 and board address plus 4 (locations E2 and E4 as shipped) for channel B and A respectively. Data may be written to the Command registers at any time, except immediately following a reset command (when a Mode instruction byte is expected).

The command register format is shown below.

Command Register

D7	D6	D5	D4	D3	D2	D1	D0
HUNT	RESET	RTS CNTL	ERROR RESET	BREAK	RECEIVE ENABLE	DTR CNTL	TRANSMIT ENABLE

Bit	Description
D7	Enter Hunt Mode (for sync. operation only) 1 - Enter Hunt mode
D6	Reset 1 - Reset chip (to receive a Mode instruction)
D5	RTS control (for RS-232 interface use only) 0 - Set RTS line low 1 - Set RTS line high (ready)
D4	Error flag reset 1 - Reset PE, OE, and FE flags
D3	Break 1 - Force transmit line high (break condition)
D2	Receive enable 0 - Disable receiver 1 - Enable receiver
D1	DTR control 0 - Set DTR line low (Enable RS-422/485 xmit driver) 1 - Set DTR line high (Disable RS-422/485 xmit driver)
D0	Transmit enable 0 - Disable transmitter 1 - Enable transmitter

Figure 5-6. Command Register Format

Status Register

The Status registers (one for each channel) allow the readiness and error status of the serial controller chip to be determined at any time.

They are located at the board address plus 2 and board address plus 4 (locations E2 and E4 as shipped) for channel B and A respectively.

The Status register format is shown below.

Status Register							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DSR	BRKDET/ SYNDET	FRAME ERROR	OVERRUN ERROR	PARITY ERROR	BUFFER EMPTY	RCVR READY	XMITR READY

Bit Description

D7 Data Set Ready
= 1 when DSR input line is high (ready).

D6 Break/sync Detect
Async: = 1 when data input line is in a break condition.
Sync: = 1 when 1 (or 2) sync characters have been detected.(2)

D5 Framing Error (async only)
= 1 when a stop bit was not detected at the end of a received character.(1)

D4 Overrun Error
= 1 when receive buffer was not read before another character was received.(1)

D3 Parity Error
= 1 when a parity error is detected.(1)

D2 Transmit Done (not normally used)
= 1 when the transmitter is actually done. Can be used with half-duplex operation to know when to turn the line around.

D1 Receiver Ready
= 1 when a character has been received and is available for reading by the system (reading the character from the data port resets this bit).

D0 Transmitter Ready
= 1 when data may be written to the transmit buffer.

Notes:
1) This error does not inhibit further operation of the interface chip. The error bit is reset using command bit D4.
2) Reading the status register resets this bit.

Figure 5-7. Status Register Format

Data Register

The Data registers (one for each channel) allow data to be read from the receiver or written to the transmitter.

They are located at the board address plus 1 and board address plus 3 (locations E1 and E3 as shipped) for channel B and A respectively. Data should be read or written to the controller chip only when the Status register indicates that the transmitter or receiver (as applicable) is ready.

When transmitting characters that are less than 8 bits long only the lower n bits are used. The upper bits are "don't care".

When receiving characters that are less than 8 bits long only the lower n bits are significant. The unused upper bits are set to zero. The parity bit (if used) is checked by the controller chip, but does not appear in the received data register.

ASYNCHRONOUS MODE

The 8251A type controller chips which are used on the VL-7304 can be programmed for synchronous or asynchronous operation. Operation in the asynchronous mode will be discussed in this section.

Asynchronous operation allow data to be sent and received without respect to any external clock or time frame. It is normally used for RS-232C communications, and can be used with the RS-422 interface if desired.

The highest asynchronous baud rate available on the VL-7304 is 19,200 baud. Applications that require higher data rates should consider operation in the synchronous mode.

Initialization

Before transmitting or receiving can begin, the controller chips must be initialized. This process consists of three steps- 1) clearing (resetting) the chip, 2) setting the operating mode (baud rate, word length, parity type, etc.), and 3) enabling the transmit and receive functions. All of these operations are performed by writing to the control port for the desired channel.

A typical initialization sequence for channel A is shown below. The same procedure (using the channel B command port) would be used to initialize channel B.

```
;Async initialization example for the VL-7304 (8251A chip).

                ;Define port locations.
00E0            SER_BOARD EQU   E0H             ;Board address = hex E0.
00E0            BAUD_REG  EQU   SER_BOARD + 0   ;Baud rate/int. reg.
00E1            SB_DATA   EQU   SER_BOARD + 1   ;Chan. B data reg.
00E2            SB_STAT   EQU   SER_BOARD + 2   ;Chan. B status reg.
00E2            SB_CMD    EQU   SER_BOARD + 2   ;Chan. B command reg.
00E3            SA_DATA   EQU   SER_BOARD + 3   ;Chan. A data reg.
00E4            SA_STAT   EQU   SER_BOARD + 4   ;Chan. A status reg.
00E4            SA_CMD    EQU   SER_BOARD + 4   ;Chan. A command reg.

0100                      ORG   100H            ;Start of code.

                        ;Initialize baud rate generator.
0100    3E 44           LD  A,44H       ;Set both chan. to 19.2K baud.
0102    D3 E0           OUT (BAUD_REG),A
0104
                        ;Initialize channel A.
0104    AF              XOR A           ;Set A to zero
0105    D3 E4           OUT (SA_CMD),A  ;Write it three times.
0107    D3 E4           OUT (SA_CMD),A
0109    D3 E4           OUT (SA_CMD),A
010B    3E 40           LD  A,40H       ;and do a reset command
010D    D3 E4           OUT (SA_CMD),A
010F
010F    3E 7A           LD  A,01111010B ;Set mode to 7 data +
0111    D3 E4           OUT (SA_CMD),A  ;even parity + 1 stop.
0113
0113    3E 37           LD  A,00110111B ;Enable tran. and Recv.
0115    D3 E4           OUT (SA_CMD),A  ;and set RTS & DTS.

                ;(continue with program or return to caller)
```

The example above programs channel A for operation at 19,200 baud with 7 data bits, even parity, and one stop bit (a typical configuration used in RS-232 systems). Each channel can also be programmed for several other data formats by changing the appropriate bits (as listed below) in the Mode instruction. The Mode instruction is accepted only during channel initialization. It must occur immediately following the reset (hex 40) command.

After the Mode instruction is written to it the chip reverts to the Command mode. A command should then be written to enable the receiver and transmitter.

The operating mode may be reprogrammed at any time by writing a Reset command (hex 40) followed by a Mode instruction. At power-up however, the chip is in an undetermined state, and the initialization sequence above (3 zero bytes followed by a hex 40) should be used before the Mode instruction.

Async. Mode Instruction Format

D7	D6	D5	D4	D3	D2	D1	D0
-STOP BITS-		PARITY TYPE	PARITY ENABLE	-CHARACTER- LENGTH		BAUD CLOCK DIVISOR	

Bit	Description
D7, D6	Number of Stop Bits to Transmit.* 00 - Invalid 01 - 1 bit 10 - 1 1/2 bits 11 - 2 bits
D5	Parity Type. 0 - Odd 1 - Even
D4	Parity Bit Enable. 0 - Disable 1 - Enable
D3, D2	Character Length (doesn't include parity bit). 00 - 5 bits 01 - 6 bits 10 - 7 bits 11 - 8 bits
D1, D0	Baud Rate Divisor. 00 - (sync mode) 01 - 1X (don't use) 10 - 16X 11 - 64X

* Receiver always requires only one (or more) stop bits.

Figure 5-8. Mode Instruction Format For Asynchronous Operation

Receiving

Once a serial channel is initialized, it can receive data from a connected device at any time. To see if a character has been received, the status port is read.

When the D1 bit in the status register is high a character has been received and is available to be read from the data buffer. The board can be polled (read) at any time to check the receive status. Refer to Interrupts in this section for interrupt operation.

If hardware handshaking is being used, it may also be necessary to set the RTS line (D5 in the command register) high or low to tell the connected device that you are ready/not ready to receive data.

Typical routines are shown in the Z80 examples below.

```
                    ;SERIAL INPUT EXAMPLE #1
                    ;Wait for a character to be received and return
                    ;to the caller with character in "A".
                    ;
0117   DB E4        READ1    IN  A,(SA_STAT)   ;Get the status
0119   E6 02                 AND 2             ;Mask the recv status
011B   28 FA                 JR  Z,READ1       ;Loop if not ready
011D   DB E3                 IN  A,(SA_DATA)   ;Read the character
011F   C9                    RET               ;Return to caller


                    ;SERIAL INPUT EXAMPLE #2
                    ;Check receive buffer and return with character
                    ;in "A" if one has been received.  Return with
                    ;A=0 if no character waiting.
                    ;
0120   DB E4        READ2    IN  A,(SA_STAT)   ;Get the status
0122   E6 02                 AND 2             ;Mask the recv status
0124   C8                    RET Z             ;Return A=0 (no data)
0125   DB E3                 IN  A,(SA_DATA)   ;Read the character
0127   C9                    RET               ;Return with data
```

Transmitting

Operation of the board for transmitting data is similar to receiving it. Data may be written to the transmit buffer (to be automatically transmitted as soon as the previous character transmission is completed) whenever the status bit D0 is high.

Transmitting will only occur when the CTS input line is high (i.e. the connected device signals that it is ready to receive data). If the CTS line goes low transmitting will halt after the current character is completed. If the connecting device does not use hardware handshaking (RTS/CTS lines) and does not hold this line permanently high, the CTS input may be jumpered "always ready" on the VL-7304 board. See the Configuration section for more information.

In some applications it may also be necessary to check the DSR input line to make sure that the connected device is turned on and ready to receive data.

For interrupt driven operation refer to Interrupts in this section.

A typical Z80 non-interrupt driven output routine is shown below.

```
                    ;SERIAL OUTPUT EXAMPLE
                    ;Transmit the character in "C", (changes "A").
                    ;
0128   DB E4        XMITA    IN  A,(SA_STAT)  ;Get the status
012A   E6 01                 AND 1            ;Mask the xmit status
012C   28 FA                 JR  Z,XMITA      ;Loop if not ready
012E   79                    LD  A,C          ;Move char to A
012F   D3 E3                 OUT (SA_DATA),A  ;Write the character
0131   C9                    RET              ;Return to caller
```

SYNCHRONOUS MODE

Each VL-7304 channel can operate in either synchronous and asynchronous mode. Asynchronous operation is generally simpler and easier to use, while the synchronous mode allows higher speed operation.

In the async mode characters are transmitted only when data is written to the transmit buffer. Since it is never known when a character might start, it is harder to tell the difference between noise on the line and a real data bit. For proper error checking the bits must be longer and the transmission rates lower.

In sync mode characters are transmitted constantly to maintain synchronization between the transmitter and receiver. When data does not need to be transmitted, fill ("sync") characters are automatically inserted by the controller chip. The receiver knows when to expect the next bit (or character) and constantly checks itself by reading the fill (sync) characters.

Since transmitter and receiver are closely synchronized in this mode, the baud rate clock must be the same. This normally means that the transmitter is clocked from an on-board generator, and the same clock is also connected (along with the data lines) to the receiver. Both of the channels on the VL-7304 include a clock output (for the transmitter) and a clock input (for receiving).

Sync mode operation may be used with the RS-232 or RS-422 interfaces (although RS-232 lines do not operate well above 19,200 baud or over long distances). In either case the receiver clock input line on the VL-7304 must be connected to the same clock source as the transmitter of the connected device (i.e. the transmit clock output of the connected device). The receiver must also be re-jumpered to use the external clock input line (rather than the on-board baud rate clock). See Baud Rate Clock Inputs in Section 3.

The VL-7304 can operate at up to 38,400 baud in sync mode.

Initialization

Before transmitting or receiving can begin, the controller chips must be initialized. This process consists of three steps- 1) clearing (resetting) the chip, 2) setting the operating mode (baud rate, word length, parity type, etc.), and 3) enabling the transmit and receive functions. All of these operations are performed by writing to the control port for the desired channel.

A typical initialization sequence for channel A is shown below. The same procedure (using the channel B command port) would be used to initialize channel B.

```
                    ;Sync initialization example for the VL-7304 (8251A chip).
                    ;
                    ;Define port locations.
      00E0          SER_BOARD EQU   E0H             ;Board address = E0.
      00E0          BAUD_REG  EQU   SER_BOARD + 0   ;Baud rate/int. reg.
      00E1          SB_DATA   EQU   SER_BOARD + 1   ;Chan. B data reg.
      00E2          SB_STAT   EQU   SER_BOARD + 2   ;Chan. B status reg.
      00E2          SB_CMD    EQU   SER_BOARD + 2   ;Chan. B command reg.
      00E3          SA_DATA   EQU   SER_BOARD + 3   ;Chan. A data reg.
      00E4          SA_STAT   EQU   SER_BOARD + 4   ;Chan. A status reg.
      00E4          SA_CMD    EQU   SER_BOARD + 4   ;Chan. A command reg.

0100                        ORG   100H              ;Start of code.

                          ;Initialize baud rate generator.
0100  3E 77               LD  A,77H   ;Set both chan. to 38.4K baud.
0102  D3 E0               OUT (BAUD_REG),A
0104
                          ;Initialize channel A.
0104  AF                  XOR A             ;Set A to zero
0105  D3 E4               OUT (SA_CMD),A    ;Write it three times.
0107  D3 E4               OUT (SA_CMD),A
0109  D3 E4               OUT (SA_CMD),A
010B  3E 40               LD  A,40H         ;and do a reset command
010D  D3 E4               OUT (SA_CMD),A

010F  3E BC               LD  A,10111100B ;Set mode to 8 bits +
0111  D3 E4               OUT (SA_CMD),A  ;even parity w/1 sync.

0113  3E AA               LD  A,AAH         ;Set sync character
0115  D3 E4               OUT (SA_CMD),A

0117  3E A4               LD  A,10100100B ;Enable tran., Recv,
0119  D3 E4               OUT (SA_CMD),A  ;Hunt & DTR.

                          ;(continue with program or return to caller)
```

The example above programs channel A for operation at 38.4K baud with 8 data bits, even parity, and single character sync. Other data formats can be selected by changing the appropriate bits (as listed below) in the mode instruction. The mode instruction is accepted only during channel initialization. It must occur immediately following the reset (hex 40) command.

The operating mode may be reprogrammed at any time by writing a Reset command (hex 40) followed by a Mode instruction. At power-up however, the chip is in an undetermined state, and the initialization sequence above (3 zero bytes followed by a hex 40) should be used before the Mode instruction.

After the Mode instruction is written, one or two sync characters must be provided. These are the character(s) that the transmitter and receiver will use for synchronizing and data fill. If the double sync mode has been selected then two characters must be provided, otherwise a single character should be written to the controller.

The double sync mode operates identically to single sync except that both characters must be received (in order) before the receiver considers itself synchronized. When gaps in the data stream occur, they are filled with the two sync characters instead of one. They essentially act as one long sync character.

After initializing the sync character(s), the controller returns to command mode.

Next a command is written to enable the receiver and transmitter and put the receiver in the "hunt" mode.

When using the RS-422/485 interface the DTR line (bit D1 in the control register) must be set low to enable the transmit drivers. Setting it high tri-states the transmit drivers (clock and data). For RS-422 use, this bit is should be set and left low. For RS-485 use, it is set low only while transmitting to allow party line access to the clock and data lines. The RS-422/485 interface does not use the RTS control signal.

When using the RS-232C interface it may be necessary to set the RTS line and/or the DTR line high to tell the connected device that you are ready to transmit and receive data (see Figure 5-6).

The Hunt mode causes the receiver to begin looking for the sync character(s). It compares each received character, on each bit boundary, with the sync character(s). When a match is found the SYNDET (sync detect) flag is set high in the status register and the receiver can begin receiving data.

If the data is continuously received (never interrupted), the receiver will stay in sync. If the communication link is broken or interrupted, the receiver must be programmed back into the Hunt mode so that it can hunt for a sync character once again.

The SYNDET bit is set whenever a sync characters(s) is received. It is reset whenever the status register is read.

Sync Mode Instruction Format

D7	D6	D5	D4	D3	D2	D1	D0
SYNC TYPE	0	PARITY TYPE	PARITY ENABLE	CHAR. LENGTH		0	0

Bit	Description
D7	Sync Char Type 0 - Double sync character (sync requires two characters) 1 - Single sync character
D6	Sync Detect 0 - Internal sync detect 1 - External sync detect (don't use)
D5	Parity Type 0 - Odd 1 - Even
D4	Parity Bit Enable 0 - Disable 1 - Enable
D3, D2	Character Length (doesn't include parity bit). 00 - 5 bits 01 - 6 bits 10 - 7 bits 11 - 8 bits
D1, D0	00 - (sync mode)

Figure 5-9. Mode Instruction Format For Synchronous Operation

Receiving

When a serial channel is initialized, it should be programmed to enter the Hunt mode to find and lock onto the next sync character(s) that is received.

The initializing or receiving routine should check the SYNDET (sync detect) flag in the status register to make sure that sync has occurred (SYNDET bit high). It may not occur if the communication line is not connected or operational, or the transmitter is not sending sync characters. Once sync has occurred, characters can be received and can be read from the receive buffer whenever status bit 1 is high.

If the data is continuously received (never interrupted), the receiver will stay in sync. If the communication link is broken or interrupted, the receiver must be programmed back into the Hunt mode so that it can hunt for a sync character once again.

The SYNDET bit is set whenever a sync bit is received. It is reset whenever the status register is read.

Once the receiver is in sync (it has exited from the Hunt mode), sync characters are treated like any other data character (except that the SYNDET status bit is set high when each sync character is received). They are received, delivered to the receive buffer, and the receive ready flag is set high. They must be read from the data buffer or an overrun error will occur.

Parity and overrun conditions are checked with each character received, just as in the asynchronous mode. Framing errors are not applicable to sync operation.

When bit 1 in the status register is high a character has been received and is available to be read from the data buffer. The board can be polled (read) at any time to check the receive status. Refer to Interrupts in this section for interrupt operation.

Depending on the character length and the sync character(s) selected it can be difficult to tell the difference between transmitted data and sync (fill) characters that are automatically inserted by the transmitter. This confusion can be avoided in a number of ways. The easiest is to choose a sync character that will never occur in the data stream (i.e. 00 or 7F with ASCII data). Another is to transmit data in fixed or variable length blocks.

For block transfers a start-of-block character (of your choosing) is sent followed by a count or length byte (for variable length blocks). These are followed by n number of characters per the length byte (or an agreed upon fixed length). Since the transmitter prepares the entire message in advance and transmits it without any gaps, all characters received (in the block) will be data. Sync character fill will never occur. After receiving the block, the receiver can receive (and ignore) sync characters until the next start-of-block character signals the start of another data block.

The software to simply check the status bit and read the data register is identical to that in asynchronous operation. Refer to the asynchronous Receiving section for software examples.

Transmitting

Operation of the board for transmitting synchronous data is similar to receiving it. Data may be written to the transmit buffer (to be automatically transmitted as soon as the previous character transmission is completed) whenever the status bit D0 is high.

Transmitting will only occur when the CTS input line is high (i.e. the connected device signals that it is ready to receive data). If the CTS line goes low transmitting will halt after the current character is completed. If the connecting device does not use hardware handshaking (RTS/CTS lines) and does not hold this line permanently high, the CTS input may be jumpered "always ready" on the VL-7304 board. See the Configuration section for more information.

In some applications it may also be necessary to check the DSR input line to make sure that the connected device is turned on and ready to receive data.

If data is not loaded into the transmit buffer before transmission of the current character has completed, then a sync character(s) (as defined during initialization) will be automatically inserted into the data stream.

Single character transmission involves simply checking the transmit ready flag and writing the data character to the data register. See the asynchronous Transmitting section for a software examples.

For interrupt driven operation refer to the Interrupts section.

INTERRUPTS

The VL-7304 board has two interrupt methods available. On-board interrupt facilities provide for standard polled interrupts, while the interrupt signal connector allows the interrupt status signals to be connected to an external interrupt prioritizer card.

Polled interrupts take longer to service than vectored interrupts since the source of the interrupt must be found before the proper routine can be called. Externally vectored (prioritized) interrupts are faster to service but add extra hardware cost and complication to the system.

Polled Operation

Polled operation is controlled by the interrupt enable bits in the Baud Rate register. The bits, one for each channel, allow the transmit and receive ready signals to cause an interrupt to the system processor. These ready signals are similar to the transmit and receive ready bits in the status registers.

Since these are not vectored interrupts, the CPU is not provided with an interrupt address, it simply knows that some interrupt source needs to be serviced. Once the interrupt occurs, the status registers in the serial controllers (and any other interrupt sources) can be checked to see which needs service. In the case of the VL-7304 card the transmit and receive ready bits should be checked. The processor must be operated in interrupt mode 1 to use polled interrupts.

The listing below shows how polled interrupts might be used.

Polled interrupts take longer to service than vectored interrupts since the source of the interrupt must be found before the proper routine can be called. This is not a problem in system with relatively few interrupt sources, but may not be effective in systems with many interrupt sources to check.

In systems with many interrupt sources, the interrupt processing time can be enhanced by selecting the order in which interrupt sources are checked. Checking the most frequently occurring interrupt source first (and the least frequent source last) will eliminate unnecessary processing time. Of course, the interrupt processing time is not important unless: interrupt response time is critical, very little CPU time is available to handle interrupts, or interrupts will occur very frequently.

```
                        ;Polled interrupt example for the VL-7304

                        ;Define port locations.
        00E0    SER_BOARD EQU   E0H             ;Board address = E0.
        00E0    BAUD_REG  EQU   SER_BOARD + 0   ;Baud rate/int. reg.
        00E1    SB_DATA   EQU   SER_BOARD + 1   ;Chan. B data reg.
        00E2    SB_STAT   EQU   SER_BOARD + 2   ;Chan. B status reg.
        00E2    SB_CMD    EQU   SER_BOARD + 2   ;Chan. B command reg.
        00E3    SA_DATA   EQU   SER_BOARD + 3   ;Chan. A data reg.
        00E4    SA_STAT   EQU   SER_BOARD + 4   ;Chan. A status reg.
        00E4    SA_CMD    EQU   SER_BOARD + 4   ;Chan. A command reg.

0100                      ORG   100H            ;Start of code.


                        ;Initialize system for interrupt operation
0100  ED 56     INITIL1   IM  1                 ;Use interrupt mode 1.
0102  3E C3               LD  A,C3H             ;Put a jump at system
0104  32 38 00            LD  (38H),A           ;interrupt addr (38H)
0107  21 12 01            LD  HL,INT            ;to the interrupt
010A  22 39 00            LD  (39H),HL          ;service routine.
010D  FB                  EI                    ;Enable CPU interrupts.

010E  3E 88               LD  A,10001000B       ;Enable the VL-7304 intrpts.
0110  D3 E0               OUT (BAUD_REG),A      ;(usually done in the 7304
                                                ;initialization routine).
0112
                          ;(Return to caller or do more initialization)


                        ;Interrupt service routine.
                        ;This is were the CPU jumps when an interrupt occurs.
0112  D9        INT       EXX                   ;Save reg's (B-L to B-L'
0113  08                  EX AF,AF'             ;and AF to AF').

0114  DB E4               IN A,(SA_STAT)        ;Is the interrupt from
0116  E6 03               AND 00000011B         ;the VL-7304 channel A?
0118  18 08               JR  INTJ1             ;No, check other sources
011A  E6 01               AND 00000001B         ;Yes, is it transmit?
011C  C2 2A 01            JP  NZ,XMITA          ;Yes, go do it.
011F  C3 2E 01            JP  RECVA             ;No, must be receive

0122  DB E2     INTJ1     IN  A,(SB_STAT)       ;Is it from channel B?
0124  E6 03               AND 00000011B
0126  18 02               JR  INTJ2             ;No, check other sources
0128  E6 01               AND 00000001B         ;Yes, is it transmit?
                          ;etc.

                INTJ2     ; .                   ;Check other sources
                          ; .
                          ; .
```

```
                    XMITA   ;Routine for Transmitting from chan. A
                            ;
                            ;  - Increment a buffer pointer,
                            ;    send the next char, etc.
                            ;
012A   D9                   EXX             ;Exchange the reg's back.
012B   08                   EX AF,AF'
012C   ED 4D                RETI            ;Return & re-enable int's.


                    RECVA   ;Routine for Receiving from chan. A
                            ;
                            ;  - Read the character,
                            ;    put it in a buffer, etc.
                            ;
012E   D9                   EXX             ;Exchange the reg's back.
012F   08                   EX AF,AF'
0130   ED 4D                RETI            ;Return & re-enable int's.
0132
```

External Prioritization

To use the board with an external interrupt prioritizer (or other vectored interrupt inputs, such as on some timer/counter chips) the desired interrupt signals should be connected from the J4 connector to the external card. See Section 4 (Installation) for connector details.

Interrupt signals are available for Chan. A Transmit Ready, Chan. A Receive Ready, Chan. B Transmit Ready, and Chan. B Receive Ready. These signals are similar to the transmit and receive ready bits in the Status registers. Writing a character to the transmitter, or reading the character from the receiver resets these output lines.

The transmit ready line differs from the transmit ready bit as follows. The transmit ready bit goes active (high) whenever the transmit buffer is empty. The transmit ready output line goes active (low) whenever the transmit buffer is empty and the CTS input line is true (high) and the transmit enable bit is true (high).

The interrupt enable bits in the Baud Rate register should be off (low) for operation with an external prioritizer. These bits control only the system interrupt signal for software polled interrupts. The signals on the J4 connector are always active.

INTERFACE OPTIONS

The VL-7304 card is available with three types of interfaces, RS-232C, RS-422, and RS-485. The VL-7304a version includes two RS-232C interfaces. The VL-7304b version includes one RS-422/485 and one RS-232C/422/485 interface. These interfaces can be used in a wide variety of configurations. Some common configurations will be noted in this section while many other configurations are possible.

The type of interface used does not dictate the data format (sync, async, baud rate, etc.) used. The primary limitation is in the performance of the interface type. In this case the RS-232C interface is the lowest performance type. It is usable only for short runs (to 50 feet) and at fairly low baud rates (to 19,200 baud).

RS-422 is a highly noise immune, higher speed, longer distance interface. Connected with twisted pair wiring it can be used at the VL-7304's fastest rate (38.4K baud) at lengths up to 4000 feet. Its balanced differential transmission is ideal for use in electrically noisy environments (factories. etc.).

The RS-485 interface is an extension of the RS-422 interface. It uses the same transmission method and can support the same data rates and cable lengths. It differs in that it is defined as a multidrop, bi-directional communications link. It allows up to 32 devices to be connected along a single (dual twisted pair) cable which is up to 4000 feet long.

RS-232C Interface

The RS-232C interface is the commonly used standard for connecting terminals, printers, modems, and other local peripheral I/O devices.

It should not be used for speeds greater than 19,200 baud or with cable lengths over 50 feet. Even at lengths of 30 or 40 feet it may be subject to data errors in electrically noisy environments, especially at higher baud rates.

Transmission uses $\pm$12V signals referenced to the system ground line.

The interface consists of a transmit and receive data lines, ready-to-transmit or receive handshake lines, and device ready (power-on) status lines. Some or all of these lines may be used by the connecting device.

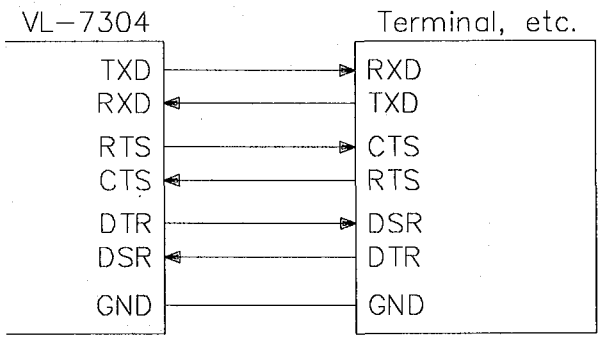
Some devices require connection of only the data lines. Instead of hardware handshake lines, a software handshake protocol (such as XON/XOFF) is used to signal readiness to receive data. In this case the VL-7304 should be jumpered with the CTS signal permanently high, or the connecting cable should be wired to connect a ready output line (DTR) directly to CTS.

Although normally used for asynchronous transmissions, the RS-232C interface can also be used for synchronous operation. In this case the receive clock (RCLK) input must be connected to the clock output line on the connected device. The transmit clock (TCLK) output line is avail-

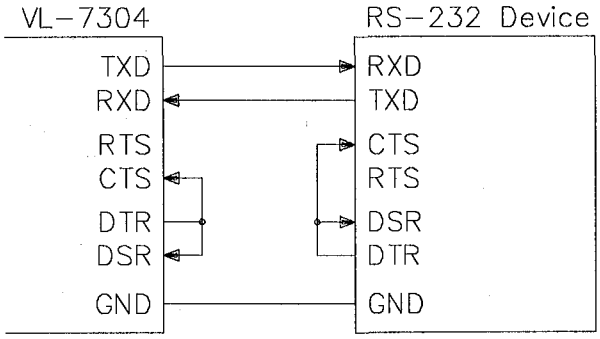
able for connecting to the receive clock line of the external device.

Several typical RS-232C connections are shown below.

The RS-232C interface can be jumpered for two different pinouts. The same signals are available in both cases, only the pin numbers where the signals appear are changed. These jumper options allow for easier connection to external devices without the need for custom interconnecting cables. The VL-7304 can be configured as Data Communications Equipment (DCE) for used with terminals and printers, or as Data Terminal Equipment (DTE) for connection to another computer or other equipment in the DCE configuration. Figure 5-10 details the pinouts for these options. Note that the pin numbers given refer to the RS-232 type connectors and cables (DB-25 type). These are not the pin numbers at the VL-7304 board edge. The VL-7304 connector is converted to the DB-25 type RS-232C connectors using a VersaLogic cable #9560 or similar.



Typical RS-232 Connection



Connection For Software Handshaking

Figure 5-10. Typical RS-232C Connections

VL-7304a Signal		DCE (to Terminal) External RS-232 Device (Pin#)	DTE (to Computer) External RS-232 Device (Pin#)
TXD (Xmit. Data)	---->	RD(3)	TD(2)
RXD (Recv. Data)	<----	TD(2)	RD(3)
RTS (Recv. Handshake)	---->	CTS(5)	RTS(4)
CTS (Xmit. Handshake)	<----	RTS(4)	CTS(5)
DTR (Xmit. Eqpt. Stat.)	---->	DSR(6)	DTR(20)
DCD (Recv. Eqpt. Stat.)	<----	DTR(20)	DSR(6)
TCLK (Xmit. Clock)	---->	TCLK(24)	RCLK(17/15)
RCLK (Recv. Clock)	<----	RCLK(17/15)	TCLK(24)

Figure 5-11. RS-232C Port Pinout Options

RS-422 Interface

RS-422 is a high speed, long distance interface with a high immunity to electrically induced noise. It is connected with twisted pair wiring and can be used at the VL-7304's fastest rate (38.4K baud) at lengths up to 4000 feet.

The RS-422 port can be connected to any other RS-422 type interface including other VL-7304 or VL-7842 CPU boards for communications between control systems. Video terminals and other communications equipment are also available with this interface.

The interface consists of several differential line pairs, one pair for each signal. The differential pairs operate between 0 and 5 volts and carry an inverted and non-inverted copy of the signal.

The signals available are the transmit data, receive data, transmit clock, and receive clock. The transmit and receive clock lines are used only for synchronous transmissions.

The RS-422 interface operates from 5 volt power only and does not require $\pm$ 12 volt power from the system.

Figure 5-12 shows a typical RS-422 connection.

Note that a shielded cable may be used if desired. Shielded cables are used primarily to contain the EMI emission of the RS-422 interface to the outside world (which is not necessary in many applications). Shielded cables have higher capacitance ratings than non-shielded cables and may not be appropriate for very long cable runs. If used, the shield should be connect to earth ground (at some point on the external bulk head connector), not the system logic ground.

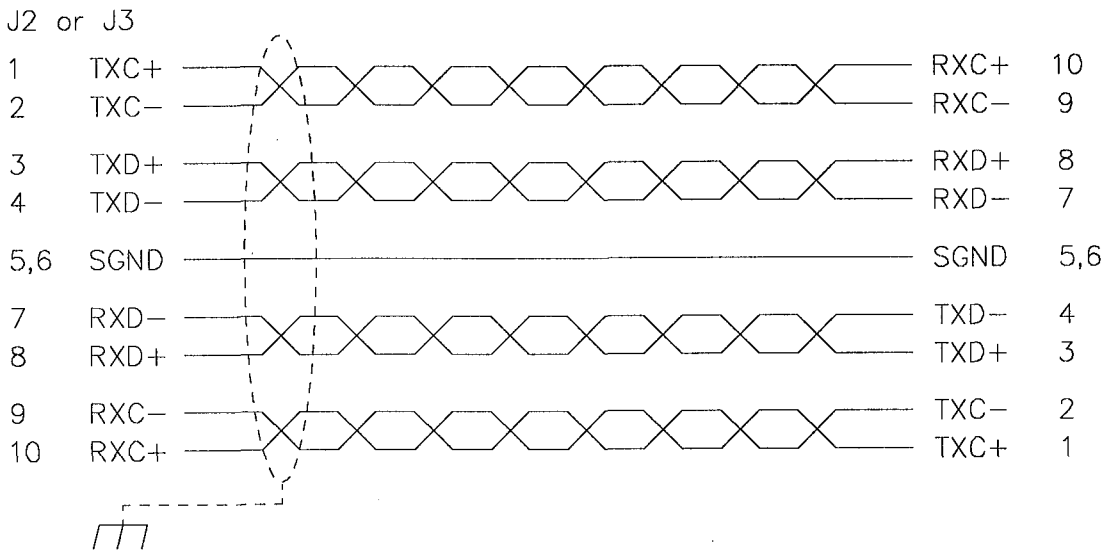


Figure 5-12. Typical RS-422 Connection

RS-485 Interface

The RS-485 interface is an extension of the RS-422 interface. It uses the same transmission method and can support the same data rates and cable lengths. It differs in that it is defined as a multidrop, bi-directional communications link rather than a simple unidirectional interface. It allows up to 32 devices to be connected along a single (dual twisted pair) cable which is up to 4000 feet long.

To use the RS-485 interface, jumpers on the VL-7304 board are inserted that link the transmit and receive lines together. In RS-485 mode transmitting and receiving occurs over the same twisted wire pair. Connected devices must take turns transmitting while all the remaining devices are receiving. This is true for both the transmitted/received data and the transmitted/received clock (used in synchronous mode).

Figure 5-13 shows the typical RS-485 connection.

The DTR bit in the control register controls the data direction (of both data and clock). Setting DTR low enables transmission. Setting it high disables transmission. The receivers are active at all times. They receive all data that occurs on the RS-485 cable (including that sent by your own transmitter). Only one transmission source should be active on the line at any given time.

The RS-485 standard, as with the other interface types, defines only the type of electrical interconnection. The software to communicate with the devices connected to the RS-485 line, and coordinate their actions so that only one transmits at a time, is defined by the applications engineer.

As with the RS-422 interface each twisted pair should be terminated with a 100 ohm resistor at each end of the line. These terminators are normally included at the RS-422 interface (such as on the VL-7304 board). With RS-485 operation however, with many interfaces connected to the same line, too many terminators will be connected. The terminating resistors should be removed from all of the interfaces in the system except for the stations at the physical start and end of the cable run.

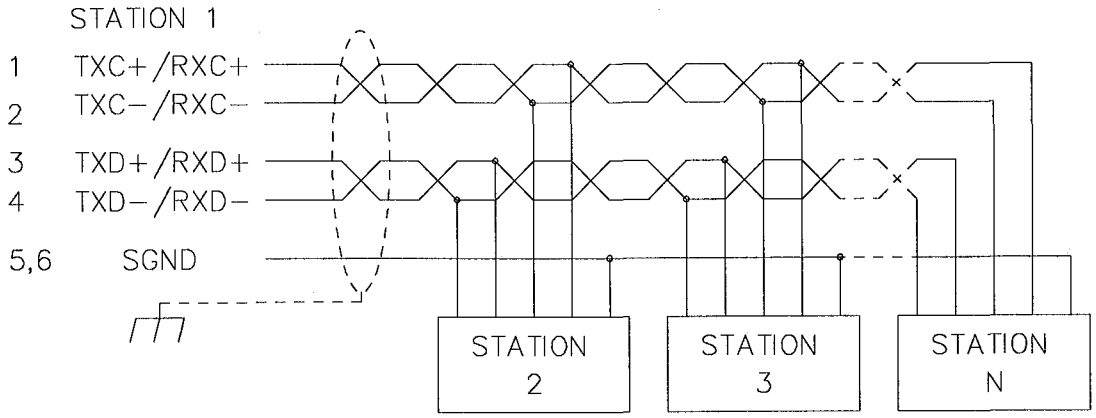
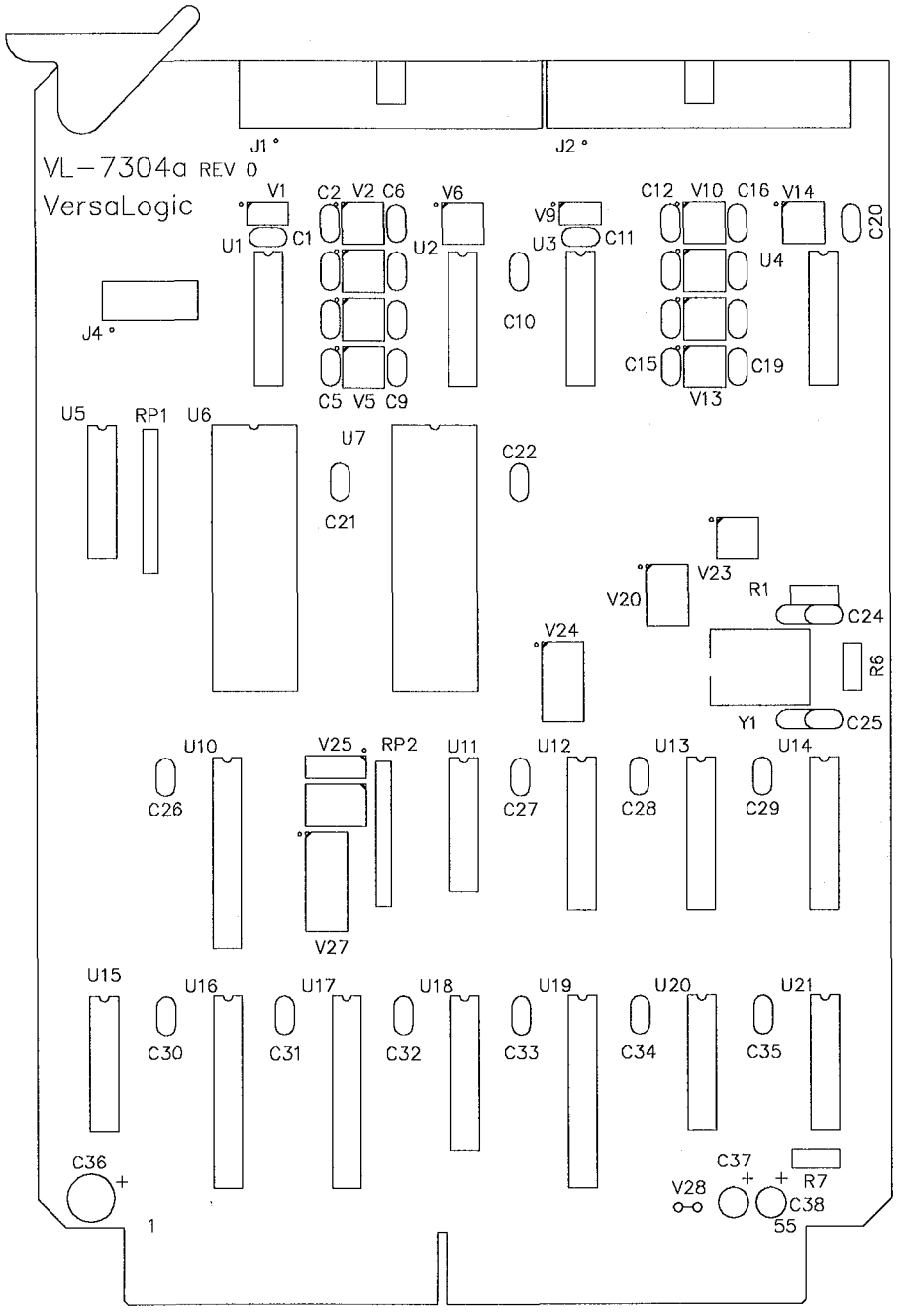
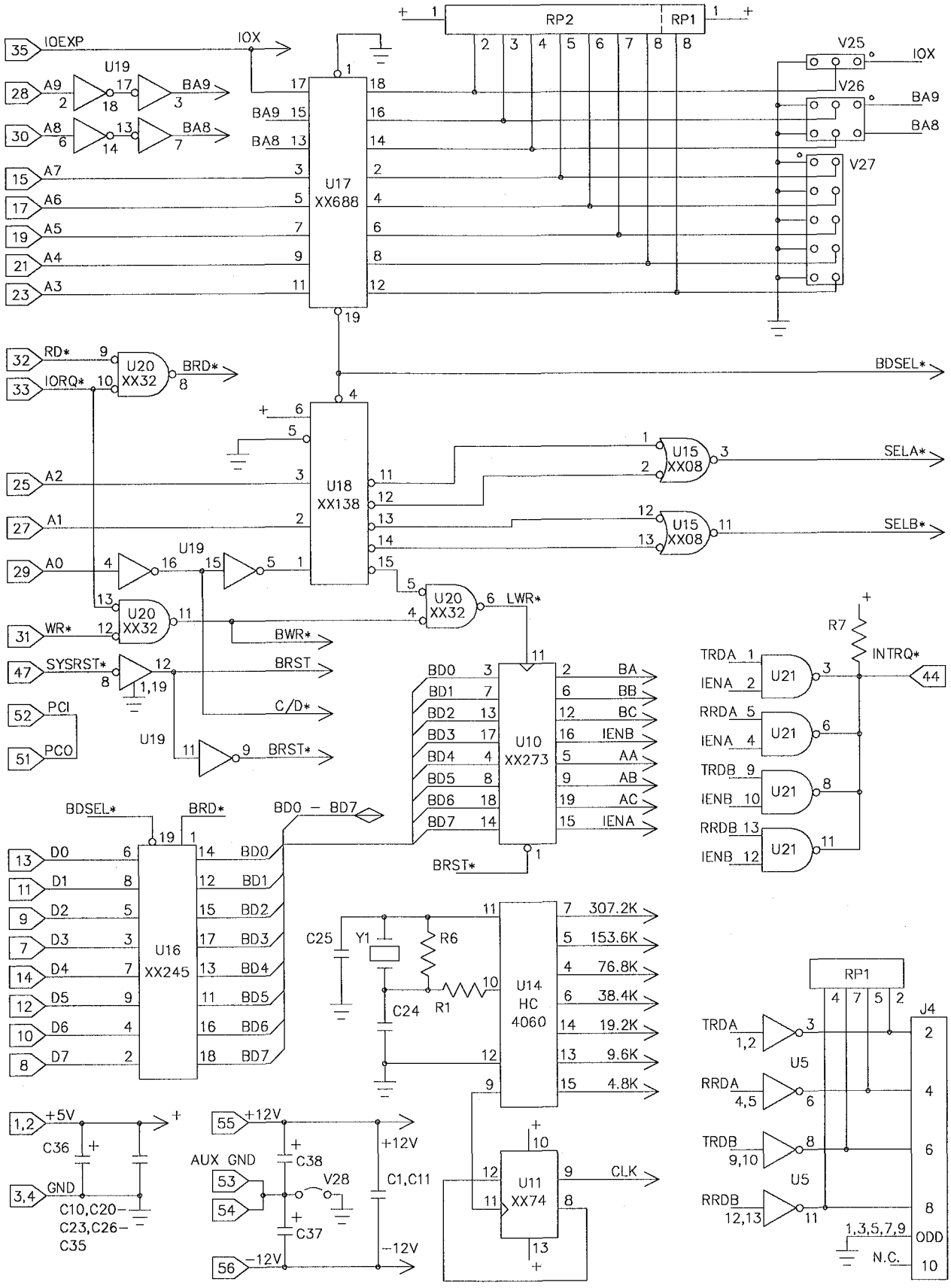
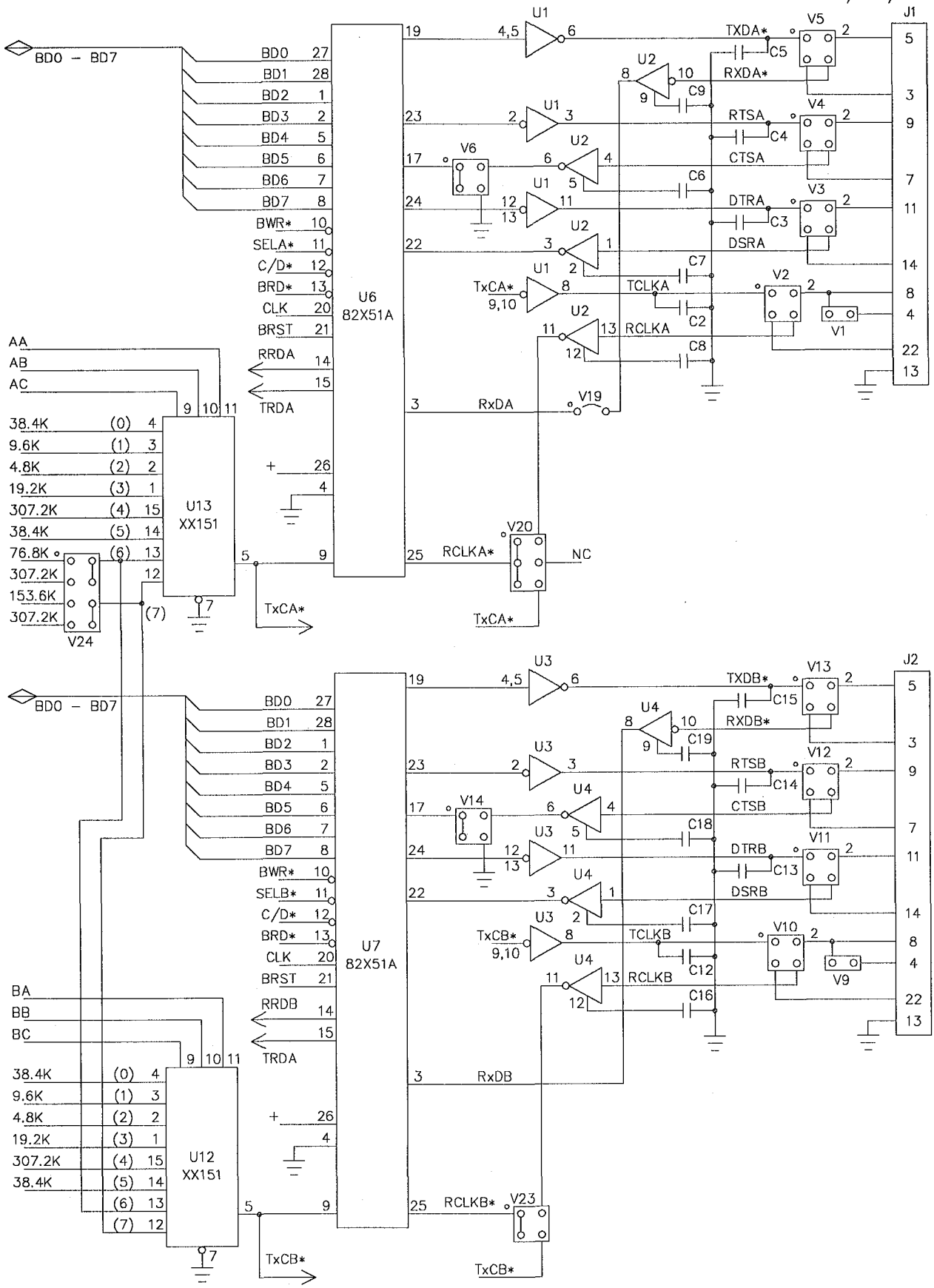


Figure 5-13. Typical RS-485 Connection.


J1
J2
VL-7304a REV 0
VersaLogic
V1
C2
V2
C6
V6
V9
C12
V10
C16
V14
C20
U1
C1
U2
U3
C11
U4
J4
C10
C15
C19
C5
V5
C9
V13
U5
RP1
U6
U7
C22
C21
V23
V20
R1
C24
V24
R6
Y1
C25
U10
V25
RP2
U11
U12
U13
U14
C26
C27
C28
C29
V27
U15
U16
U17
U18
U19
U20
U21
C30
C31
C32
C33
C34
C35
C36
C37
R7
V28
C38
1
55


IOEXP
IOX
U19
A9
BA9
A8
BA8
A7
A6
A5
A4
A3
U17
XX688
RP2
RP1
V25
V26
V27
BA9
BA8
RD*
IORQ*
U20
XX32
BRD*
BDSEL*
U18
XX138
A2
A1
A0
U15
XX08
SELA*
SELB*
WR*
BWR*
SYSRST*
BRST
C/D*
PCI
PCO
BRST*
LWR*
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
U10
XX273
BA
BB
BC
IENB
AA
AB
AC
IENA
R7
INTRQ*
TRDA
IENA
RRDA
TRDB
IENB
RRDB
U21
BDSEL*
BRD*
BD0 – BD7
U16
XX245
D0
D1
D2
D3
D4
D5
D6
D7
C25
Y1
R6
C24
R1
U14
HC
4060
307.2K
153.6K
76.8K
38.4K
19.2K
9.6K
4.8K
+5V
GND
C36
C10,C20–
C23,C26–
C35
+12V
AUX GND
C38
V28
C37
–12V
C1,C11
U11
XX74
CLK
RP1
J4
U5
1,3,5,7,9
ODD
N.C.


BD0 – BD7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BWR*
SELA*
C/D*
BRD*
CLK
BRST
RRDA
TRDA
U6
82X51A
AA
AB
AC
U13
XX151
38.4K
9.6K
4.8K
19.2K
307.2K
38.4K
76.8K
307.2K
153.6K
307.2K
V24
TxCA*
RxDA
RCLKA*
NC
V20
V19
U1
U2
V5
V4
V3
V2
V1
V6
TXDA*
RXDA*
RTSA
CTSA
DTRA
DSRA
TCLKA
RCLKA
C5
C9
C4
C6
C3
C7
C2
C8
J1
BA
BB
BC
U12
XX151
U7
82X51A
RRDB
TRDB
TxCB*
RxDB
RCLKB*
V23
U3
U4
V13
V12
V11
V10
V9
V14
TXDB*
RXDB*
RTSB
CTSB
DTRB
DSRB
TCLKB
RCLKB
C15
C19
C14
C18
C13
C17
C12
C16
J2

VL-7304a PARTS LIST
Dual RS-232 Interface

Capacitors

C1, C10, C11, C20-C22, C26-C35	.01 uf ceramic
C2-C9, C12-C19	390 pf NPO ceramic
C24, C25	22 pf NPO ceramic
C36	22 uf electrolytic, radial
C37, C38	2.2 uf electrolytic, radial

Integrated Circuits

U1, U3	1488
U2, U4	1489A
U5, U21	74LS38
U6, U7	8251A
U10	74LS273
U11	74LS74
U12, U13	74LS151
U14	74HC4060
U15	74LS08
U16	74LS245
U17	74HCT688
U18	74LS138
U19	74LS240
U20	74LS32

Resistors

R1	200 ohm, 5%, 1/4W
R6	1M ohm, 1%, 1/4W
R7	10K ohm, 5%, 1/4W
RP1	10K ohm, 7 resistor SIP
RP2	100K ohm, 7 resistor SIP

Semiconductors

Y1	4.9152 MHz crystal

Miscellaneous

J1, J2	26 pin R/A latching header
J4	10 pin R/A header

VL-73CT04a PARTS LIST
Dual RS-232 Interface (Extended Temperature Version)

Capacitors

C1, C10, C11, C20-C22, C26-C35	.01 uf ceramic
C2-C9, C12-C19	(Not used on CT version)
C24, C25	22 pf NPO ceramic
C36	22 uf electrolytic, radial
C37, C38	2.2 uf electrolytic, radial

Integrated Circuits

U1, U3	14C88
U2, U4	14C89A
U5, U21	54LS38
U6, U7	82C51A
U10	74HCT273
U11	74HCT74
U12, U13	74HCT151
U14	74HC4060
U15	74HCT08
U16	74ACT245
U17	74HCT688
U18	74HCT138
U19	74ACT240
U20	74HCT32

Resistors

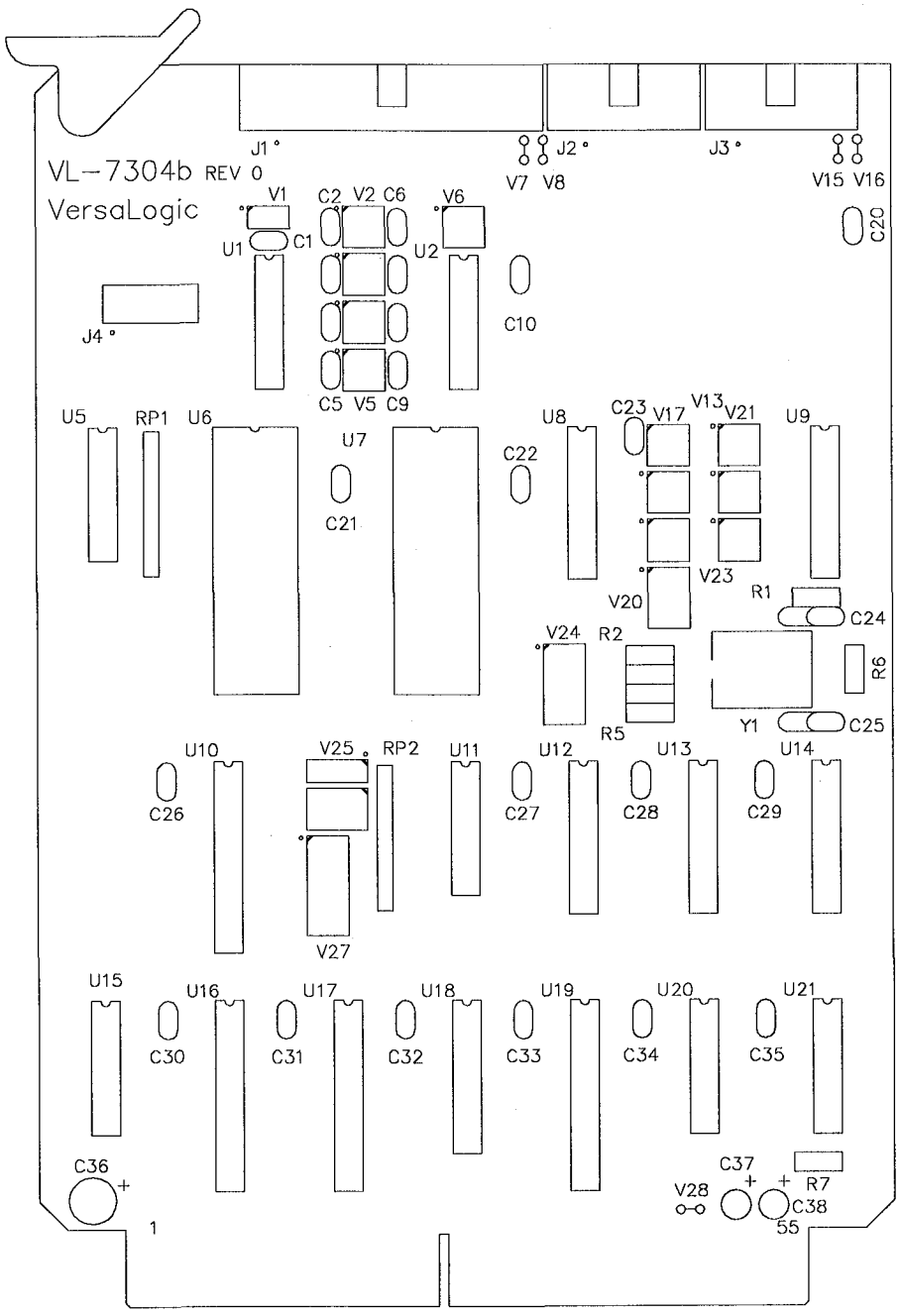
R1	200 ohm, 5%, 1/4W
R6	1M ohm, 1%, 1/4W
R7	10K ohm, 5%, 1/4W
RP1	10K ohm, 7 resistor SIP
RP2	100K ohm, 7 resistor SIP

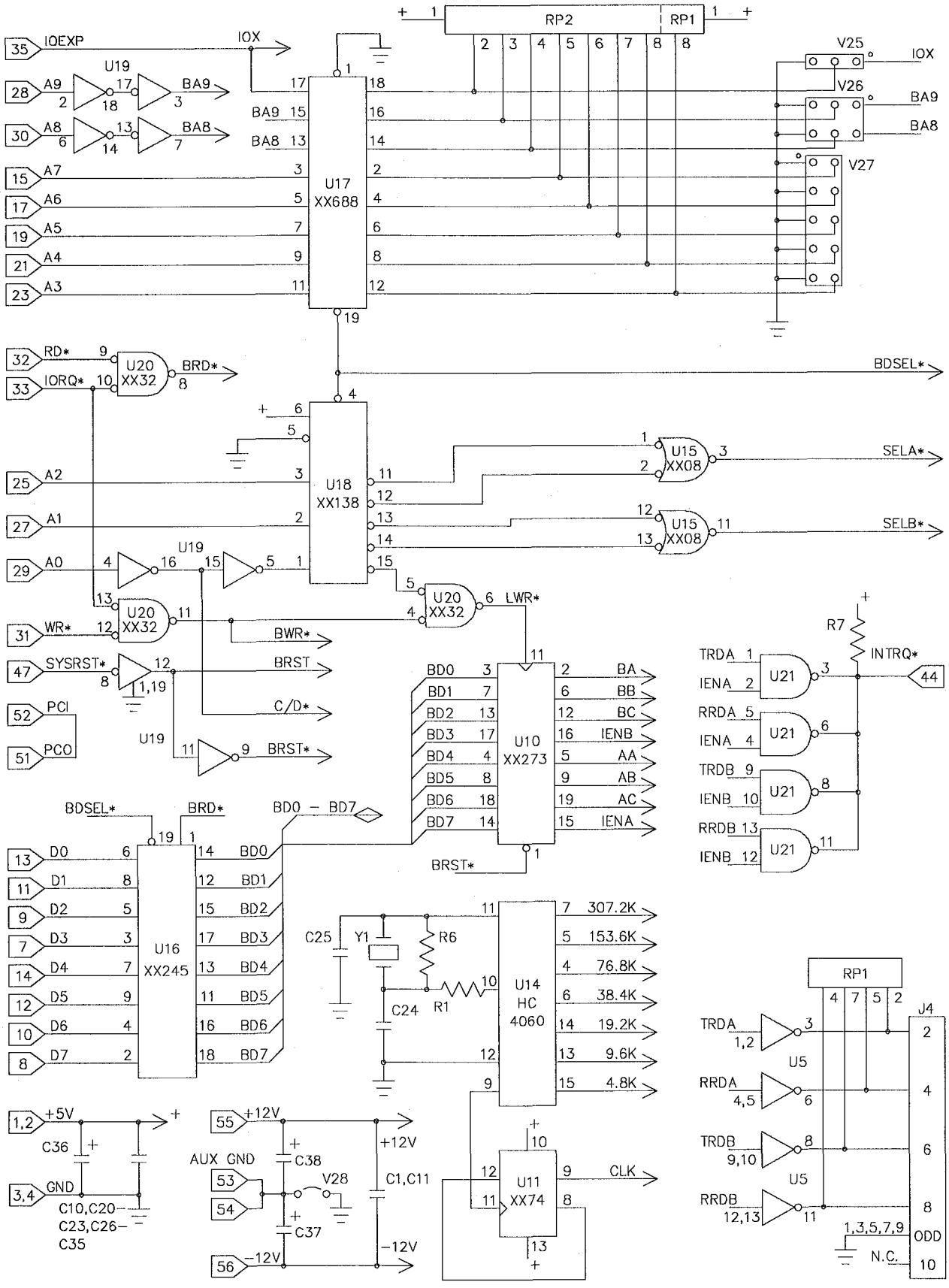
Semiconductors

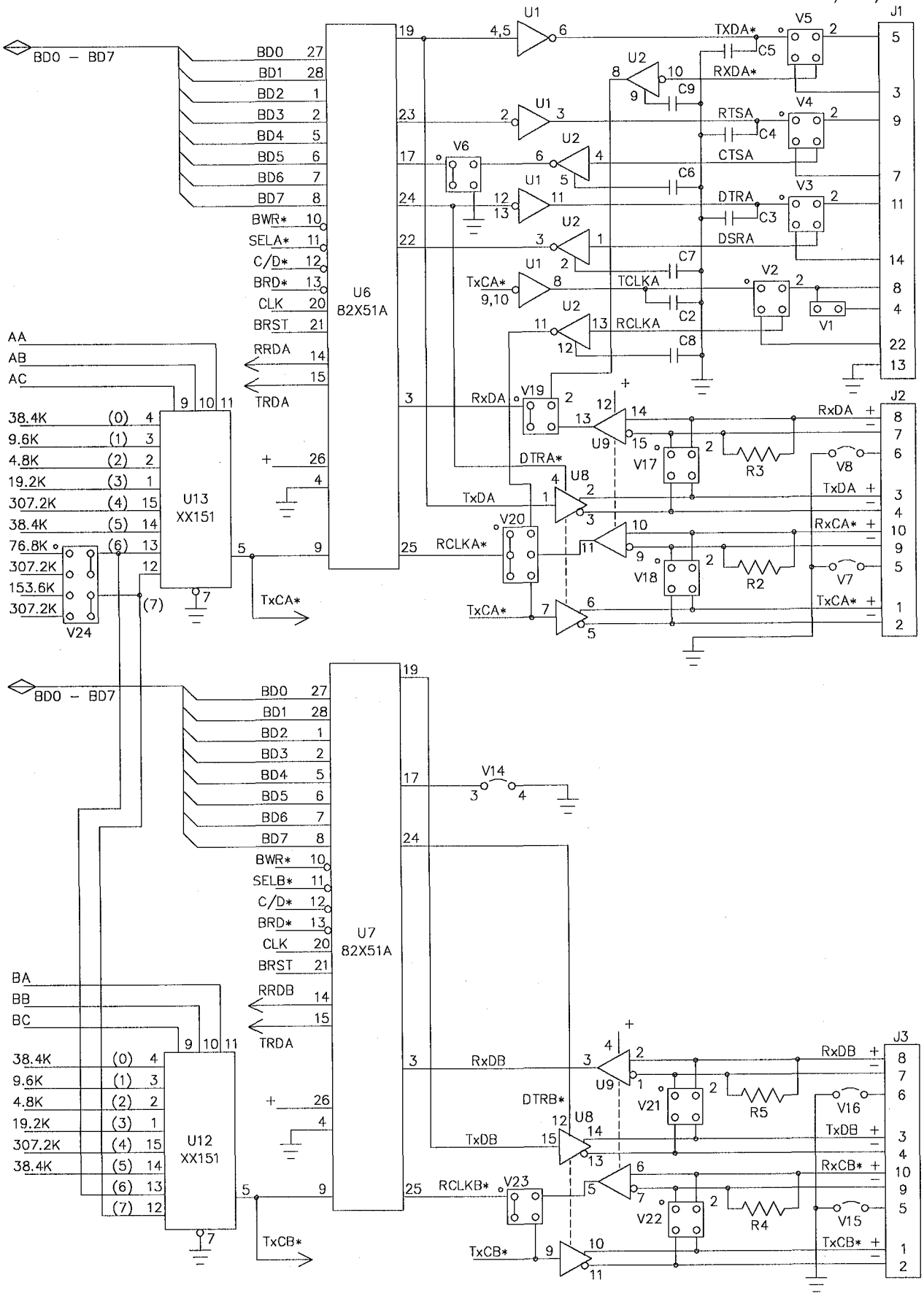
Y1	4.9152 MHz crystal

Miscellaneous

J1, J2	26 pin R/A latching header
J4	10 pin R/A header


VL-7304b REV 0
VersaLogic
J1
J2
J3
J4
V7 V8
V15 V16
V1 C2 V2 C6 V6
C20
U1 C1
U2
C10
C5 V5 C9
U5 RP1 U6
U7
C21
U8
C22
C23 V17 V13 V21
U9
V23
V20
R1
C24
V24 R2
R6
R5
Y1
C25
U10
V25
RP2
U11
U12
U13
U14
C26
C27
C28
C29
V27
U15
U16
U17
U18
U19
U20
U21
C30
C31
C32
C33
C34
C35
C36
C37
R7
V28
C38
1
55


IOEXP
IOX
U19
A9
BA9
A8
BA8
A7
A6
A5
A4
A3
U17
XX688
RP2
RP1
V25
V26
V27
BA9
BA8
RD*
IORQ*
U20
XX32
BRD*
BDSEL*
U18
XX138
A2
A1
A0
U15
XX08
SELA*
SELB*
WR*
BWR*
SYSRST*
BRST
C/D*
BRST*
PCI
PCO
LWR*
BD0 - BD7
U10
XX273
BA
BB
BC
IENB
AA
AB
AC
IENA
U16
XX245
D0
D1
D2
D3
D4
D5
D6
D7
C25
Y1
R6
R1
C24
U14
HC
4060
307.2K
153.6K
76.8K
38.4K
19.2K
9.6K
4.8K
R7
INTRQ*
TRDA
IENA
RRDA
TRDB
IENB
RRDB
U21
U5
J4
N.C.
+5V
C36
GND
C10,C20-
C23,C26-
C35
+12V
AUX GND
C38
V28
C37
-12V
C1,C11
U11
XX74
CLK


BD0 – BD7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BWR*
SELA*
C/D*
BRD*
CLK
BRST
RRDA
TRDA
U6
82X51A
AA
AB
AC
38.4K
9.6K
4.8K
19.2K
307.2K
38.4K
76.8K
307.2K
153.6K
307.2K
V24
U13
XX151
TxCA*
RCLKA*
RxDA
TxDA
DTRA*
TxCA*
U1
U2
V19
V20
U8
U9
V17
V18
R3
R2
V8
V7
TXDA*
RXDA*
RTSA
CTSA
DTRA
DSRA
TCLKA
RCLKA
C5
C9
C4
C6
C3
C7
C2
C8
V5
V4
V3
V2
V1
J1
J2
RxDA +
TxDA +
RxCA* +
TxCA* +
BA
BB
BC
BD0 – BD7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BWR*
SELB*
C/D*
BRD*
CLK
BRST
RRDB
TRDA
U7
82X51A
38.4K
9.6K
4.8K
19.2K
307.2K
38.4K
U12
XX151
TxCB*
RCLKB*
RxDB
TxDB
DTRB*
TxCB*
V14
V23
U8
U9
V21
V22
R5
R4
V16
V15
RxDB +
TxDB +
RxCB* +
TxCB* +
J3

VL-7304b PARTS LIST
Dual Channel RS-422/232 Interface

Capacitors

C1, C10, C20-C23, C26-C35	.01 uf ceramic
C2-C9	390 pf NPO ceramic
C24, C25	22 pf NPO ceramic
C36	22 uf electrolytic, radial
C37, C38	2.2 uf electrolytic, radial

Integrated Circuits

U1	1488
U2	1489A
U5, U21	74LS38
U6, U7	8251A
U8	75174
U9	75175
U10	74LS273
U11	74LS74
U12, U13	74LS151
U14	74HC4060
U15	74LS08
U16	74LS245
U17	74HCT688
U18	74LS138
U19	74LS240
U20	74LS32

Resistors

R1	200 ohm, 5%, 1/4W
R2, R3, R4, R5	100 ohm, 5%, 1/4W
R6	1M ohm, 1%, 1/4W
R7	4K7 ohm, 5%, 1/4W
RP1, RP2	10K ohm, 7 resistor SIP

Semiconductors

Y1	4.9152 MHz crystal

Miscellaneous

J1	26 pin R/A latching header
J2, J3	10 pin R/A latching header
J4	10 pin R/A header

Section 6
REFERENCE

INTRODUCTION

The reference section includes tables of information which appear elsewhere in this manual. It is repeated here for easy reference once the general operation of the board is understood.

Information on the hardware jumper options has not been included in this section. A summary of the jumper options available appears at the start of Section 2 (VL-7304a version) and Section 3 (VL-7304b version).

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications

Storage Temperature:
- VL-7304: -40° to +75° C
- VL-73CT04: -40° to +85° C

Free Air Operating Temperature:
- VL-7304: 0° to +65° C
- VL-73CT04: -40° to +85° C

Power Requirements:
- VL-7304a: 5V ±5% @ 290 ma typ.
  ±12V ±10% @ 35 ma typ.
- VL-7304b: 5V ±5% @ 460 ma typ.
  ±12V ±10% @ 18 ma typ. (if RS-232C used)
- VL-73CT04a: 5V ±10% @ 28 ma typ.
  ±12V ±10% @ 8 ma typ.

I/O Port Address	As Shipped	Read Function	Write Function
Board Address + 0	E0	-	Baud Rate Reg.
Board Address + 1	E1	Ch. B Data	Ch. B Data
Board Address + 2	E2	Ch. B Status	Ch. B Command
Board Address + 3	E3	Ch. A Data	Ch. A Data
Board Address + 4	E4	Ch. A Status	Ch. A Command
Board Address + 5	E5	-	-
Board Address + 6	E6	-	-
Board Address + 7	E7	-	-

I/O Port Locations

Baud Rate Register							
D7	D6	D5	D4	D3	D2	D1	D0
INT. CH.A	---	BAUD RATE CHANNEL A	----	INT CH.B	---	BAUD RATE CHANNEL B	----

Bit	Description
D7	Channel A Interrupt Enable 0 - Disable interrupts 1 - Enable interrupts
D6-D4	Channel A Baud Rate Select 0-7 - Per the baud rate table
D3	Channel B Interrupt Enable 0 - Disable interrupts 1 - Enable interrupts
D2-D0	Channel B Baud Rate Select 0-7 - Per the baud rate table

Baud Rate Register Format

Software Select#	(As shipped) Table 1	Table 2
0	2400	2400
1	600	600
2	300	300
3	1200	1200
4	19200	19200
5	2400	2400
6	4800	19200
7	9600	19200

16X Async Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	600	600
1	150	150
2	75	75
3	300	300
4	4800	4800
5	600	600
6	1200	4800
7	2400	4800

64X Async Mode Baud Rate Options

Software Select#	(As shipped) Table 1	Table 2
0	38400	38400
1	9600	9600
2	4800	4800
3	19200	19200
4	N/A*	N/A*
5	38400	38400
6	N/A*	N/A*
7	N/A*	N/A*

* Not available. Higher than the 60K baud limit of the serial chip (76.8K baud).

Sync Mode Baud Rate Options

Command Register

D7	D6	D5	D4	D3	D2	D1	D0
HUNT	RESET	RTS CNTL	ERROR RESET	BREAK	RECEIVE ENABLE	DTR CNTL	TRANSMIT ENABLE

Bit	Description
D7	Enter Hunt Mode (for sync. operation only) 1 - Enter Hunt mode
D6	Reset 1 - Reset chip (to receive a Mode instruction)
D5	RTS control (for RS-232 interface use only) 0 - Set RTS line low 1 - Set RTS line high (ready)
D4	Error flag reset 1 - Reset PE, OE, and FE flags
D3	Break 1 - Force transmit line high (break condition)
D2	Receive enable 0 - Disable receiver 1 - Enable receiver
D1	DTR control 0 - Set DTR line low (Enable RS-422/485 xmit driver) 1 - Set DTR line high (Disable RS-422/485 xmit driver)
D0	Transmit enable 0 - Disable transmitter 1 - Enable transmitter

Command Register Format

Status Register							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DSR	BRKDET/ SYNDET	FRAME ERROR	OVERRUN ERROR	PARITY ERROR	BUFFER EMPTY	RCVR READY	XMITR READY

Bit Description

D7 Data Set Ready
= 1 when DSR input line is high (ready).

D6 Break/sync Detect
Async: = 1 when data input line is in a break condition.
Sync: = 1 when 1 (or 2) sync characters have been detected.(2)

D5 Framing Error (async only)
= 1 when a stop bit was not detected at the end of a received character.(1)

D4 Overrun Error
= 1 when receive buffer was not read before another character was received.(1)

D3 Parity Error
= 1 when a parity error is detected.(1)

D2 Transmit Done (not normally used)
= 1 when the transmitter is actually done. Can be used with half-duplex operation to know when to turn the line around.

D1 Receiver Ready
= 1 when a character has been received and is available for reading by the system (reading the character from the data port resets this bit).

D0 Transmitter Ready
= 1 when data may be written to the transmit buffer.

Notes:
1) This error does not inhibit further operation of the interface chip. The error bit is reset using command bit D4.
2) Reading the status register resets this bit.

Status Register Format

Async Mode Instruction Format

D7	D6	D5	D4	D3	D2	D1	D0
-STOP BITS-		PARITY TYPE	PARITY ENABLE	-CHARACTER- LENGTH		BAUD CLOCK DIVISOR	

Bit	Description
D7, D6	Number of Stop Bits to Transmit* 00 - Invalid 01 - 1 bit 10 - 1 1/2 bits 11 - 2 bits
D5	Parity Type 0 - Odd 1 - Even
D4	Parity Bit Enable 0 - Disable 1 - Enable
D3, D2	Character Length (doesn't include parity bit) 00 - 5 bits 01 - 6 bits 10 - 7 bits 11 - 8 bits
D1, D0	Baud Rate Divisor 00 - (sync mode) 01 - 1X (don't use) 10 - 16X 11 - 64X

* Receiver always requires only one (or more) stop bits.

Mode Instruction Format For Asynchronous Operation

Sync Mode Instruction Format

D7	D6	D5	D4	D3	D2	D1	D0
SYNC TYPE	0	PARITY TYPE	PARITY ENABLE	CHAR. LENGTH		0	0

Bit	Description
D7	Sync Char Type 0 - Double sync character (sync requires two characters) 1 - Single sync character
D6	Sync Detect 0 - Internal sync detect 1 - External sync detect (don't use)
D5	Parity Type 0 - Odd 1 - Even
D4	Parity Bit Enable 0 - Disable 1 - Enable
D3, D2	Character Length (doesn't include parity bit) 00 - 5 bits 01 - 6 bits 10 - 7 bits 11 - 8 bits
D1, D0	00 - (Sync mode)

Mode Instruction Format For Synchronous Operation

J1/J2 Pin	Signal Name	RS-232C Pin
1	-	1
2	-	14
3	TD	2
4	(RCLK)	15
5	RD	3
6	-	16
7	RTS	4
8	RCLK	17
9	CTS	5
10	-	18
11	DSR	6
12	-	19
13	GND	7
14	DTR	20
15	-	8
16	-	21
17	-	9
18	-	22
19	-	10
20	-	23
21	-	11
22	TCLK	24
23	-	12
24	-	25
25	-	13
26	-	-

Note: These connectors can be converted to the RS-232C pinout using VersaLogic cable #9560.

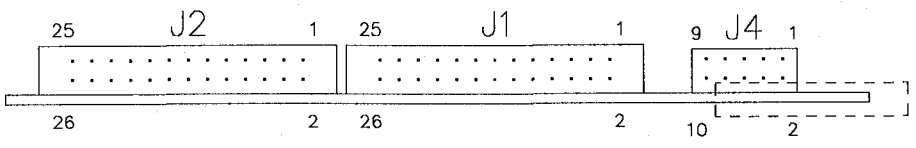
RS-232C Connector Pinouts

J2/J3 Pin	Signal Name	Direction
1	TXC+	OUT
2	TXC-	OUT
3	TXD+	OUT
4	TXD-	OUT
5	SGND	-
6	SGND	-
7	RXD-	IN
8	RXD+	IN
9	RXC-	IN
10	RXC+	IN

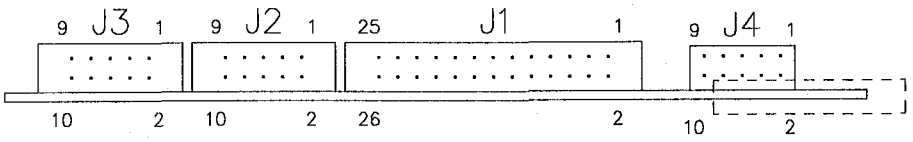
RS-422 Connector Pinouts

J4 Pin	Signal Name	Output Drive (Sink ma)
1	GND	
2	Chan. A Xmit Int.	20
3	GND	
4	Chan. A Recv Int.	20
5	GND	
6	Chan. B Xmit Int.	20
7	GND	
8	Chan. B Recv Int.	20
9	GND	
10	-	

Interrupt Connector J4



VL-7304a Connector Pin Locations



VL-7304b Connector Pin Locations

STD BUS PINOUT

Connections from the VL-7304 board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7304.

COMPONENT SIDE				SOLDER SIDE			
PIN	SIGNAL	FLOW	DESCRIPTION	PIN	SIGNAL	FLOW	DESCRIPTION
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	-	-5V or bat. backup	6	-5V	-	-5V power
7	D3/A19	I/O	Data bus	8	D7	I/O	Data bus
9	D2/A18	I/O	Data bus	10	D6	I/O	Data bus
11	D1/A17	I/O	Data bus	12	D5/A21	I/O	Data bus
13	D0/A16	I/O	Data bus	14	D4/A20	I/O	Data bus
15	A7	In	Address bus	16	A15	-	Address bus
17	A6	In	Address bus	18	A14	-	Address bus
19	A5	In	Address bus	20	A13	-	Address bus
21	A4	In	Address bus	22	A12	-	Address bus
23	A3	In	Address bus	24	A11	-	Address bus
25	A2	In	Address bus	26	A10	-	Address bus
27	A1	In	Address bus	28	A9	In	Address bus
29	A0	In	Address bus	30	A8	In	Address bus
31	WR*	In	Write strobe	32	RD*	In	Read strobe
33	IORQ*	In	I/O addr. select	34	MEMRQ*	-	Memory addr. select
35	IOEXP*	In	I/O expansion	36	MEMEX*	-	Memory expansion
37	REFRESH*	-	Refresh timing	38	MCSYNC*	-	Machine cycle sync.
39	STATUS1*	-	CPU status	40	STATUS0*	-	CPU status
41	BUSAK*	-	Bus acknowledge	42	BUSRQ*	-	Bus request
43	INTAK*	-	Interrupt acknowl.	44	INTRQ*	Out	Interrupt request
45	WAITRQ*	-	Wait request	46	NMIRQ*	-	Non-maskable interrupt
47	SYSRESET*	In	System reset	48	PBRESET*	-	Push button reset
49	CLOCK*	-	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	In	±12 volt ground	54	AUXGND	In	±12 volt ground
55	AUX+V	In	+12 volt input	56	AUX-V	In	-12 volt input

Notes:
* Denotes an active low signal.
±12V supply required only for RS-232C interface operation.

DECIMAL / HEX / ASCII CONVERSION CHART

The chart below is useful for both ASCII and decimal/hex conversion. The "^" symbol denotes control characters. "^A" represents control A, etc.

Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL	32	20		64	40	@	96	60	`
1	01	^A SOH	33	21	!	65	41	A	97	61	a
2	02	^B STX	34	22	"	66	42	B	98	62	b
3	03	^C ETX	35	23	#	67	43	C	99	63	c
4	04	^D EOT	36	24	$	68	44	D	100	64	d
5	05	^E ENQ	37	25	%	69	45	E	101	65	e
6	06	^F ACK	38	26	&	70	46	F	102	66	f
7	07	^G BEL	39	27	'	71	47	G	103	67	g
8	08	^H BS	40	28	(	72	48	H	104	68	h
9	09	^I HT	41	29	)	73	49	I	105	69	i
10	0A	^J LF	42	2A	*	74	4A	J	106	6A	j
11	0B	^K VT	43	2B	+	75	4B	K	107	6B	k
12	0C	^L FF	44	2C	,	76	4C	L	108	6C	l
13	0D	^M CR	45	2D	-	77	4D	M	109	6D	m
14	0E	^N SO	46	2E	.	78	4E	N	110	6E	n
15	0F	^O SI	47	2F	/	79	4F	O	111	6F	o
16	10	^P DLE	48	30	0	80	50	P	112	70	p
17	11	^Q DC1	49	31	1	81	51	Q	113	71	q
18	12	^R DC2	50	32	2	82	52	R	114	72	r
19	13	^S DC3	51	33	3	83	53	S	115	73	s
20	14	^T DC4	52	34	4	84	54	T	116	74	t
21	15	^U NAK	53	35	5	85	55	U	117	75	u
22	16	^V SYN	54	36	6	86	56	V	118	76	v
23	17	^W ETB	55	37	7	87	57	W	119	77	w
24	18	^X CAN	56	38	8	88	58	X	120	78	x
25	19	^Y EM	57	39	9	89	59	Y	121	79	y
26	1A	^Z SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL

Technical Note
Replacing Pro-Log's 7304 with VersaLogic's VL-7304

Although the VersaLogic VL-7304 and the Pro-Log 7304 boards are almost identical in function, there are two differences which affect plug-in replacement in existing systems. These differences are:

1) The VersaLogic board does not include a TTY (teletype) interface. Applications that require a TTY interface will not be able to use the VersaLogic board.

2) The baud rate selection tables on the VL-7304 are not identical to the Pro-Log 7304. Some of the slower baud rates have been replaced with more standard ones. Systems which require baud rates of 50, 110, or 1800 will not be able to use the VersaLogic board. Operation at 75 or 150 baud requires a change in system software.

Systems which operate at any other Pro-Log supported rate (300, 600, 1200, 2400, 4800, 9600 or 19,200 baud) can use the VersaLogic board as a direct plug-in replacement for the Pro-Log 7304.

The VL-7304 baud rate tables are shown below for reference. The Pro-Log identical rates are shown in bold.

Software Select#	Table 1	Table 2
0	**2400**	2400
1	**600**	600
2	**300**	300
3	**1200**	1200
4	19200	19200
5	**2400**	2400
6	**4800**	**19200**
7	**9600**	**19200**

Baud Rates with 16X Clock Divider

Software Select#	Table 1	Table 2
0	**600**	600
1	**150**	150
2	**75**	75
3	**300**	300
4	4800	4800
5	**600**	600
6	**1200**	**4800**
7	**2400**	**4800**

Baud Rates with 64X Clock Divider