Model VL-1225 & VL-1226
Analog Input/Output Cards for the STD Bus

REFERENCE MANUAL

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Overview

This manual details the installation and operation of VersaLogic's VL-1225 and VL-1226 analog I/O cards. The VL-1225 card includes both analog input and output channels. The VL-1226 includes the same analog input channels, but no output channels. Both cards provide 10- or 11-bit input resolution.

Introduction

In its standard configuration the VL-1225/6 provides 16 single-ended, or 8 differential analog input channels. It features 10- or 11-bit resolution, 25 µs conversion time, and an on-board DC to DC converter (requires +5 volt supply only). The board operates with an input range 0 to +10, ±5, or ±10 volts. It can accommodate input signals in a single-ended, differential, or pseudo-differential configuration.

Each input channel can be read as desired by the system CPU. The board is capable of 25,000 samples per second throughput.

In addition to the input channels noted above, the VL-1225 card includes two 8-bit analog output channels. These channels may be jumpered for 0 to +10, ±5, or ±10 volt output at 5 mA.

The VL-1225 and VL-1226 are plug-in compatible with the Analog Devices RTI-1225 and RTI-1226 cards.

Features

- 16 single-ended or 8 differential input channels.
- Two output channels (VL-1225 only).
- 10-bit (1024 counts), or 11-bit (2048 counts) input resolution.
- 8-bit output resolution (VL-1225 only).
- 25 µs input conversion time.
- 0 to +10, ±5, or ±10 volt input and output ranges.
- 16-bit memory or I/O addressing.
- MEMEX and IOEXP supported.
- +5 volt single supply operation.
- Plug-in replacement for Analog Devices RTI-1225/1226.

Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

ANALOG INPUT (VL-1225 and VL-1226)
Number of Channels: 16 single-ended or 8 differential
Range: 0 to +10V, ±5V, ±10V
Resolution:
- 10 bits (1024 counts) RTI-1225/6 Compatible Mode
- 11 bits (2048 counts) VL-1225/6 Extended Mode

Conversion Time: 25 µs + settling time
Settling Time: 15 µs
Throughput: 25,000 channels/sec
Overvoltage Protection:
- ±35V with power on
- ±20V with power off

Impedance: 1 x 108 W min.
Data Format: Binary, offset binary, or two's complement
Common Mode Voltage (CMV): ±10V min
Common Mode Rejection (CMR): 60 dB
Linearity: ±½ LSB
Differential Nonlinearity: ±½ LSB
Temperature Coefficient:
- Gain ±50 ppm/°C of FSR
- Offset ±25 ppm/°C of FSR

Addressing: 16 bits + MEMEX or IOEXP
Mapping: 8-byte memory or I/O block on any 8-byte boundary
Size: Meets all STD 32 Bus mechanical specifications
Storage Temperature: -40° to +75 °C
Free Air Operating Temperature: 0° to +65 °C
Power Requirements:
- 5V ±5% @ 480 ma typ. (VL-1225)
- 5V ±5% @ 430 ma typ. (VL-1226)

ANALOG OUTPUT (VL-1225 only)
Number of Channels: 2
Resolution: 8 bits (256 counts)
Data Format: Binary, offset binary, or two's complement
Range: 0 to +10V, ±5V, ±10V
Settling Time: 25 µs (to ±½ LSB)
Linearity: ±½ LSB
Differential Nonlinearity: ±½ LSB
Temperature Coefficient:
- Gain ±50 ppm/°C of FSR
- Offset ±30 µV/°C

BUS COMPATIBILITY (VL-1225 and VL1226)
STD 80: Full compliance, all bus speeds
STD Z80: Full compliance, all bus speeds
STD 32: I/O slave, SA8-I, IXP

Configuration

Jumper Options

Various options available on the VL-1225/6 cards are selected using removable jumper blocks (shorting plugs). Features are selected or deselected by installing or removing the jumpers as noted. The terms "In" or "Jumpered" are used to indicate an installed plug: "Out" or "Open" are used to indicate a removed plug.

Figure 2-1 shows the jumper block locations on the VL-1225 card. Figure 2-3 shows the jumper block locations on the VL-1226 card. The figures indicate the position of the jumpers as shipped from the factory.

VL-1225 Jumper Block Locations

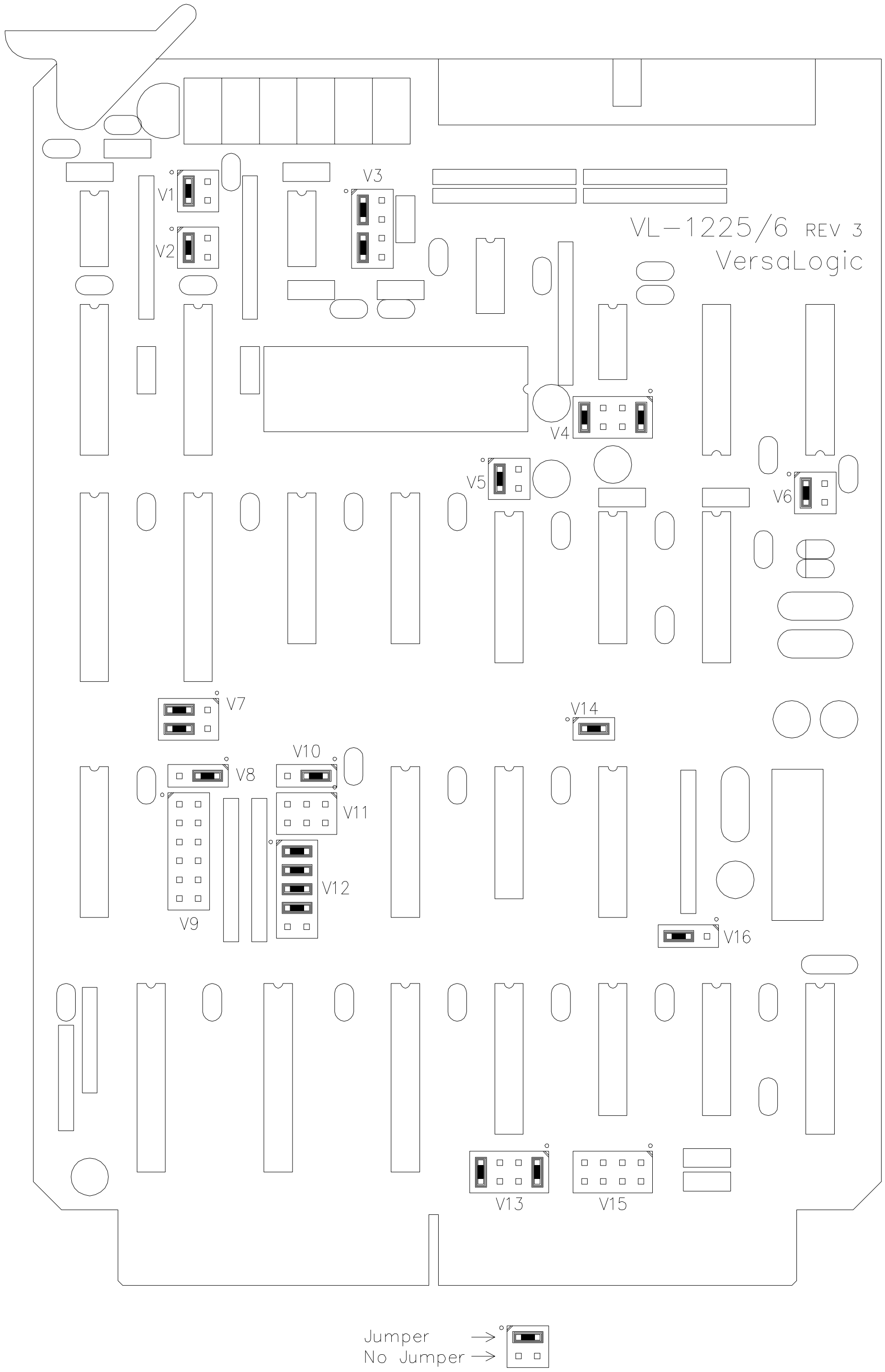


Figure 2-1. Jumper Block Locations for VL-1225

VL-1225 Jumper Options

Jumper Block	Description	As Shipped	Page
V1	Channel 0 Output Voltage Range (see also V16)	±10V	2-18
	$V1_{1-3}$ = In, $V1_{2-4}$ = In – ±5V		
	$V1_{1-3}$ = In, $V1_{2-4}$ = Out – ±10V		
	$V1_{1-3}$ = Out, $V1_{2-4}$ = In – 0 to 10V		
V2	Channel 1 Output Voltage Range (see also V16)	±10V	2-18
	$V2_{1-3}$ = In, $V2_{2-4}$ = In – ±5V		
	$V2_{1-3}$ = In, $V2_{2-4}$ = Out – ±10V		
	$V2_{1-3}$ = Out, $V2_{2-4}$ = In – 0 to 10V		
V3	Input Voltage Range Select	±10V	2-16
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – ±5V		
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = In, $V3_{6-8}$ = Out – ±10V		
	$V3_{1-3}$ = Out, $V3_{2-4}$ = In, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – 0 to 10V		
V4 & V6	Input Mode	S.E.	2-13
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = Out, $V4_{7-8}$ = In, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Single Ended		
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = In, $V4_{7-8}$ = Out, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Pseudo-Differential		
	$V4_{1-2}$ = Out, $V4_{3-4}$ = In, $V4_{5-6}$ = Out, $V4_{7-8}$ = Out, $V6_{1-2}$ = Out, $V6_{3-4}$ = In – Differential		
V5	Input Data Format	2's Comp.	2-17
	$V5_{1-3}$ = Out, $V5_{2-4}$ = In – Binary / Offset Binary		
	$V5_{1-3}$ = In, $V5_{2-4}$ = Out – Two's Complement		
$V7_{1-3\&3-5}$	Channel 0 Output Data Format	2's Comp.	2-19
	$V7_{1-3}$ = In, $V7_{3-5}$ = Out – Binary / Offset Binary		
	$V7_{1-3}$ = Out, $V7_{3-5}$ = In – Two's Complement		
$V7_{2-4\&4-6}$	Channel 1 Output Data Format	2's Comp.	2-19
	$V7_{2-4}$ = In, $V7_{4-6}$ = Out – Binary / Offset Binary		
	$V7_{2-4}$ = Out, $V7_{4-6}$ = In – Two's Complement		
V8	MEMEX Select	Ignore	2-12
	$V8_{1-2}$ = In, $V8_{2-3}$ = Out – Ignore MEMEX		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = Out – Enable on MEMEX high		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = In – Enable on MEMEX low		
V9	Board Address (A10 – A15)	FF08H	2-6
	$V9_{1-2}$ = In – A15 decoded Low; $V9_{1-2}$ = Out – A15 decoded High		
	$V9_{3-4}$ = In – A14 decoded Low; $V9_{3-4}$ = Out – A14 decoded High		
	$V9_{5-6}$ = In – A13 decoded Low; $V9_{5-6}$ = Out – A13 decoded High		
	$V9_{7-8}$ = In – A12 decoded Low; $V9_{7-8}$ = Out – A12 decoded High		
	$V9_{9-10}$ = In – A11 decoded Low; $V9_{9-10}$ = Out – A11 decoded High		
	$V9_{11-12}$ = In – A10 decoded Low; $V9_{11-12}$ = Out – A10 decoded High		
V10	IOEXP Select	Ignore	2-10
	$V10_{1-2}$ = In, $V10_{2-3}$ = Out – Ignore IOEXP		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = Out – Enable on IOEXP high		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = In – Enable on IOEXP low		
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi	2-6
	$V11_{1-3}$ = In, $V11_{2-4}$ = In, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 8-Bit Mode (ignore A8 & A9)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = High, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = High, A9 = Low)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = Low, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = Low, A9 = Low)		
V12	Board Address (A3 – A7)	FF08H	2-6
	$V12_{1-2}$ = In – A7 decoded Low; $V12_{1-2}$ = Out – A7 decoded High		
	$V12_{3-4}$ = In – A6 decoded Low; $V12_{3-4}$ = Out – A6 decoded High		
	$V12_{5-6}$ = In – A5 decoded Low; $V12_{5-6}$ = Out – A5 decoded High		
	$V12_{7-8}$ = In – A4 decoded Low; $V12_{7-8}$ = Out – A4 decoded High		
	$V12_{9-10}$ = In – A3 decoded Low; $V12_{9-10}$ = Out – A3 decoded High		
V13	Address Type Select	Memory	2-6
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit Memory Mapped		
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = In, $V13_{7-8}$ = Out – 8- or 10-Bit I/O Mapped		
	$V13_{1-2}$ = Out, $V13_{3-4}$ = In, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit I/O Mapped		
V14	Analog Input Resolution	10-Bit	2-16
	V14 = In – 10-Bit; V14 = Out – 11-Bit		
V15	Interrupt Request Select	None	2-21
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – None		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = In – INT2* (P50)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = In, $V15_{7-8}$ = Out – INT1* (P37)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = In, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – INT* (P44)		
	$V15_{1-2}$ = In, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – IRQx (E47)		
V16	D/A Power-Up Output Voltage	RTI-1225	2-20
	$V16_{1-2}$ = In, $V16_{2-3}$ = Out – Zero Volts (in Two's Complement/Bipolar, and Binary/Unipolar modes)		
	– Negative Full Scale (in Offset Binary/Bipolar mode)		
	$V16_{1-2}$ = Out, $V16_{2-3}$ = In – Zero Volts (in Offset Binary/Bipolar mode)		
	– Negative Full Scale (in Two's Complement/Bipolar mode)		
	– Half Scale (in Binary/Unipolar mode)		

Figure 2-2. VL-1225 Jumper Functions

VL-1226 Jumper Block Locations

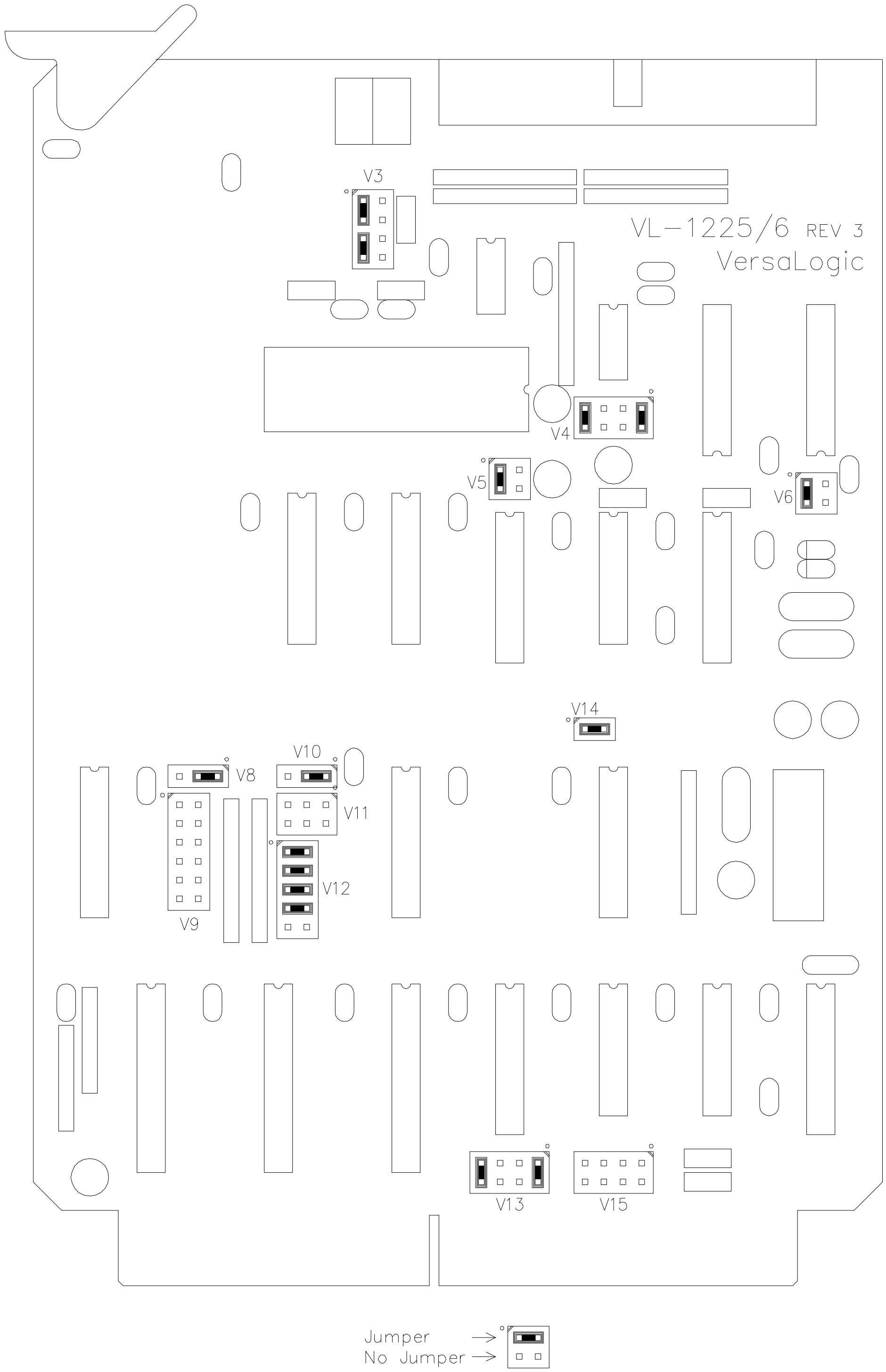


Figure 2-3. Jumper Block Locations for VL-1226

VL-1226 Jumper Options

Jumper Block	Description	As Shipped	Page
V1	1225 Only	—	—
V2	1225 Only	—	—
V3	Input Voltage Range Select	±10V	2-16
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – ±5V		
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = In, $V3_{6-8}$ = Out – ±10V		
	$V3_{1-3}$ = Out, $V3_{2-4}$ = In, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – 0 to 10V		
V4 & V6	Input Mode	S.E.	2-13
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = Out, $V4_{7-8}$ = In, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Single Ended		
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = In, $V4_{7-8}$ = Out, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Pseudo-Differential		
	$V4_{1-2}$ = Out, $V4_{3-4}$ = In, $V4_{5-6}$ = Out, $V4_{7-8}$ = Out, $V6_{1-2}$ = Out, $V6_{3-4}$ = In – Differential		
V5	Input Data Format	2's Comp.	2-17
	$V5_{1-3}$ = Out, $V5_{2-4}$ = In – Binary / Offset Binary		
	$V5_{1-3}$ = In, $V5_{2-4}$ = Out – Two's Complement		
V7	1225 Only	—	—
V8	MEMEX Select	Ignore	2-12
	$V8_{1-2}$ = In, $V8_{2-3}$ = Out – Ignore MEMEX		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = Out – Enable on MEMEX high		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = In – Enable on MEMEX low		
V9	Board Address (A10 – A15)	FF08H	2-6
	$V9_{1-2}$ = In – A15 decoded Low; $V9_{1-2}$ = Out – A15 decoded High		
	$V9_{3-4}$ = In – A14 decoded Low; $V9_{3-4}$ = Out – A14 decoded High		
	$V9_{5-6}$ = In – A13 decoded Low; $V9_{5-6}$ = Out – A13 decoded High		
	$V9_{7-8}$ = In – A12 decoded Low; $V9_{7-8}$ = Out – A12 decoded High		
	$V9_{9-10}$ = In – A11 decoded Low; $V9_{9-10}$ = Out – A11 decoded High		
	$V9_{11-12}$ = In – A10 decoded Low; $V9_{11-12}$ = Out – A10 decoded High		
V10	IOEXP Select	Ignore	2-10
	$V10_{1-2}$ = In, $V10_{2-3}$ = Out – Ignore IOEXP		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = Out – Enable on IOEXP high		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = In – Enable on IOEXP low		
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi	2-6
	$V11_{1-3}$ = In, $V11_{2-4}$ = In, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 8-Bit Mode (ignore A8 & A9)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = High, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = High, A9 = Low)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = Low, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = Low, A9 = Low)		
V12	Board Address (A3 – A7)	FF08H	2-6
	$V11_{1-2}$ = In – A7 decoded Low; $V11_{1-2}$ = Out – A7 decoded High		
	$V11_{3-4}$ = In – A6 decoded Low; $V11_{3-4}$ = Out – A6 decoded High		
	$V11_{5-6}$ = In – A5 decoded Low; $V11_{5-6}$ = Out – A5 decoded High		
	$V11_{7-8}$ = In – A4 decoded Low; $V11_{7-8}$ = Out – A4 decoded High		
	$V11_{9-10}$ = In – A3 decoded Low; $V11_{9-10}$ = Out – A3 decoded High		
V13	Address Type Select	Memory	2-6
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit Memory Mapped		
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = In, $V13_{7-8}$ = Out – 8- or 10-Bit I/O Mapped		
	$V13_{1-2}$ = Out, $V13_{3-4}$ = In, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit I/O Mapped		
V14	Analog Input Resolution	10-Bit	2-16
	V14 = In – 10-Bit; V14 = Out – 11-Bit		
V15	Interrupt Request Select	None	2-21
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – None		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = In – INT2* (P50)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = In, $V15_{7-8}$ = Out – INT1* (P37)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = In, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – INT* (P44)		
	$V15_{1-2}$ = In, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – IRQx (E47)		
V16	1225 Only	—	—

Figure 2-4. VL-1226 Jumper Functions

Board Addressing

The VL-1225/6 supports 8-, 10-, and 16-bit I/O addressing, and 16-bit memory addressing. 8-bit I/O addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10- or 16-bit addressing can be used with 16-bit processors (8088, 80188, 80186, etc.) to decode 1024 or 65536 I/O port addresses. 16-bit memory addressing can be used with most 8-bit processors (Z80, 8085, 6809, etc.) if desired.

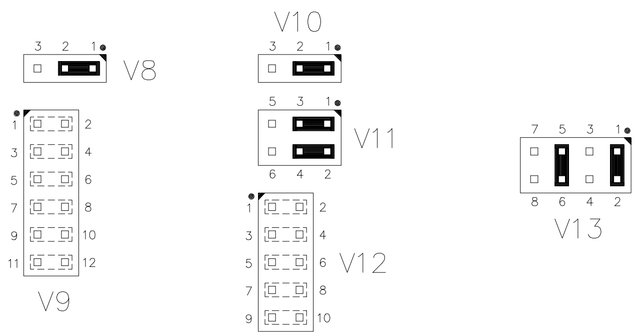
I/O addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-1225/6. Memory addressing can be extended (capacity doubled) using the MEMEX signal which is decoded by the VL-1225/6.

As shipped the board is configured for 16-bit memory addressing with a board address of hex FF08. The card occupies eight consecutive addresses (i.e. FF08H to FF0FH). The VL-1226 uses four of these addresses as control, data, and status registers, the remaining four are inaccessible. The VL-1225 uses six addresses, with two inaccessible. See the Register Mapping section on page 4-1 for further information.

8-Bit I/O Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e., "3" and "0" = hex address 30).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-10.



$V12_{1-2}$	$V12_{3-4}$	$V12_{5-6}$	$V12_{7-8}$	Upper Digit		$V12_{9-10}$	Lower Digit
X	X	X	X	0		X	0
X	X	X	–	1		–	8
X	X	–	X	2			
X	X	–	–	3			
X	–	X	X	4			
X	–	X	–	5			
	X	–	–	X	6		
	X	–	–	–	7		
	–	X	X	X	8		
	–	X	X	–	9		
	–	X	–	X	A		
	–	X	–	–	B		
	–	–	X	X	C		
	–	–	X	–	D		
	–	–	–	X	E		
	–	–	–	–	F		

X = Jumper installed
– = Jumper removed

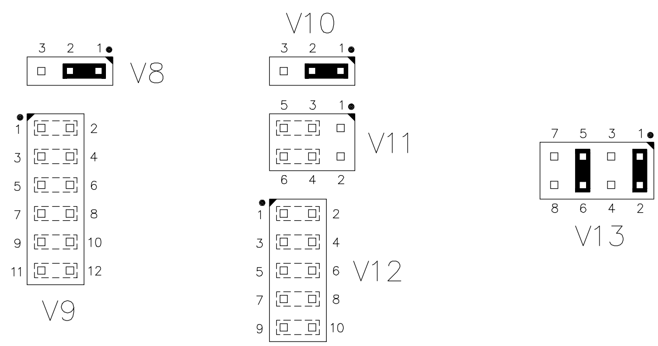
Jumper Block	Description	As Shipped
V8	MEMEX Select	Ignore
V9	Board Address (A10 – A15)	FF08H
V10	IOEXP Select	Ignore
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi
V12	Board Address (A3 – A7)	FF08H
V13	Address Type Select	Memory

Figure 2-5. 8-Bit I/O Address Jumpers

10-Bit I/O Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired starting address (i.e., "1" and "3" and "0" = hex address 130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-10.



$V11_{3-5}$	$V11_{4-6}$	Upper Digit
X	X	0
X	–	1
–	X	2
–	–	3

$V12_{1-2}$	$V12_{3-4}$	$V12_{5-6}$	$V12_{7-8}$	Middle Digit
X	X	X	X	0
X	X	X	–	1
X	X	–	X	2
X	X	–	–	3
X	–	X	X	4
X	–	X	–	5
X	–	–	X	6
X	–	–	–	7
–	X	X	X	8
–	X	X	–	9
–	X	–	X	A
–	X	–	–	B
–	–	X	X	C
–	–	X	–	D
–	–	–	X	E
–	–	–	–	F

$V12_{9-10}$	Lower Digit
X	0
–	8

X = Jumper installed
– = Jumper removed

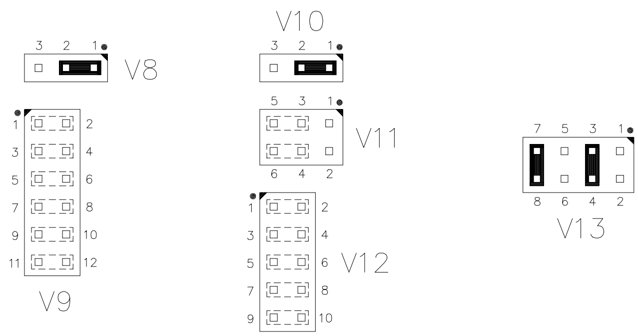
Jumper Block	Description	As Shipped
V8	MEMEX Select	Ignore
V9	Board Address (A10 – A15)	FF08H
V10	IOEXP Select	Ignore
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi
V12	Board Address (A3 – A7)	FF08H
V13	Address Type Select	Memory

Figure 2-6. 10-Bit I/O Address Jumpers

16-Bit I/O Addressing

To configure the board for a 16-bit I/O address refer to the figure below. See the table to select the jumpering for the appropriate four hex digits of the desired starting address (i.e., "6" and "1" and "3" and "0" = hex address 6130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-10.



$V9_{1\text{-}2}$	$V9_{3\text{-}4}$	$V9_{5\text{-}6}$	$V9_{7\text{-}8}$	Upper Digit	$V9_{9\text{-}10}$	$V9_{11\text{-}12}$	$V11_{3\text{-}5}$	$V11_{4\text{-}6}$	Second Digit	$V12_{1\text{-}2}$	$V12_{3\text{-}4}$	$V12_{5\text{-}6}$	$V12_{7\text{-}8}$	Third Digit	$V12_{9\text{-}10}$	Lower Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	–	1	X	X	X	–	1	X	X	X	–	1	–	8
X	X	–	X	2	X	X	–	X	2	X	X	–	X	2		
X	X	–	–	3	X	X	–	–	3	X	X	–	–	3		
X	–	X	X	4	X	–	X	X	4	X	–	X	X	4		
X	–	X	–	5	X	–	X	–	5	X	–	X	–	5		
X	–	–	X	6	X	–	–	X	6	X	–	–	X	6		
X	–	–	–	7	X	–	–	–	7	X	–	–	–	7		
–	X	X	X	8	–	X	X	X	8	–	X	X	X	8		
–	X	X	–	9	–	X	X	–	9	–	X	X	–	9		
–	X	–	X	A	–	X	–	X	A	–	X	–	X	A		
–	X	–	–	B	–	X	–	–	B	–	X	–	–	B		
–	–	X	X	C	–	–	X	X	C	–	–	X	X	C		
–	–	X	–	D	–	–	X	–	D	–	–	X	–	D		
–	–	–	X	E	–	–	–	X	E	–	–	–	X	E		
–	–	–	–	F	–	–	–	–	F	–	–	–	–	F		

X = Jumper installed
– = Jumper removed

Jumper Block	Description	As Shipped
V8	MEMEX Select	Ignore
V9	Board Address (A10 – A15)	FF08H
V10	IOEXP Select	Ignore
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi
V12	Board Address (A3 – A7)	FF08H
V13	Address Type Select	Memory

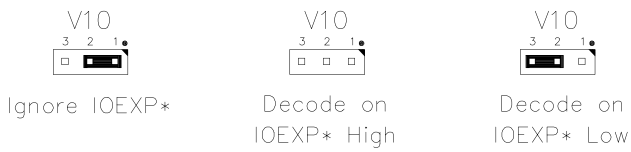
Figure 2-7. 16-Bit I/O Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown below.



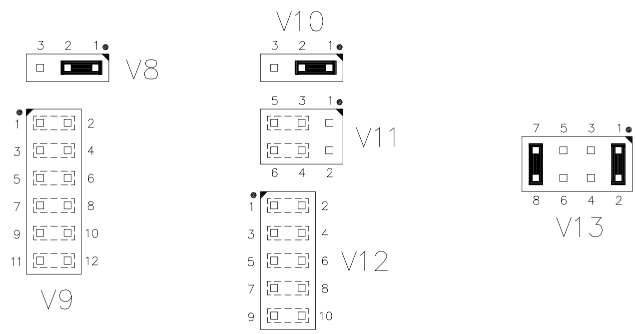
Jumper Block	Description			As Shipped
V10	IOEXP Select			Ignore
	$V10_{1-2}$ = In,	$V10_{2-3}$ = Out	– Ignore IOEXP	
	$V10_{1-2}$ = Out,	$V10_{2-3}$ = Out	– Enable on IOEXP high	
	$V10_{1-2}$ = Out,	$V10_{2-3}$ = In	– Enable on IOEXP low	

Figure 2-8. IOEXP Options

16-Bit Memory Addressing

To configure the board for a 16-bit memory address refer to the figure below. Use the table to select the jumpering for the appropriate four hex digits of the desired starting address (i.e., “6” and “1” and “3” and “0” = hex address 6130).

This jumper configuration ignores the state of the MEMEX signal in addressing the board. To use the MEMEX signal refer to the MEMEX Signal heading in this section.



$V9_{1\text{-}2}$	$V9_{3\text{-}4}$	$V9_{5\text{-}6}$	$V9_{7\text{-}8}$	Upper Digit	$V9_{9\text{-}10}$	$V9_{11\text{-}12}$	$V11_{3\text{-}5}$	$V11_{4\text{-}6}$	Second Digit	$V12_{1\text{-}2}$	$V12_{3\text{-}4}$	$V12_{5\text{-}6}$	$V12_{7\text{-}8}$	Third Digit	$V12_{9\text{-}10}$	Lower Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	–	1	X	X	X	–	1	X	X	X	–	1	–	8
X	X	–	X	2	X	X	–	X	2	X	X	–	X	2		
X	X	–	–	3	X	X	–	–	3	X	X	–	–	3		
X	–	X	X	4	X	–	X	X	4	X	–	X	X	4		
X	–	X	–	5	X	–	X	–	5	X	–	X	–	5		
X	–	–	X	6	X	–	–	X	6	X	–	–	X	6		
X	–	–	–	7	X	–	–	–	7	X	–	–	–	7		
–	X	X	X	8	–	X	X	X	8	–	X	X	X	8		
–	X	X	–	9	–	X	X	–	9	–	X	X	–	9		
–	X	–	X	A	–	X	–	X	A	–	X	–	X	A		
–	X	–	–	B	–	X	–	–	B	–	X	–	–	B		
–	–	X	X	C	–	–	X	X	C	–	–	X	X	C		
–	–	X	–	D	–	–	X	–	D	–	–	X	–	D		
–	–	–	X	E	–	–	–	X	E	–	–	–	X	E		
–	–	–	–	F	–	–	–	–	F	–	–	–	–	F		

X = Jumper installed
– = Jumper removed

Jumper Block	Description	As Shipped
V8	MEMEX Select	Ignore
V9	Board Address (A10 – A15)	FF08H
V10	IOEXP Select	Ignore
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi
V12	Board Address (A3 – A7)	FF08H
V13	Address Type Select	Memory

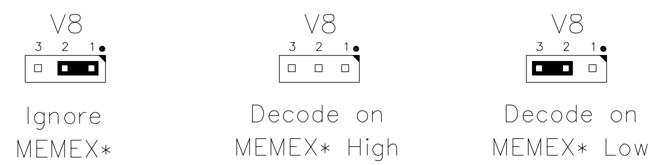
Figure 2-9. 16-Bit Memory Address Jumpers

MEMEX Signal

The MEMEX (memory expansion) signal on the STD Bus is normally used to select between two different memory banks or maps. It can be used to double the number of available memory addresses in the system (by selecting between the two memory banks). The MEMEX signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low MEMEX signal usually selects the standard or normal memory map. A high MEMEX signal usually selects the secondary or alternate memory map. Boards that ignore (or do not decode) MEMEX will appear in both memory maps.

As shipped the MEMEX jumper is configured to ignore the MEMEX signal. The board will be addressed whether the MEMEX signal is high or low. It can be jumpered for two other modes as shown below.



Jumper Block	Description			As Shipped
V8	MEMEX Select			Ignore
	$V8_{1\text{-}2}$ = In,	$V8_{2\text{-}3}$ = Out	– Ignore MEMEX	
	$V8_{1\text{-}2}$ = Out,	$V8_{2\text{-}3}$ = Out	– Enable on MEMEX high	
	$V8_{1\text{-}2}$ = Out,	$V8_{2\text{-}3}$ = In	– Enable on MEMEX low	

Figure 2-10. MEMEX Options

Analog Input Configuration

The VL-1225/6 board accommodates 16 single-ended or 8 differential channels.

Input Mode

The VL-1225/6 board can be configured for three types of voltage inputs: differential, single-ended, and pseudo-differential. In addition, by adding an external user-supplied 500 W resistor, the VL-1225/6 can be hooked up to a 4-20 ma current loop. All inputs connected to the boards must be of the same type.

Typical connections for the three input modes are shown in the figures below. Since ground loops (current flowing between various equipment ground lines) affect analog measurements made with reference to ground, careful attention should be paid to the ground connections shown. In particular, the STD Bus power supply logic ground line should never be connected to earth ground when operating in the differential or pseudo-differential modes.

Single Ended Mode

The single-ended mode is used for signals that are referenced to a common ground. It is normally used only for higher level signals on short distance runs (less than 10 feet). In this mode up to 16 input channels can be accommodated.

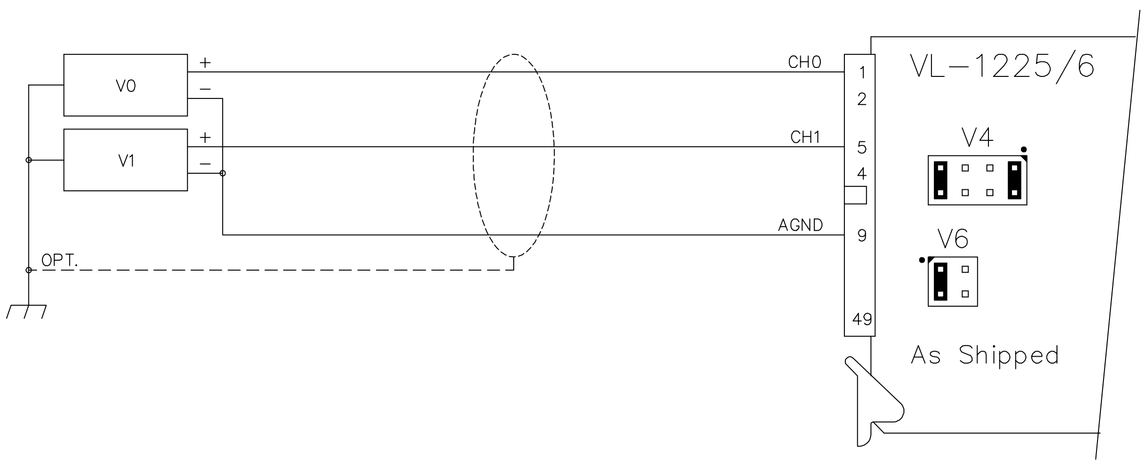


Figure 2-11. Single Ended Input Mode

Pseudo-Differential Mode

The pseudo-differential mode is used for signals that are not referenced to ground, but are all connected to a single common return line. This mode can provide most of the advantages of full differential input while requiring fewer total wires. In the pseudo-differential mode, 16 input channels can be accommodated.

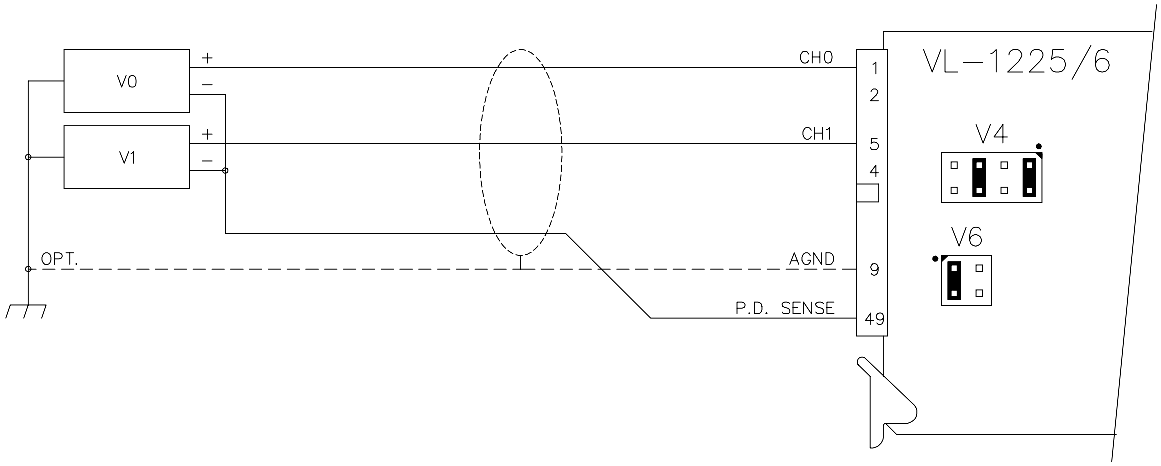


Figure 2-12. Pseudo-Differential Input Mode

Differential Mode

The differential mode is used for signals that are not referenced to a common or ground point, but simply have a voltage difference between the two input wires (usually a twisted pair). It is desirable to use the differential mode in electrically noisy environments since it reduces the effects of electromagnetically induced noise and ground currents. It is especially useful in eliminating the effects of common mode noise generated on input lines over longer distances. In the differential mode, only eight input channels are available.

Note that in full differential operation a return path must be provided for the bias currents of the input amplifier. This can be accomplished by grounding the voltage source power supply(s) to the VL-1225/6 board, or by installing a 10K to 100K W resistor as shown for each channel. These resistors should be located in close proximity to the voltage source.

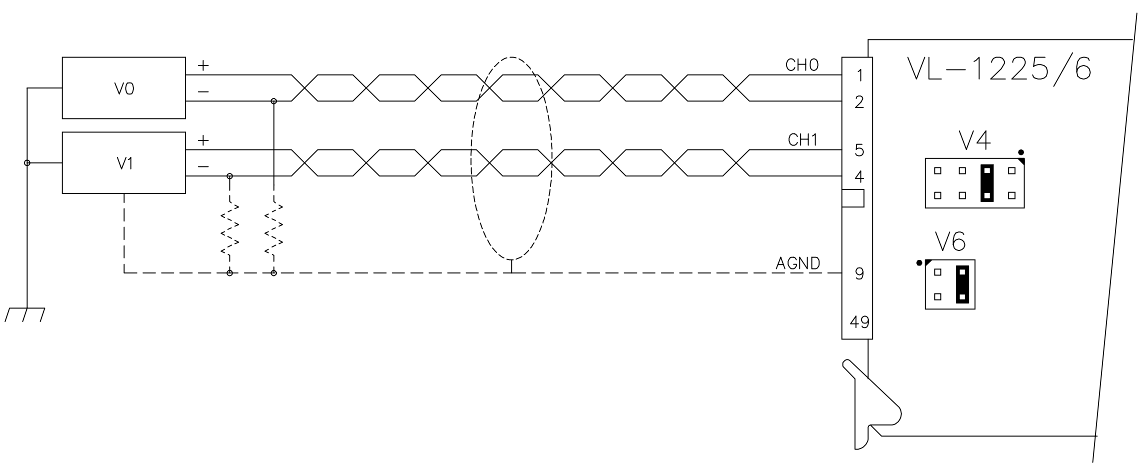


Figure 2-13. Differential Input Mode

Current Loop Mode

While the VL-1225/6 cannot directly hook up to a 4-20 ma current loop, the addition of an external user-supplied 500 W precision dropping resistor can be used to develop a 2-10 volt signal proportional to the 4-20 ma current. This voltage is applied to the VL-1225/6 as a differential-mode signal. The input range should be jumpered for unipolar 0 to 10V operation. The circuit below can be repeated for all 8 differential input channels.

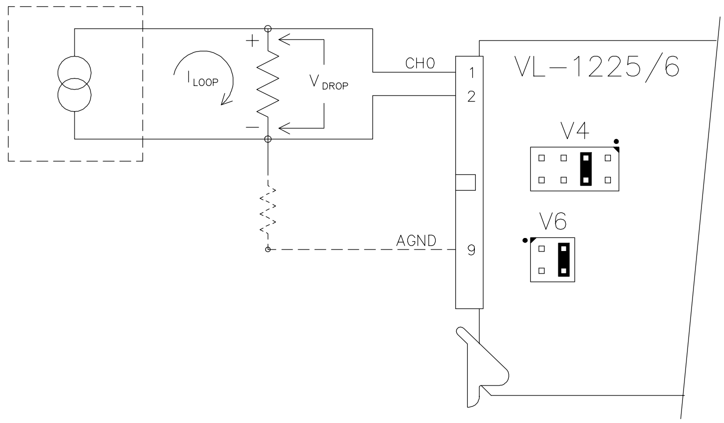
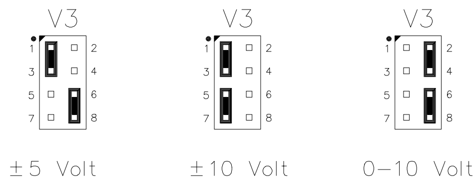


Figure 2-14. Current Loop Input Mode

Input Voltage Range

The board may be operated with an input range of 0 to +10 volts, ±10 volts, or ±5 volts. The 0 to +10 volt range is preferred for signals which do not go negative, since the per volt resolution is twice that of the ±10 volt range. If the input signals do not exceed ±5 volts, the ±5 volt range is preferred for the same reason. Input voltage range selection applies to all input channels.

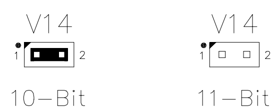


Jumper Block	Description					As Shipped
V3	Input Voltage Range Select					±10V
	$V3_{1-3}$ = In,	$V3_{2-4}$ = Out,	$V3_{5-7}$ = Out,	$V3_{6-8}$ = In	– ±5V	
	$V3_{1-3}$ = In,	$V3_{2-4}$ = Out,	$V3_{5-7}$ = In,	$V3_{6-8}$ = Out	– ±10V	
	$V3_{1-3}$ = Out,	$V3_{2-4}$ = In,	$V3_{5-7}$ = Out,	$V3_{6-8}$ = In	– 0 to 10V	

Figure 2-15. Input Range Selection

Input Resolution

The A/D converter can be jumpered to provide 10 bits or 11 bits of resolution. 10-bit mode is used for compatibility with Analog Devices RTI-1225/6 boards, it provides 1024 digital counts. 11-bit mode provides 2048 counts for applications which require twice the resolution. Input resolution applies to all input channels.



Jumper Block	Description		As Shipped
V14	Analog Input Resolution		10-Bit
	V14 = In	– 10-Bit	
	V14 = Out	– 11-Bit	

Figure 2-16. Input Range Selection

Input Data Format

The digital data format for the analog input channels can be jumpered for binary, offset binary, or two's complement. The configuration affects all channels.

The selection is dependent upon the input voltage range selected with jumper V3. Unipolar voltages should use the binary data format. Bipolar voltages can use two's complement or offset binary formats, however, two's complement is is the best choice since it "maps" the positive and negative voltages into positive and negative digital values.

See the Input Data Representation section starting on page 4-4 for further information on the various analog input data formats.

Input Range	Valid Input Data Formats
0 to +10V	Binary
±10V	Offset Binary or Two's Complement
±5V	Offset Binary or Two's Complement

Figure 2-17. Valid Input Data Formats

Jumper Block	Description			As Shipped
V5	Input Data Format			2's Complement
	$V5_{1\text{-}3}$ = In,	$V5_{2\text{-}4}$ = Out	– Two's Complement	
	$V5_{1\text{-}3}$ = Out,	$V5_{2\text{-}4}$ = In	– Binary / Offset Binary	

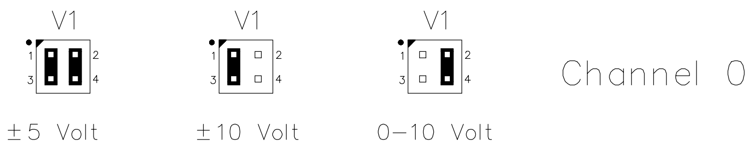
Figure 2-18. Input Data Format Options

Analog Output Configuration

The VL-1225 board accommodates two analog output channels. Both output channels are single-ended and are referenced to analog ground.

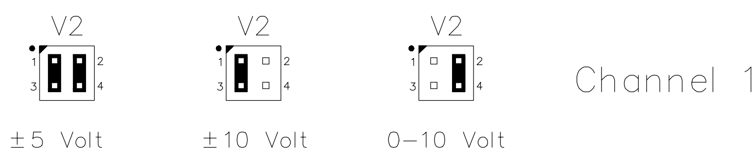
Output Voltage Range

Each output channel can be configured independently to produce output voltage ranges of 0 to +10 volts, ±5 volts, or ±10 volts as shown below.



Jumper Block	Description	As Shipped
V1	Channel 0 Output Voltage Range	±10V
	$V1_{1\text{-}3}$ = In, $V1_{2\text{-}4}$ = In – ±5V $V1_{1\text{-}3}$ = In, $V1_{2\text{-}4}$ = Out – ±10V $V1_{1\text{-}3}$ = Out, $V1_{2\text{-}4}$ = In – 0 to 10V	

Figure 2-19. Channel 0 Output Voltage Range



Jumper Block	Description	As Shipped
V2	Channel 1 Output Voltage Range	±10V
	$V2_{1\text{-}3}$ = In, $V2_{2\text{-}4}$ = In – ±5V $V2_{1\text{-}3}$ = In, $V2_{2\text{-}4}$ = Out – ±10V $V2_{1\text{-}3}$ = Out, $V2_{2\text{-}4}$ = In – 0 to 10V	

Figure 2-20. Channel 1 Output Voltage Range

Output Data Format

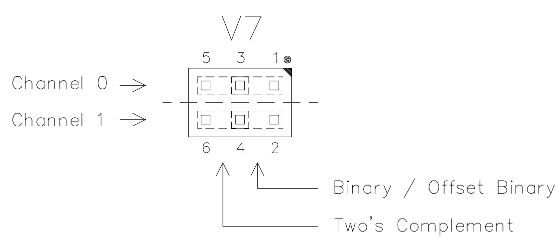
The digital data format for the analog output channels can be jumpered for binary, offset binary, or two's complement. Each channel can be configured independently.

The selection is dependent upon the output voltage range selected with jumpers V1 and V2. Unipolar voltages should use the binary data format. Bipolar voltages can use two's complement or offset binary formats, however, two's complement is the best choice since it "maps" the positive and negative digital values into positive and negative voltages.

See the Output Data Representation section starting on page 4-10 for further information on the various analog output data formats.

Output Range	Valid Output Data Formats
±5V	Offset Binary or Two's Complement
±10V	Offset Binary or Two's Complement
0 to +10V	Binary

Figure 2-21. Valid Output Data Formats

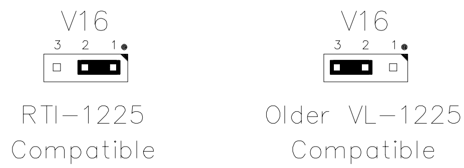


Jumper Block	Description			As Shipped
$V7_{1\text{-}3\&3\text{-}5}$	Channel 0 Output Data Format			2's Comp.
	$V7_{1\text{-}3}$ = Out,	$V7_{3\text{-}5}$ = In	– Two's Complement	
	$V7_{1\text{-}3}$ = In,	$V7_{3\text{-}5}$ = Out	– Binary / Offset Binary	
$V7_{2\text{-}4\&4\text{-}6}$	Channel 1 Output Data Format			2's Comp.
	$V7_{2\text{-}4}$ = Out,	$V7_{4\text{-}6}$ = In	– Two's Complement	
	$V7_{2\text{-}4}$ = In,	$V7_{4\text{-}6}$ = Out	– Binary / Offset Binary	

Figure 2-22. Output Data Format Options

Output Power-Up Voltage

Jumper V16 is provided to force the output voltage of both channels to zero volts when the VL-1225 powers up or the CPU is reset. The jumper position is dependent upon the output range and output data format. Refer to the table below for the proper configuration.



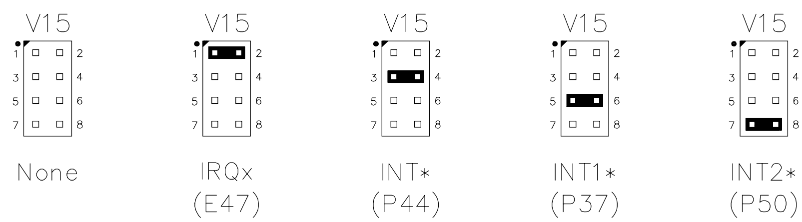
Jumper Block	Description			As Shipped
V16	D/A Power-Up Output Voltage			RTI-1225 Compatible
	$V16_{1-2}$ = In,	$V16_{2-3}$ = Out	– Zero Volts (in Two's Complement/Bipolar, and Binary/Unipolar modes) – Negative Full Scale (in Offset Binary/Bipolar mode)	
	$V16_{1-2}$ = Out,	$V16_{2-3}$ = In	– Zero Volts (in Offset Binary/Bipolar mode) – Negative Full Scale (in Two's Complement/Bipolar mode) – Half Scale (in Binary/Unipolar mode)	

Figure 2-23. Output Power-Up Voltage

Interrupt Configuration

Jumper V15 connects the interrupt request signal from the VL-1225/6 card to one of four STD Bus interrupt request lines. The choice of which jumper position to choose depends upon the capabilities of the CPU or interrupt controller used in the system.

If an STD 32 Slot X interrupt controller is used, interrupts are requested on the dedicated slot specific signal IRQx (E47).



Jumper Block	Description	As Shipped
V15	Interrupt Request Select	None
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – None	
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = In – INT2* (P50)	
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = In, $V15_{7-8}$ = Out – INT1* (P37)	
	$V15_{1-2}$ = Out, $V15_{3-4}$ = In, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – INT* (P44)	
	$V15_{1-2}$ = In, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – IRQx (E47)	

Figure 2-24. Interrupt Configuration Options

Installation

Handling

CAUTION: The VL-1225/6 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

Installation

The VL-1225/6 card can be installed in any slot of an STD Bus card cage, excluding Slot-X in STD 32 cages, and should only be used with other standard (TTL level bus) STD Bus boards. When inserting or extracting the VL-1225/6, make sure the system power is off, also make sure the card is properly oriented (ejector pointing up).

Priority Chain

The VL-1225/6 card does not use the STD Bus priority interrupt chain signals PCO (P51) and PCI (P52). However, because PCI is connected to PCO on board, the card can be installed between cards using the chain.

Signal Levels

The maximum non-destructive input voltage applied to any of the inputs on connector J1 is ±35V with power on (±20V with power off). These voltages are measured with respect to analog ground. Each analog channel presents a minimum input impedance of 1 x 10^8 W.

The analog outputs (VL-1225 only) are capable of providing up to ±5 ma of current across the full output span.

External Connections

J1 is an unlatched 34-pin dual-row (.1" center) header type connector. External connections to the VL-1225/6 can be made with standard cable assemblies, or with the following mating connectors:

Mating Connectors

Connector	Mating Connector
J1	34-pin socket type connectors such as 3M #3414-6634

Figure 3-1. Mating Connectors

Physical Pin Locations

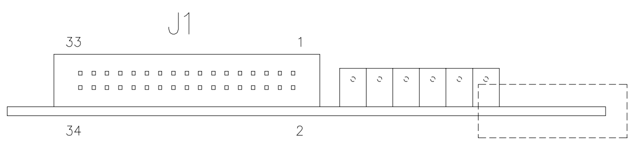
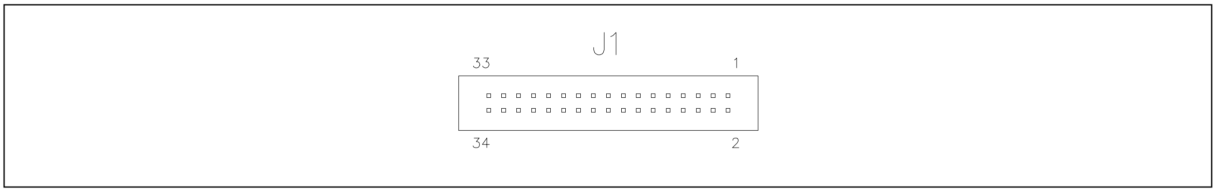


Figure 3-2. I/O Connector Physical Pin Locations

Connector Pinout

J1 — Analog Input/Output Connector



J1 Pin	Single Ended or Pseudo-Differential	Differential
1	Channel 0	Channel 0–
2	Channel 8	Channel 0+
3	Analog Ground	Analog Ground
4	Channel 9	Channel 1+
5	Channel 1	Channel 1
6	Analog Ground	Analog Ground
7	Channel 2	Channel 2–
8	Channel 10	Channel 2+
9	Analog Ground	Analog Ground
10	Channel 11	Channel 3+
11	Channel 3	Channel 3–
12	Analog Ground	Analog Ground
13	Channel 4	Channel 4–
14	Channel 12	Channel 4+
15	Analog Ground	Analog Ground
16	Channel 13	Channel 5+
17	Channel 5	Channel 5–
18	Analog Ground	Analog Ground
19	Channel 6	Channel 6–
20	Channel 14	Channel 6+
21	Analog Ground	Analog Ground
22	Channel 15	Channel 7+
23	Channel 7	Channel 7–
24	Analog Ground	Analog Ground
25	PD	N/C
26	Analog Ground	Analog Ground
27	Analog Ground	Analog Ground
28	Analog Ground	Analog Ground
29	DAC0 (VL-1225 Only)	DAC0 (VL-1225 Only)
30	Analog Ground	Analog Ground
31	Analog Ground	Analog Ground
32	DAC1 (VL-1225 Only)	DAC1 (VL-1225 Only)
33	Analog Ground	Analog Ground
34	Analog Ground	Analog Ground

Figure 3-3. J1 – Analog Input / Output Connector Pinout

Channel 0 to 7. Analog voltages are applied to these inputs for A/D conversion. In single-ended configuration, these inputs are referenced to Analog Ground. In pseudo-differential configuration, these inputs are considered "high side" and are referenced to PD.

Channel 0+ to 7+. Differential "high side" voltages are applied to these inputs for A/D conversion. Each input is referenced to a corresponding differential "low side" input.

Channel 0– to 7–. Differential "low side" voltages are applied to these inputs for A/D conversion. Each input is referenced to a corresponding differential "high side" input.

PD — Pseudo Differential "Low Side". All "low side" pseudo-differential analog voltages are connected together and brought to this pin for differential reference.

DAC0, DAC1 — Analog Outputs. These signals are the 8-bit analog output signals from the two D/A converters (VL-1225 only). Up to ±5 ma can be drawn from each of these outputs.

Analog Ground. This signal is the on-board analog ground. In single-ended mode, all analog inputs are referenced to this signal. The use of multiple ground connections is recommended to maintain a high degree of signal integrity. In differential mode, a return path for the input bias currents of the on-board instrumentation amplifiers must be connected to this pin. This is accomplished by wiring a 10K to 100K W resistor between analog ground and the "low side" of each differential signal source. These resistors should be located in close physically proximity to the signal sources. The cable shield can used for this purpose. The analog outputs (VL-1225 only) are referenced to analog ground.

N/C — No Connection. This signal is not connected to on-board circuitry. It has no function on the VL-1225/6.

Registers

Introduction

This section includes information about registers, control and status bits, and data formats. It focuses primarily on the individual registers, the bits contained within them, and their functional descriptions.

Register Mapping

The VL-1225/6 occupies eight consecutive addresses in the I/O or memory map. The VL-1226 uses four of these addresses as control, data, and status registers, the remaining four are inaccessible. The VL-1225 uses six addresses, with two inaccessible.

The locations of the eight ports are determined by the board address, which is jumper selectable. For compatibility with Analog Devices RTI-1225/6 boards, VersaLogic ships the VL-1225/6 jumpered to memory address FF08H. However, most users configure the board using I/O mapping rather than memory mapping. For simplicity, this manual uses the as-shipped memory mapped addresses when referring to register locations. If you have reconfigured the card, you should substitute your own address for the FF0XH addresses indicated throughout this manual.

Input Port	Output Port	Name	Port Address	As Shipped Address	Page
—	OD1	Channel 1 Output Data Register	Board Address + 7	FF0FH	4-10
—	OD0	Channel 0 Output Data Register	Board Address + 6	FF0EH	4-10
IDHIGH	—	Input Data High Register	Board Address + 5	FF0DH	4-3
IDLOW	—	Input Data Low Register	Board Address + 4	FF0CH	4-3
—	SELECT	Input Channel Select Register	Board Address + 3	FF0BH	4-2
—	—	Not Used	Board Address + 2	FF0AH	—
—	—	Not Used	Board Address + 1	FF09H	—
ISTAT	ICTRL	Interrupt Status / Interrupt Control	Board Address + 0	FF08H	4-13

Figure 4-1. I/O Port Addresses

Analog Input Registers

Input Channel Select Register

Input Channel Select Register (SELECT) — FF0BH

7	6	5	4	3	2	1	0
X	X	X	X	S3	S2	S1	S0

Figure 4-2. Input Channel Select Register

The Channel Select register is a write register used to select the input channel number to be read. Writing a channel number to this register initiates a conversion cycle. Do not write to this register if bit D7 (BUSY) of IDHIGH = 1.

X — Not Used. These bits have no function in the VL-1225/6. It does not matter what value is written to them.

S3, S2, S1, S0 — Channel Address. These bits select the analog channel to use for A/D conversion.

S3	S2	S1	S0	Selected Channel
0	0	0	0	Channel 0
0	0	0	1	Channel 1
0	0	1	0	Channel 2
0	0	1	1	Channel 3
0	1	0	0	Channel 4
0	1	0	1	Channel 5
0	1	1	0	Channel 6
0	1	1	1	Channel 7
1	0	0	0	Channel 8
1	0	0	1	Channel 9
1	0	1	0	Channel 10
1	0	1	1	Channel 11
1	1	0	0	Channel 12
1	1	0	1	Channel 13
1	1	1	0	Channel 14
1	1	1	1	Channel 15

Input Data Low Register

Input Data Low Register (IDLOW) — FF0CH

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 4-4. Input Data Low Register

The Input Data Low register is a read register containing the lower 8 bits of data from the A/D conversion results. It is used in conjunction with the Input Data High register to read the complete 10- or 11-bit A/D data word.

The Input Data Low register should always be read after reading the Input Data High register, never first.

See the Analog Input Operation section on page 5-1 for further information on accessing this register.

AD7-AD0 — A/D Data (Least Significant Bits). These bits contain data bits D7 through D0 of the A/D conversion results. See the Input Data Representation section for a discussion of input data formats.

Input Data High Register

Input Data High Register (IDHIGH) — FF0DH

7	6	5	4	3	2	1	0
BUSY	X	X	X	X	AD10	AD9	AD8

Figure 4-3. Input Data High Register

The Input Data High register is a read register containing the conversion busy bit and the upper order bits of data from the A/D conversion results. It is used in conjunction with the Input Data Low register to read the complete 10- or 11-bit A/D data word.

The Input Data High register should always be read before reading the Input Data Low register.

See the Analog Input Operation section on page 5-1 for further information on accessing this register.

BUSY — Busy. This bit is set to “1” when an A/D conversion is currently in progress, and automatically resets to “0” when the A/D conversion is complete. Use this bit to determine when the analog input data is valid.

X — Not Used. These bits have no function in the VL-1225/6. They will read randomly as 1 or 0, therefore it is important to mask these bits off when interpreting the A/D results.

AD10-AD8 — A/D Data (Most Significant Bits). These bits contain data bits D10 through D8 of the A/D conversion results. In 10-bit mode, AD10 has no function, and it will always = 0. See the Input Data Representation section below for a discussion of input data formats.

Input Data Representation

The format of the data read from the board varies depending on the input range and the data format that is selected. Each of the data formats is discussed below.

Input Binary Format (10-Bit Resolution)

Binary format is used only with the unipolar 0 to +10V input range. 10-bit binary format divides the full 10 Volt analog input range into 1024 steps of 9.77 mV each. The code 0000H is associated with an analog input voltage of 0 Volts (ground). The largest code (03FFH) describes the highest voltage, i.e., +9.9902 Volts. All codes are considered positive. The upper six bits of the Data High register are all zeros.

The formulas for calculating analog or binary digital values are given by:

$$Digital = \left[\frac{Analog}{Step}\right] \qquad\qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.00976563

Sample values are shown in the table below:

Input Voltage	Data (Hex)	Data (Decimal)	Comment
+10.0000	—	—	Out of range
+9.9902	03FF	1023	Maximum voltage
+5.0000	0200	512	Half scale
+2.5000	0100	256	Quarter scale
+1.2500	0080	128	Eighth scale
+0.00977	0001	1	1 LSB
0.0000	0000	0	Zero (ground input)

Figure 4-2. Binary Data Format (10-Bit Resolution)

Input Binary Format (11-Bit Resolution)

Binary format is used only with the unipolar 0 to +10V input range. 11-bit binary format divides the full 10 Volt analog input range into 2048 steps of 4.88 mV each. The code 0000H is associated with an analog input voltage of 0 Volts (ground). The largest code (07FFH) describes the highest voltage, i.e., +9.9951 Volts. All codes are considered positive. The upper five bits of the Data High register are all zeros.

The formulas for calculating analog or binary digital values are given by:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.00488281

Sample values are shown in the table below:

Input Voltage	Data (Hex)	Data (Decimal)	Comment
+10.0000	—	—	Out of range
+9.9951	07FF	2047	Maximum voltage
+5.0000	0400	1024	Half scale
+2.5000	0200	512	Quarter scale
+1.2500	0100	256	Eighth scale
+0.00488	0001	1	1 LSB
0.0000	0000	0	Zero (ground input)

Figure 4-3. Binary Data Format (11-Bit Resolution)

Input Offset Binary Format (10-Bit Resolution)

Offset binary format is used with the bipolar ±5 or ±10V input ranges. 10-bit offset binary format divides the full bipolar analog input range into 1024 steps. The code 0000H is associated with the most negative voltage, i.e. –10 Volts. The largest code (03FFH) describes the most positive voltage, i.e., +9.9805 Volts. An analog input of 0 Volts (ground) will read as 0200H. The upper six bits of the Data High register are all zeros.

The formulas for calculating analog or offset binary digital values are given by:

$$Digital = \left[\frac{Analog + Span}{Step} \right] \qquad Analog = Step \times (Digital - 1) - Span$$

Where:

Analog	=	Applied voltage	
Digital	=	A/D Conversion Data	
Span	=	9.98046875	(±10V Range)
		4.99023437	(±5V Range)
Step	=	0.01953125	(±10V Range)
		0.00976563	(±5V Range)

Sample values are shown in the table below:

±5V Input Voltage	±10V Input Voltage	Data (Hex)	Data (Decimal)	Comment
+5.0000	+10.0000	—	—	Out of range
+4.9902	+9.9805	03FF	1023	Maximum positive voltage
+2.5000	+5.0000	0300	768	Positive half scale
+1.2500	+2.5000	0280	640	Positive quarter scale
+0.00977	+0.01953	0201	513	Positive 1 LSB
0.0000	0.0000	0200	512	Zero (ground input)
–0.00997	–0.01953	01FF	511	Negative 1 LSB
–1.2500	–2.5000	0180	384	Negative quarter scale
–2.5000	–5.0000	0100	256	Negative half scale
–5.0000	–10.0000	0000	0	Maximum negative voltage

Figure 4-4. Offset Binary Data Format (10-Bit Resolution)

Input Offset Binary Format (11-Bit Resolution)

Offset binary format is used with the bipolar ±5 or ±10V input ranges. 11-bit offset binary format divides the full bipolar analog input range into 2048 steps. The code 0000H is associated with the most negative voltage, i.e. –10 Volts. The largest code (07FFH) describes the most positive voltage, i.e., +9.9902 Volts. An analog input of 0 Volts (ground) will read as 0400H. The upper five bits of the Data High register are all zeros.

The formulas for calculating analog or offset binary digital values are given by:

$$Digital = \left[\frac{Analog + Span}{Step} \right] \qquad Analog = Step \times (Digital - 1) - Span$$

Where:

Analog	=	Applied voltage	
Digital	=	A/D Conversion Data	
Span	=	9.99023437	(±10V Range)
		4.99511719	(±5V Range)
Step	=	0.00976563	(±10V Range)
		0.00488281	(±5V Range)

Sample values are shown in the table below:

±5V Input Voltage	±10V Input Voltage	Data (Hex)	Data (Decimal)	Comment
+5.0000	+10.0000	—	—	Out of range
+4.9951	+9.9902	07FF	2047	Maximum positive voltage
+2.5000	+5.0000	0600	1536	Positive half scale
+1.2500	+2.5000	0500	1280	Positive quarter scale
+0.00488	+0.00977	0401	1025	Positive 1 LSB
0.0000	0.0000	0400	1024	Zero (ground input)
–0.00488	–0.00977	03FF	1023	Negative 1 LSB
–1.2500	–2.5000	0300	768	Negative quarter scale
–2.5000	–5.0000	0200	512	Negative half scale
–5.0000	–10.0000	0000	0	Maximum negative voltage

Figure 4-5. Offset Binary Data Format (11-Bit Resolution)

Input Two's Complement Format (10-Bit Resolution)

Two's complement format is used with the bipolar ±5 or ±10V input ranges. 10-bit two's complement format, like 10-bit offset binary format, divides the full bipolar analog input range into 1024 steps. The code 0000H, however, is associated with an analog input voltage of 0 Volts (ground). Positive analog input voltages are represented by positive digital numbers, whereas negative analog input voltages are represented by negative digital numbers (encoded in a 10-bit field), i.e., –1 = 03FFH. The upper six bits of the Data High register are all zeros. Two's complement format is the most common format for expressing bipolar analogs.

The formulas for calculating analog or two's complement digital values are given by:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.01953125 (±10V Range)
0.00976563 (±5V Range)

Sample values are shown in the table below:

±5V Input Voltage	±10V Input Voltage	Data (Hex)	Data (Decimal)	Comment
+5.0000	+10.0000	—	—	Out of range
+4.9902	+9.9805	01FF	511	Maximum positive voltage
+2.5000	+5.0000	0100	256	Positive half scale
+1.2500	+2.5000	0080	128	Positive quarter scale
+0.00977	+0.01953	0001	1	Positive 1 LSB
0.0000	0.0000	0000	0	Zero (ground input)
– 0.00977	– 0.01953	03FF	– 1	Negative 1 LSB
– 1.2500	– 2.5000	0380	– 128	Negative quarter scale
– 2.5000	– 5.0000	0300	– 256	Negative half scale
– 5.0000	– 10.0000	0200	– 512	Maximum negative voltage

Figure 4-6. Two's Complement Data Format (10-Bit Resolution)

Input Two's Complement Format (11-Bit Resolution)

Two's complement format is used with the bipolar ±5 or ±10V input ranges. 11-bit two's complement format, like 11-bit offset binary format, divides the full bipolar analog input range into 2048 steps. The code 0000H, however, is associated with an analog input voltage of 0 Volts (ground). Positive analog input voltages are represented by positive digital numbers, whereas negative analog input voltages are represented by negative digital numbers (encoded in an 11-bit field), i.e., –1 = 07FFH. The upper five bits of the Data High register are all zeros. Two's complement format is the most common format for expressing bipolar analogs.

The formulas for calculating analog or two's complement digital values are given by:

$$Digital = \left[\frac{Analog}{Step}\right] \qquad Analog = Step \times Digital$$

Where:

Analog	=	Applied voltage	
Digital	=	A/D Conversion Data	
Step	=	0.00976563	(±10V Range)
		0.00488281	(±5V Range)

Sample values are shown in the table below:

±5V Input Voltage	±10V Input Voltage	Data (Hex)	Data (Decimal)	Comment
+5.0000	+10.0000	—	—	Out of range
+4.9951	+9.9902	03FF	1023	Maximum positive voltage
+2.5000	+5.0000	0200	512	Positive half scale
+1.2500	+2.5000	0100	256	Positive quarter scale
+0.00488	+0.00977	0001	1	Positive 1 LSB
0.0000	0.0000	0000	0	Zero (ground input)
– 0.00488	– 0.00977	07FF	– 1	Negative 1 LSB
– 1.2500	– 2.5000	0700	– 256	Negative quarter scale
– 2.5000	– 5.0000	0600	– 512	Negative half scale
– 5.0000	– 10.0000	0400	– 1024	Maximum negative voltage

Figure 4-7. Two's Complement Data Format (11-Bit Resolution)

Analog Output Registers

Output Data Registers

Channel 0 (OD0) — FF0EH
Channel 1 (OD1) — FF0FH

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Figure 4-11. Output Data Registers

The Output Data registers are write only registers used for D/A conversion. One register is assigned for each output channel. Data may be written to these registers as fast as desired, since the D/A conversion is virtually instantaneous.

DA7-DA0 — D/A Data. The 8-bit data value written to these bits is converted to an analog output voltage. See the Output Data Representation section for a discussion of output data formats.

Output Data Representation

The format of the data written to the Data Output registers depends on the output range and the output data format that is selected. Each of the data formats is discussed below.

Output Binary Format

Binary format is used only with the unipolar 0 to +10V output range. Binary format divides the full 10 Volt analog output range into 256 steps of 39.06 mV each. The code 00H produces an analog output of 0 Volts. The largest code (FFH) produces a full scale analog output of +9.9609 Volts. All codes are considered positive.

The formulas for calculating analog or binary digital values are given by:

$$Digital = \left[\frac{Analog}{Step}\right] \qquad Analog = Step \times Digital$$

Where:

Analog = Output voltage

Digital = D/A Conversion Data

Step = 0.0390625

Output Voltage	Data (Hex)	Data (Decimal)	Comment
+10.0000	—	—	Out of range
+9.9951	FF	255	Maximum voltage
+5.0000	80	128	Half scale
+2.5000	40	64	Quarter scale
+1.2500	20	32	Eighth scale
+0.03906	01	1	1 LSB
0.0000	00	0	Zero

Figure 4-8. Binary Format

Output Offset Binary Format

Offset binary format is used with the bipolar ±5 or ±10V output ranges. It divides the full bipolar analog output range into 256 steps. The code 00H produces a negative full scale output, and the largest code (FFH) produces a positive full scale output.

The formulas for calculating analog or offset binary digital values are given by:

$$Digital = \left[\frac{Analog + Span}{Step} \right] \qquad Analog = Step \times (Digital - 1) - Span$$

Where:

Analog	=	Applied voltage	
Digital	=	D/A Conversion Data	
Span	=	9.921875	(±10V Range)
		4.9609375	(±5V Range)
Step	=	0.078125	(±10V Range)
		0.0390625	(±5V Range)

Sample values are shown in the table below:

±5V Output Voltage	±10V Output Voltage	Data (Hex)	Data (Decimal)	Comment
+5.0000	+10.0000	—	—	Out of range
+4.9609	+9.9219	FF	255	Maximum positive voltage
+2.5000	+5.0000	C0	192	Positive half scale
+1.2500	+2.5000	A0	160	Positive quarter scale
+0.03906	+0.07813	81	129	Positive 1 LSB
0.0000	+0.0000	80	128	Zero Volts
– 0.03906	– 0.07813	7F	127	Negative 1 LSB
– 1.2500	– 2.5000	60	96	Negative quarter scale
– 2.5000	– 5.0000	40	64	Negative half scale
– 5.0000	– 10.0000	00	0	Maximum negative voltage

Figure 4-9. Offset Binary Format

Output Two's Complement Format

Two's Complement format is used with the ±5V or the ±10V output ranges. It divides the full bipolar analog output range into 256 steps. The code 00H produces an analog output of 0 Volts. Positive digital values produce positive analog output voltages, and negative digital values produce negative analog output voltages. Two's complement format is the most common format for expressing bipolar analogs.

The formulas for calculating analog or two's complement digital values are given by:

$$Digital = \left[\frac{Analog}{Step}\right] \qquad\qquad Analog = Step \times Digital$$

Where:

Analog	=	Applied voltage	
Digital	=	D/A Conversion Data	
Step	=	0.078125	(±10V Range)
		0.0390625	(±5V Range)

Sample values are shown in the table below:

±5V Output Voltage	±10V Output Voltage	Data (Hex)	Data (Decimal)	Comment
+5.0000	+10.0000	—	—	Out of range
+4.9609	+9.9219	7F	127	Maximum positive voltage
+2.5000	+5.0000	40	64	Positive half scale
+1.2500	+2.5000	20	32	Positive quarter scale
+0.03906	+0.07813	01	1	Positive 1 LSB
0.0000	+0.0000	00	0	Zero Volts
– 0.03906	– 0.07813	FF	– 1	Negative 1 LSB
– 1.2500	– 2.5000	E0	– 32	Negative quarter scale
– 2.5000	– 5.0000	C0	– 64	Negative half scale
– 5.0000	– 10.0000	80	– 128	Maximum negative voltage

Figure 4-10. Two's Complement Format

Interrupt Registers

Interrupt Control Register

Interrupt Control Register (ICTRL) — FF08H

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	IE

Figure 4-15. Interrupt Control Register

The Interrupt Control register is a write register used to enable and disable conversion-complete interrupts.

X — Not Used. These bits have no function in the VL-1225/6. It does not matter what value is written to them.

IE — Interrupt Enable. Setting this bit to “1” enables interrupts. In this mode an interrupt request is sent to the CPU when the A/D conversion is complete. Reset this bit to “0” to disable interrupt requests. See page 5-2 for further information about operating the VL-1225/6 with interrupts. An interrupt software example is shown on page 6-2.

Interrupt Status Register

Interrupt Status Register (ISTAT) — FF08H

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	IR

Figure 4-16. Interrupt Status Register

The Interrupt Status register is a read register used to determine the current interrupting status of the VL-1225/6 board.

X — Not Used. These bits have no function in the VL-1225/6. They will always read as “0”.

IR — Interrupt Request. This bit is set to “1” when an interrupt is being requested. It is cleared to “0” when the CPU acknowledges the interrupt. This bit is always “0” when bit D1 (IE) of ICTRL = 0. In systems with multiple, non-vectored interrupting devices, this bit can be read to verify that the VL-1225/6 is responsible for the interrupt.

Operation

This section describes how to operate the VL-1225/6. Two typical input modes of operation, polled mode, and interrupt mode are discussed, as well as a discussion of output mode. Code examples written in 80188 assembly language are included in the next section.

Polled Mode Analog Input

Polled mode operation is the simplest method of operating the VL-1225/6 for analog input. It is the responsibility of the CPU to start each new A/D conversion as desired, and to read the digital results upon completion.

Polled Mode Steps

- Channel selection and Trigger
- Wait until done and keep High Data
- Read Low Data
- Mask unused bits and/or sign extend

Channel selection and Trigger

Output the desired channel number to the Channel Select register (see page 4-2). This automatically triggers the A/D circuits to begin converting. The conversion will complete in about 40 µS. If desired, the CPU is free to execute unrelated code, and then return to the next step in the sequence.

Wait until done and keep High Data

Read the Input Data High register until bit D7 (BUSY) = 0. This is best accomplished by reading the contents of this register directly into the CPU's accumulator or into an 8-bit variable. The Input Data High register contains the conversion status bit and some of the high-order data bits of the A/D results. Bit D7 (BUSY) is set to 1 when the conversion is triggered in the previous step. When BUSY = 0, the A/D conversion has completed, signaling that both Input Data High and Input Data Low registers contain valid data. Since the CPU has been reading the Input Data High register in order to test the BUSY bit, the upper-order bits of the A/D results have already been fetched from the VL-1225/6. It is not necessary to re-read the Input Data High register.

Read the Low Data

Read the Input Data Low register directly into another CPU register. See page 4-3.

Mask unused bits (Optional)

Bit D7 (BUSY) of the Input Data High register is guaranteed to equal 0, however bits D6 – D3 (or D6 – D2 in 10-bit resolution mode) are not guaranteed to be stable. The data should be masked to "0" by ANDing with 07H (or 03H in 10-bit resolution mode). This step can be skipped if the sign extension procedure described below is performed.

Sign Extension (Optional)

In two's complement mode, if you're handling the A/D data using 16-bit variables or CPU registers, it might be desirable to "sign extend" the 10- or 11-bit value into 16 bits prior to storage or mathematical manipulation. This is accomplished by duplicating the sign bit (bit D2 (AD10) in 11-bit resolution mode, or bit D1 (AD9) in 10-bit resolution mode) into all unused bit positions to it's left. The process of sign extension inherently masks unused bits with "1" or "0" as appropriate. The software examples show how this is done with shift instructions.

Interrupt Mode Analog Input

Interrupt mode eliminates the need to repeatedly poll the Status register while waiting for the A/D conversion to complete. This frees up the CPU to execute unrelated code while the VL-1225/6 is busy with an A/D conversion.

Interrupt Mode Steps

- Interrupt Service Routine (ISR)
- Initialize VL-1225/6 for interrupt mode
- Initialize interrupt controller
- Initialize CPU to receive interrupt
- Channel selection and Trigger

Interrupt Service Routine (ISR)

The interrupt service routine reads A/D conversion results from the VL-1225/6 and stores the data somewhere. Data is input from the Input Data High register first, followed by the Input Data Low register. Since execution of the ISR is triggered by bit D7 (BUSY) of IDHIGH, data is guaranteed valid upon ISR entry. It is not necessary to double check the BUSY bit before reading the data. The act of reading the Input Data Low clears the interrupt request signal.

The ISR can be written to mask unused high-order bits and perform sign-extension for two's complement format. If continuous operation is desired, the ISR can select a different channel. Be prepared, however, for another interrupt within 40 µS. If the ISR does not return to the mainline program before this time delay, ISR recursion will occur. Unless special precautions are taken, the CPU return stack will overflow.

In systems with multiple, non-vectored interrupting devices, the interrupt request status bit D0 (IR) of ISTAT can be read to verify that the VL-1225/6 is responsible for the interrupt. See page 4-13 for further information.

Initialize VL-1225/6 for interrupt mode

Set bit D0 (IE) in the Interrupt Control register. See page 4-13 for further information.

Initialize interrupt controller

This involves setting up interrupt vector registers, priority, and unmasking. See your interrupt controller instruction manual for further information.

Initialize CPU to receive interrupts

This involves preparing the interrupt vector table, and enabling interrupts. See your CPU instruction manual for further information.

Channel selection and Trigger

Output the desired channel number to the Channel Select register (see page 4-2). This automatically triggers the A/D circuits to begin converting. An interrupt is generated when the VL-1225/6 completes a A/D conversion.

Analog Output

Writing to a VL-1225 output channel is as simple as writing one byte of data to the desired output channel address. Upon writing the data, the appropriate D/A converter will change its output value.

Software Examples

This section shows some software examples written in Microsoft MASM 5.0 assembly language to assist you in constructing your own software routines. The interrupt code example is written specifically for use with VersaLogic's 80188 CPU card, VL-188.

Polled Mode Analog Input

The following example reads channel 0 into the AX register. It is assumed that the board is addressed at I/O location 0300H.

The key program sections are:

READ Reads A/D channel 0 into AX register.

BUSY Location where program loops waiting for A/D conversion to complete.

```
                                                ;VL-1225/6 REGISTER ADDRESSES
= 0300          istat   equ      00300h   ;Interrupt Status Register
= 0300          ictrl   equ      00300h   ;Interrupt Control Register
= 0303          select  equ      00303h   ;Input Channel Select Register
= 0304          idlow   equ      00304h   ;Input Data Low Register
= 0305          idhigh  equ      00305h   ;Input Data High Register
= 0306          od0     equ      00306h   ;Channel 0 Output Data Register
= 0307          od1     equ      00307h   ;Channel 1 Output Data Register


0000            code    segment  para public 'CODE'
                        assume   cs:code

0000            read:                     ;READ CHANNEL 0 INTO AX REGISTER

0000  BA 0303           mov      dx,select;Select channel 0 and Trigger
0003  B0 00             mov      al,00h
0005  EE                out      dx,al

0006  BA 0305           mov      dx,idhigh;Read BUSY bit and High Data
0009  EC        busy:   in       al,dx
000A  A8 80             test     al,10000000b
000C  75 FB             jnz      busy     ;Loop if BUSY = 1

000E  8A E0             mov      ah,al    ;Mask off unused high-order bits
0010  80 E4 03          and      ah,03h   ;(Use 'ah,07h' for 11 bit mode)

0013  BA 0304           mov      dx,idlow ;Read Data Low register second
0016  EC                in       al,dx

0017            signex:                   ;Sign extend to fill 16-bit register
                                          ;The following 3 instructions are
                                          ;optional.  They are used in
                                          ;two's complement mode only.

0017  B1 06             mov      cl,6     ;Shift count (use 'cl,5' for 11-bit mode)
0019  D3 E0             sal      ax,cl    ;Shift AD10 or AD11 into bit position D7
001B  D3 F8             sar      ax,cl    ;Shift it back, extending sign

001D            code    ends              ;AX register contains A/D data
                        end      read
```

Interrupt Mode Analog Input

The following code example shows how to operate the VL-1225/6 using interrupts. This specific example requests an A/D conversion from channel 0. When the data is ready, an interrupt is generated causing the DONE flag to be set. Data can be read from the variable named VALUE.

The key program sections are:

MAIN	Execution begins at this point. Installation and setup are coordinated.
INIT_188	Initializes the VL-188 interrupt controller to accept interrupts from the STD Bus. Installs interrupt vector into low RAM.
INIT_1225	Initializes the VL-1225/6 to generate interrupts upon conversion complete.
ISR	Interrupt Service Routine. This subroutine is responsible for reading, processing, and/or storing the A/D results from the VL-1225/6.

```
                                                    ;VL-1225/6 REGISTER ADDRESSES
= 0300                  istat    equ      00300h    ;Interrupt Status Register
= 0300                  ictrl    equ      00300h    ;Interrupt Control Register
= 0303                  select   equ      00303h    ;Input Channel Select Register
= 0304                  idlow    equ      00304h    ;Input Data Low Register
= 0305                  idhigh   equ      00305h    ;Input Data High Register
= 0306                  od0      equ      00306h    ;Channel 0 Output Data Register
= 0307                  od1      equ      00307h    ;Channel 1 Output Data Register

                                                    ;VL-188 I/O PORT ADDRESSES
= FF22                  eoi      equ      0FF22h    ;80188 EOI Register
= FF3A                  int1     equ      0FF3Ah    ;80188 INT1 Control Register

0000                    stack    segment public 'STACK'
0000  0100[ ?? ]        db       100h dup (?)
0100                    stack    ends

0000                    data     segment public 'DATA'
0000  ????              value    dw       ?
0002  ????              done     dw       ?
0004                    data     ends

0000                    vector   segment public 'VECTOR'
0034                             org      0034h
0034 ????????????????   vec      dq       ?
003C                    vector   ends

0000                    code     segment para public 'CODE'
                                 assume   cs:code,ds:data

0000                    main:                       ;MAINLINE CODE

0000  B8 ---- R                  mov      ax,data   ;Set data segment register
0003  8E D8                      mov      ds,ax

0005  C7 06 0000 R 0000          mov      value,0   ;Initialize A/D results variable

000B  E8 0027 R                  call     init_188  ;Initialize VL-188 interrupts
000E  E8 0045 R                  call     init_1225 ;Initialize VL-1225/6 interrupts
0011  FB                         sti                ;Enable CPU interrupt flag
```

```
0012                    read:
0012  C7 06 0002 R 0000          mov      done,0        ;Clear done flag
0018  BA 0303                    mov      dx,select     ;Select channel 0 and Trigger
001B  B0 00                      mov      al,00h
001D  EE                         out      dx,al
                                                        ;Unrelated CPU code can be
                                                        ;executed here.  The VL-1225/6
                                                        ;requires 40 microseconds to
                                                        ;complete an A/D conversion.

001E  83 3E 0002 R FF   dcheck:  cmp      done,0ffffh   ;Wait here until the ISR executes
0023  75 F9                      jnz      dcheck

0025                    valid:                          ;The variable 'value' now contains
                                                        ;valid A/D data.

0025  EB FE             stop:    jmp      stop          ;Rest of mainline goes here

0027                    init_188:         ;VL-188 INTERRUPT INITIALIZATION

0027  BA FF3A                    mov      dx,int1       ;INT1 CONTROL REGISTER
002A  B8 0017                    mov      ax,0017h      ;D15 0 —     = Non Functional Bit
002D  EF                         out      dx,ax         ;D14 0 —     = Non Functional Bit
                                                        ;D13 0 —     = Non Functional Bit
                                                        ;D12 0 —     = Non Functional Bit
                                                        ;D11 0 —     = Non Functional Bit
                                                        ;D10 0 —     = Non Functional Bit
                                                        ;D9  0 —     = Non Functional Bit
                                                        ;D8  0 —     = Non Functional Bit
                                                        ;D7  0 —     = Non Functional Bit
                                                        ;D6  0 SFNM  = Normal
                                                        ;D5  0 C     = Non Cascade
                                                        ;D4  1 LTM   = Level Trigger
                                                        ;D3  0 MSK   = Non masked
                                                        ;D2  1 PR2   = Priority 7
                                                        ;D1  1 PR1   = Priority 7
                                                        ;D0  1 PR0   = Priority 7

                                                        ;Un-mask STD Bus INTRQ* interrupts
                                                        ;and set to non-cascade mode because
                                                        ;VL-1225/6 does not provide interrupt
                                                        ;vector.  CPU will internally
                                                        ;generate type code 13.

002E  B8 ---- R                  mov      ax,vector     ;Install service routine address
0031  8E D8                      mov      ds,ax         ;into CPU Interrupt Vector Table
                                 assume   ds:vector
0033  C7 06 0034 R 004C R                 mov           word ptr vec[0],offset isr
0039  C7 06 0036 R ---- R                 mov           word ptr vec[2],seg    isr
                                 assume   ds:data
003F  B8 ---- R                  mov      ax,data
0042  8E D8                      mov      ds,ax
0044  C3                         ret

0045                    init_1225:                      ;VL-1225/6 INTERRUPT INITIALIZATION

0045  B0 01                      mov      al,01h        ;CONTROL REGISTER
0047  BA 0300                    mov      dx,ictrl      ;D7 0 — = Non Functional Bit
004A  EE                         out      dx,al         ;D6 0 — = Non Functional Bit
004B  C3                         ret                    ;D5 0 — = Non Functional Bit
                                                        ;D4 0 — = Non Functional Bit
                                                        ;D3 0 — = Non Functional Bit
                                                        ;D2 0 — = Non Functional Bit
                                                        ;D1 0 — = Non Functional Bit
                                                        ;D0 1 IE  = Interrupt Enable
```

```
004C                 isr:                          ;INTERRUPT SERVICE ROUTINE

004C  50                      push    ax           ;Save CPU registers
004D  51                      push    cx
004E  52                      push    dx
004F  1E                      push    ds

0050  B8 ---- R               mov     ax,data      ;Set data segment register
0053  8E D8                   mov     ds,ax

                                                   ;Read A/D results
0055  BA 0305                 mov     dx,idhigh    ;Read Data High register first
0058  EC                      in      al,dx

0059  8A E0                   mov     ah,al        ;Mask off unused high-order bits
005B  80 E4 03                and     ah,03h       ;(Use 'ah,07h' for 11 bit mode)

005E  BA 0304                 mov     dx,idlow     ;Read Data Low register second
0061  EC                      in      al,dx

0062                          signex:              ;Sign extend to fill 16-bit register
                                                   ;The following 3 instructions are
                                                   ;optional.  They are used in
                                                   ;two's complement mode only.

0062  B1 06                   mov     cl,6         ;Shift count (use 'cl,5' for 11-bit mode)
0064  D3 E0                   sal     ax,cl        ;Shift AD10 or AD11 into bit position D7
0066  D3 F8                   sar     ax,cl        ;Shift it back, extending sign

0068  A3 0000 R               mov     value,ax     ;Store results into variable

006B  C7 06 0002 R FFFF       mov     done,0ffffh  ;Set flag indicating that ISR has ex-
ecuted

                                                   ;Additional processing code is
                                                   ;inserted here if desired.
                                                   ;This could include mathematic
                                                   ;manipulation, data storage,
                                                   ;limit checks, etc.
0071                 isr_exit:
0071  BA FF22                 mov     dx,eoi       ;Issue a Non-Specific End-Of-Interrupt
0074  B8 8000                 mov     ax,8000h     ;command to 80188 interrupt controller
0077  EF                      out     dx,ax

0078  1F                      pop     ds           ;Restore CPU registers
0079  5A                      pop     dx
007A  59                      pop     cx
007B  58                      pop     ax

007C  CF                      iret                 ;Return to interrupted program

007D                 code     ends
                              end     main
```

Analog Output

The following example outputs zero volts to D/A channel 1. It is assumed that the board is addressed at I/O location 0300H, and the output channel is jumpered for two's complement format.

The key program section is:

WRITE Outputs the value 80h (zero volts) to D/A channel number 1.

```
                                                  ;VL-1225 REGISTER ADDRESSES
= 0300          istat   equ     00300h            ;Interrupt Status Register
= 0300          ictrl   equ     00300h            ;Interrupt Control Register
= 0303          select  equ     00303h            ;Input Channel Select Register
= 0304          idlow   equ     00304h            ;Input Data Low Register
= 0305          idhigh  equ     00305h            ;Input Data High Register
= 0306          od0     equ     00306h            ;Channel 0 Output Data Register
= 0307          od1     equ     00307h            ;Channel 1 Output Data Register


0000            code    segment para public 'CODE'
                        assume  cs:code

0000            write:                            ;OUTPUT ZERO VOLTS ON CHANNEL 1

0000  BA 0307           mov     dx,od1            ;Select channel 1
0003  B0 80             mov     al,80h            ;80h = Zero volts in 2's complement mode
0005  EE                out     dx,al             ;Output data to D/A converter

0006            code    ends
                        end     write
```

Reference

Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

ANALOG INPUT (VL-1225 and VL-1226)
Number of Channels: 16 single-ended or 8 differential
Range: 0 to +10V, ±5V, ±10V
Resolution:
    10 bits (1024 counts) RTI-1225/6 Compatible Mode
    11 bits (2048 counts) VL-1225/6 Extended Mode
Conversion Time: 25 µs + settling time
Settling Time: 15 µs
Throughput: 25,000 channels/sec
Overvoltage Protection:
    ±35V with power on
    ±20V with power off
Impedance: 1 x 10^8 Ω min.
Data Format: Binary, offset binary, or two's complement
Common Mode Voltage (CMV): ±10V min
Common Mode Rejection (CMR): 60 dB
Linearity: ±½ LSB
Differential Nonlinearity: ±½ LSB
Temperature Coefficient:
    Gain ±50 ppm/°C of FSR
    Offset ±25 ppm/°C of FSR
Addressing: 16 bits + MEMEX or IOEXP
Mapping: 8-byte memory or I/O block on any 8-byte boundary
Size: Meets all STD 32 Bus mechanical specifications
Storage Temperature: –40° to +75 °C
Free Air Operating Temperature: 0° to +65 °C
Power Requirements:
    5V ±5% @ 480 ma typ. (VL-1225)
    5V ±5% @ 430 ma typ. (VL-1226)

ANALOG OUTPUT (VL-1225 only)
Number of Channels: 2
Resolution: 8 bits (256 counts)
Data Format: Binary, offset binary, or two's complement
Range: 0 to +10V, ±5V, ±10V @ 5 ma (max)
Settling Time: 25 µs (to ±½ LSB)
Linearity: ±½ LSB
Differential Nonlinearity: ±½ LSB
Temperature Coefficient:
    Gain ±50 ppm/°C of FSR
    Offset ±30 µV/°C

BUS COMPATIBILITY (VL-1225 and VL-1226)
STD 80: Full compliance, all bus speeds
STD Z80: Full compliance, all bus speeds
STD 32: I/O slave, SA8-I, IX

VL-1225 Jumper Block Locations

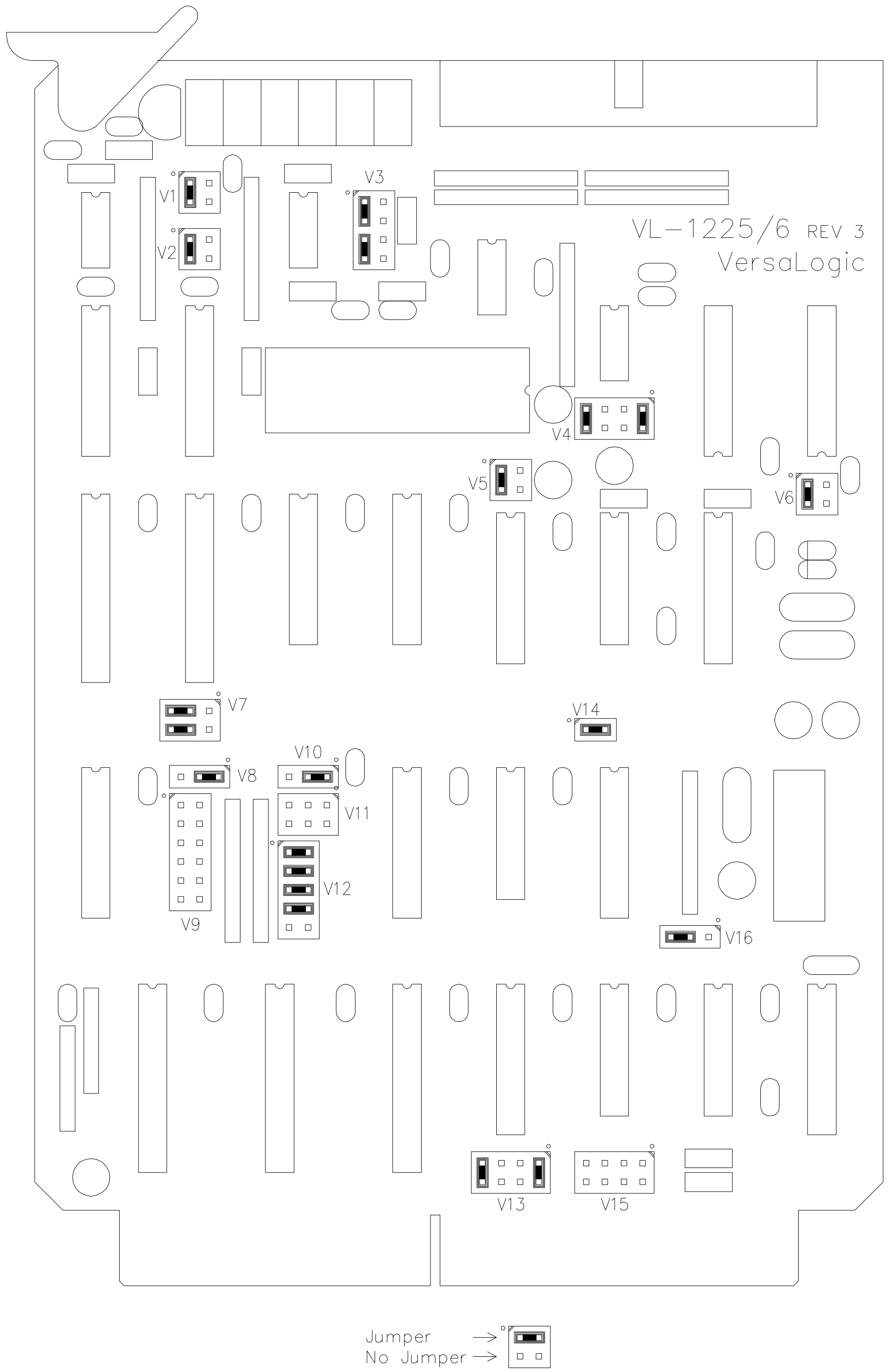


Figure 7-1. Jumper Block Locations for VL-1225

VL-1225 Jumper Options

Jumper Block	Description	As Shipped	Page
V1	Channel 0 Output Voltage Range (see also V16)	±10V	2-18
	$V1_{1-3}$ = In, $V1_{2-4}$ = In – ±5V		
	$V1_{1-3}$ = In, $V1_{2-4}$ = Out – ±10V		
	$V1_{1-3}$ = Out, $V1_{2-4}$ = In – 0 to 10V		
V2	Channel 1 Output Voltage Range (see also V16)	±10V	2-18
	$V2_{1-3}$ = In, $V2_{2-4}$ = In – ±5V		
	$V2_{1-3}$ = In, $V2_{2-4}$ = Out – ±10V		
	$V2_{1-3}$ = Out, $V2_{2-4}$ = In – 0 to 10V		
V3	Input Voltage Range Select	±10V	2-16
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – ±5V		
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = In, $V3_{6-8}$ = Out – ±10V		
	$V3_{1-3}$ = Out, $V3_{2-4}$ = In, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – 0 to 10V		
V4 & V6	Input Mode	S.E.	2-13
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = Out, $V4_{7-8}$ = In, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Single Ended		
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = In, $V4_{7-8}$ = Out, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Pseudo-Differential		
	$V4_{1-2}$ = Out, $V4_{3-4}$ = In, $V4_{5-6}$ = Out, $V4_{7-8}$ = Out, $V6_{1-2}$ = Out, $V6_{3-4}$ = In – Differential		
V5	Input Data Format	2's Comp.	2-17
	$V5_{1-3}$ = Out, $V5_{2-4}$ = In – Binary / Offset Binary		
	$V5_{1-3}$ = In, $V5_{2-4}$ = Out – Two's Complement		
$V7_{1-3 \& 3-5}$	Channel 0 Output Data Format	2's Comp.	2-19
	$V7_{1-3}$ = In, $V7_{3-5}$ = Out – Binary / Offset Binary		
	$V7_{1-3}$ = Out, $V7_{3-5}$ = In – Two's Complement		
$V7_{2-4 \& 4-6}$	Channel 1 Output Data Format	2's Comp.	2-19
	$V7_{2,4}$ = In, $V7_{4,6}$ = Out – Binary / Offset Binary		
	$V7_{2,4}$ = Out, $V7_{4,6}$ = In – Two's Complement		
V8	MEMEX Select	Ignore	2-12
	$V8_{1-2}$ = In, $V8_{2-3}$ = Out – Ignore MEMEX		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = Out – Enable on MEMEX high		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = In – Enable on MEMEX low		
V9	Board Address (A10 – A15)	FF08H	2-6
	$V9_{1-2}$ = In – A15 decoded Low; $V9_{1-2}$ = Out – A15 decoded High		
	$V9_{3-4}$ = In – A14 decoded Low; $V9_{3-4}$ = Out – A14 decoded High		
	$V9_{5-6}$ = In – A13 decoded Low; $V9_{5-6}$ = Out – A13 decoded High		
	$V9_{7-8}$ = In – A12 decoded Low; $V9_{7-8}$ = Out – A12 decoded High		
	$V9_{9-10}$ = In – A11 decoded Low; $V9_{9-10}$ = Out – A11 decoded High		
	$V9_{11-12}$ = In – A10 decoded Low; $V9_{11-12}$ = Out – A10 decoded High		
V10	IOEXP Select	Ignore	2-10
	$V10_{1-2}$ = In, $V10_{2-3}$ = Out – Ignore IOEXP		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = Out – Enable on IOEXP high		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = In – Enable on IOEXP low		
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi	2-6
	$V11_{1-3}$ = In, $V11_{2-4}$ = In, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 8-Bit Mode (ignore A8 & A9)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = High, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = High, A9 = Low)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = Low, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = Low, A9 = Low)		
V12	Board Address (A3 – A7)	FF08H	2-6
	$V12_{1-2}$ = In – A7 decoded Low; $V12_{1-2}$ = Out – A7 decoded High		
	$V12_{3-4}$ = In – A6 decoded Low; $V12_{3-4}$ = Out – A6 decoded High		
	$V12_{5-6}$ = In – A5 decoded Low; $V12_{5-6}$ = Out – A5 decoded High		
	$V12_{7-8}$ = In – A4 decoded Low; $V12_{7-8}$ = Out – A4 decoded High		
	$V12_{9-10}$ = In – A3 decoded Low; $V12_{9-10}$ = Out – A3 decoded High		
V13	Address Type Select	Memory	2-6
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit Memory Mapped		
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = In, $V13_{7-8}$ = Out – 8- or 10-Bit I/O Mapped		
	$V13_{1-2}$ = Out, $V13_{3-4}$ = In, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit I/O Mapped		
V14	Analog Input Resolution	10-Bit	2-16
	V14 = In – 10-Bit; V14 = Out – 11-Bit		
V15	Interrupt Request Select	None	2-21
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – None		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = In – INT2* (P50)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = In, $V15_{7-8}$ = Out – INT1* (P37)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = In, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – INT* (P44)		
	$V15_{1-2}$ = In, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – IRQx (E47)		
V16	D/A Power-Up Output Voltage	Zero Volts	2-20
	$V16_{1-2}$ = In, $V16_{2-3}$ = Out – Zero Volts (in Two's Complement/Bipolar, and Binary/Unipolar modes)		
	– Negative Full Scale (in Offset Binary/Bipolar mode)		
	$V16_{1-2}$ = Out, $V16_{2-3}$ = In – Zero Volts (in Offset Binary/Bipolar mode)		
	– Negative Full Scale (in Two's Complement/Bipolar mode)		
	– Half Scale (in Binary/Unipolar mode)		

Figure 7-2. VL-1225 Jumper Functions

VL-1226 Jumper Block Locations

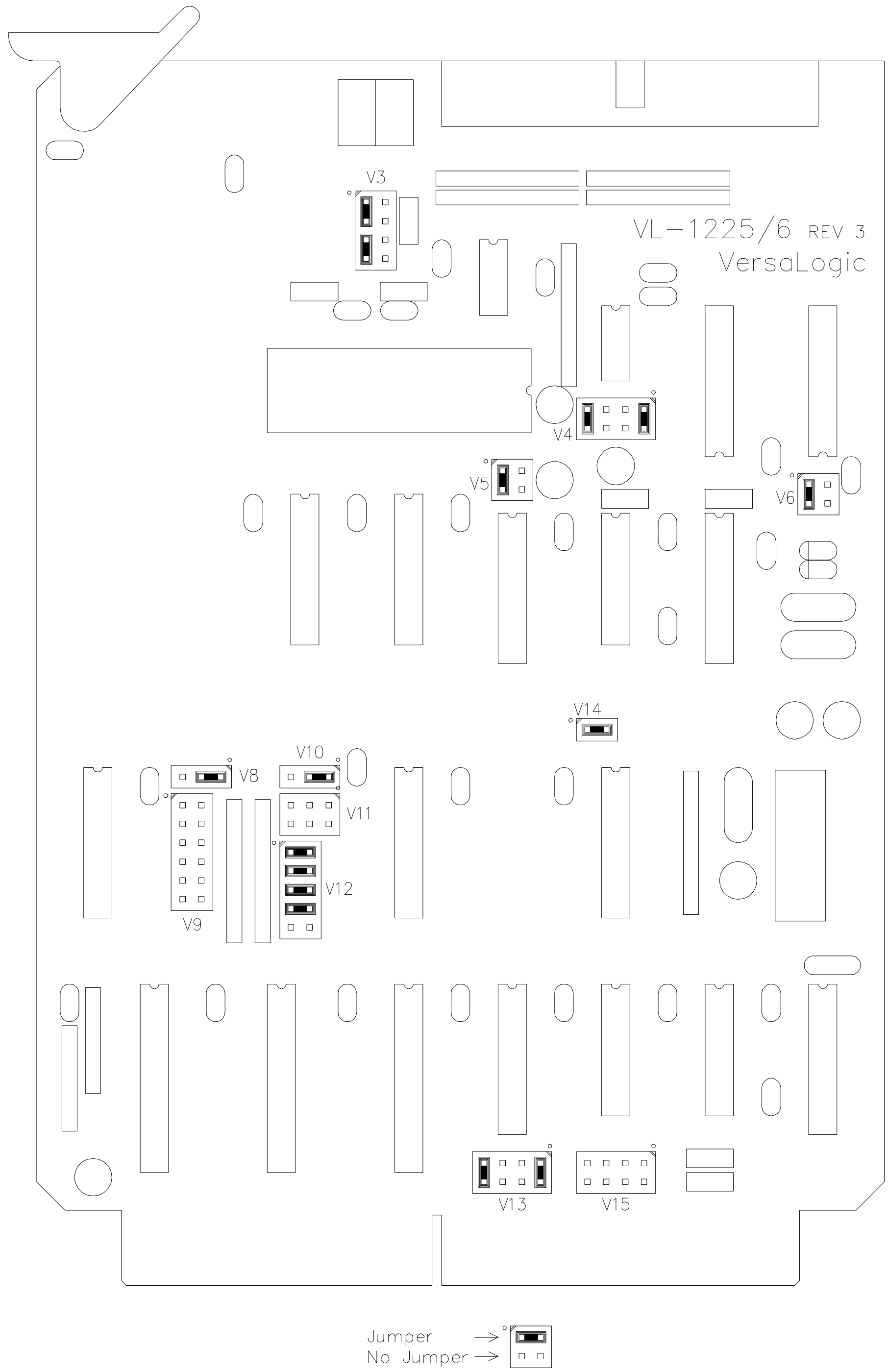


Figure 7-3. Jumper Block Locations for VL-1226

VL-1226 Jumper Options

Jumper Block	Description	As Shipped	Page
V1	1225 Only	—	—
V2	1225 Only	—	—
V3	Input Voltage Range Select	±10V	2-16
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – ±5V		
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = In, $V3_{6-8}$ = Out – ±10V		
	$V3_{1-3}$ = Out, $V3_{2-4}$ = In, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – 0 to 10V		
V4 & V6	Input Mode	S.E.	2-13
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = Out, $V4_{7-8}$ = In, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Single Ended		
	$V4_{1-2}$ = In, $V4_{3-4}$ = Out, $V4_{5-6}$ = In, $V4_{7-8}$ = Out, $V6_{1-2}$ = In, $V6_{3-4}$ = Out – Pseudo-Differential		
	$V4_{1-2}$ = Out, $V4_{3-4}$ = In, $V4_{5-6}$ = Out, $V4_{7-8}$ = Out, $V6_{1-2}$ = Out, $V6_{3-4}$ = In – Differential		
V5	Input Data Format	2's Comp.	2-17
	$V5_{1-3}$ = Out, $V5_{2-4}$ = In – Binary / Offset Binary		
	$V5_{1-3}$ = In, $V5_{2-4}$ = Out – Two's Complement		
V7	1225 Only	—	—
V8	MEMEX Select	Ignore	2-12
	$V8_{1-2}$ = In, $V8_{2-3}$ = Out – Ignore MEMEX		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = Out – Enable on MEMEX high		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = In – Enable on MEMEX low		
V9	Board Address (A10 – A15)	FF08H	2-6
	$V9_{1-2}$ = In – A15 decoded Low; $V9_{1-2}$ = Out – A15 decoded High		
	$V9_{3-4}$ = In – A14 decoded Low; $V9_{3-4}$ = Out – A14 decoded High		
	$V9_{5-6}$ = In – A13 decoded Low; $V9_{5-6}$ = Out – A13 decoded High		
	$V9_{7-8}$ = In – A12 decoded Low; $V9_{7-8}$ = Out – A12 decoded High		
	$V9_{9-10}$ = In – A11 decoded Low; $V9_{9-10}$ = Out – A11 decoded High		
	$V9_{11-12}$ = In – A10 decoded Low; $V9_{11-12}$ = Out – A10 decoded High		
V10	IOEXP Select	Ignore	2-10
	$V10_{1-2}$ = In, $V10_{2-3}$ = Out – Ignore IOEXP		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = Out – Enable on IOEXP high		
	$V10_{1-2}$ = Out, $V10_{2-3}$ = In – Enable on IOEXP low		
V11	Board Address (A8, A9) / 8-Bit Mode Selector	A8Hi, A9Hi	2-6
	$V11_{1-3}$ = In, $V11_{2-4}$ = In, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 8-Bit Mode (ignore A8 & A9)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = High, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = Out, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = High, A9 = Low)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = Low, A9 = High)		
	$V11_{1-3}$ = Out, $V11_{2-4}$ = Out, $V11_{3-5}$ = In, $V11_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = Low, A9 = Low)		
V12	Board Address (A3 – A7)	FF08H	2-6
	$V11_{1-2}$ = In – A7 decoded Low; $V11_{1-2}$ = Out – A7 decoded High		
	$V11_{3-4}$ = In – A6 decoded Low; $V11_{3-4}$ = Out – A6 decoded High		
	$V11_{5-6}$ = In – A5 decoded Low; $V11_{5-6}$ = Out – A5 decoded High		
	$V11_{7-8}$ = In – A4 decoded Low; $V11_{7-8}$ = Out – A4 decoded High		
	$V11_{9-10}$ = In – A3 decoded Low; $V11_{9-10}$ = Out – A3 decoded High		
V13	Address Type Select	Memory	2-6
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit Memory Mapped		
	$V13_{1-2}$ = In, $V13_{3-4}$ = Out, $V13_{5-6}$ = In, $V13_{7-8}$ = Out – 8- or 10-Bit I/O Mapped		
	$V13_{1-2}$ = Out, $V13_{3-4}$ = In, $V13_{5-6}$ = Out, $V13_{7-8}$ = In – 16-Bit I/O Mapped		
V14	Analog Input Resolution	10-Bit	2-16
	V14 = In – 10-Bit; V14 = Out – 11-Bit		
V15	Interrupt Request Select	None	2-21
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – None		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = In – INT2* (P50)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = Out, $V15_{5-6}$ = In, $V15_{7-8}$ = Out – INT1* (P37)		
	$V15_{1-2}$ = Out, $V15_{3-4}$ = In, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – INT* (P44)		
	$V15_{1-2}$ = In, $V15_{3-4}$ = Out, $V15_{5-6}$ = Out, $V15_{7-8}$ = Out – IRQx (E47)		
V16	1225 Only	—	—

Figure 7-4. VL-1226 Jumper Functions

Register Map

The VL-1225/6 occupies eight bytes in the I/O or memory map. Only four of these addresses are actually used to interface with the board.

The locations of the eight ports are determined by the board address, which is jumper selectable. For compatibility with Analog Devices RTI-1225/6 boards, VersaLogic ships the VL-1225/6 jumpered to memory address FF08H. However, most users configure the board using I/O mapping rather than memory mapping. For simplicity, this manual uses the as-shipped memory mapped addresses when referring to register locations. If you have reconfigured the card, you should substitute your own address for the FF0XH addresses indicated throughout this manual.

Input Port	Output Port	Name	Port Address	As Shipped Address	Page
—	OD1	Channel 1 Output Data Register	Board Address + 7	FF0FH	4-10
—	OD0	Channel 0 Output Data Register	Board Address + 6	FF0EH	4-10
IDHIGH	—	Input Data High Register	Board Address + 5	FF0DH	4-3
IDLOW	—	Input Data Low Register	Board Address + 4	FF0CH	4-3
—	SELECT	Input Channel Select Register	Board Address + 3	FF0BH	4-2
—	—	Not Used	Board Address + 2	FF0AH	—
—	—	Not Used	Board Address + 1	FF09H	—
ISTAT	ICTRL	Interrupt Status / Interrupt Control	Board Address + 0	FF08H	4-13

Figure 7-5. I/O Port Addesses

Calibration

The VL-1225/6 is calibrated before shipment. However, it may be desirable to recalibrate the card after installation, and approximately once each year (depending on the accuracy requirements of the application).

Required Equipment

- A voltmeter with resolution and accuracy to ½ LSB of the input range being used.
- A low noise voltage source adjustable over the input range.
- A small flat-blade screwdriver.

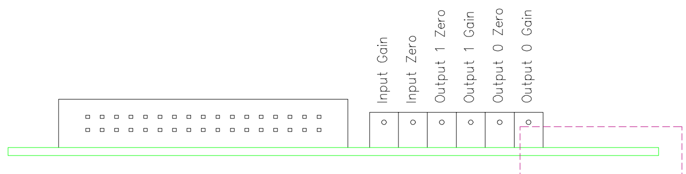


Figure 7-6. Adjustment Pot Locations

Input Calibration (VL-1225 and VL-1226)

- Disconnect all inputs to the card and connect the voltage source to any channel.
- Using the voltmeter, adjust the voltage source according to table below:

10-Bit Resolution			11-Bit Resolution		
±5V Range	**±10V Range**	**0 to 10V Range**	**±5V Range**	**±10V Range**	**0 to 10V Range**
–4.99511719V	–9.99023438V	+0.00488281V	–4.99755859V	–9.99511719V	+0.00244141V

- Using a program to continuously read the input channel, adjust the “Input Zero” pot until the reading toggles between the two values shown in the table below.

10-Bit Resolution			11-Bit Resolution		
Binary	**Offset Binary**	**Two’s Complement**	**Binary**	**Offset Binary**	**Two’s Complement**
0000H	0000H	0200H	0000H	0000H	0400H
0001H	0001H	0201H	0001H	0001H	0401H

- Using the voltmeter, adjust the voltage source according to the table below.

10-Bit Resolution			11-Bit Resolution		
±5V Range	**±10V Range**	**0 to 10V Range**	**±5V Range**	**±10V Range**	**0 to 10V Range**
+4.98535156V	+9.97070313V	+9.8535156V	+4.99267578V	+9.98535156V	+9.99267578V

- Using a program to continuously read the input channel, adjust the “Input Gain” pot until the reading toggles between the two values shown in the table below.

10-Bit Resolution			11-Bit Resolution		
Binary	**Offset Binary**	**Two’s Complement**	**Binary**	**Offset Binary**	**Two’s Complement**
03FFH	03FFH	01FFH	07FFH	07FFH	03FFH
03FEH	03FEH	01FEH	07FEH	07FEH	03FEH

Output Calibration (VL-1225 only)

- Disconnect all inputs and outputs from the card and connect the voltmeter to channel 0.
- Referring to the table below, select the column which matches the output range and data format of the channel being calibrated.
- Write the "ZERO" data to the output channel as indicated in the table. This causes the largest negative voltage to be output.
- Adjust the ZERO pot (Z0 for channel 0, Z1 for channel 1) until the "ZERO" output reading, as indicated in the table, shows on the voltmeter.
- Write the "GAIN" data to the output channel. This causes the largest positive voltage to be output.
- Adjust the GAIN pot (G0 for channel 0, G1 for channel 1) until the "GAIN" output reading, as indicated in the table, shows on the voltmeter.
- Repeat the above steps for channel 1.

	Output Range				
	±5V Offset Binary	**±5V Two's Complement**	**±10V Offset Binary**	**±10V Two's Complement**	**0 to 10V Natural Binary**
"ZERO"					
Data	00H	80H	00H	80H	00H
Output	–5.000V	–5.000V	–10.000V	–10.000V	0.000V
"GAIN"					
Data	FFH	7FH	FFH	7FH	FFH
Output	+4.961V	+4.961V	+9.922V	+9.922V	+9.961V

Figure 7-8. Calibration Codes

External Connections

J1 is an unlatched 34-pin dual-row (.1" center) header type connector. External connections to the VL-1225/6 can be made with standard cable assemblies, or with the following mating connectors:

Mating Connectors

Connector	Mating Connector
J1	26-pin socket type connectors such as 3M #3399-7026, Ansley 609-3441, or Robinson Nugent FDSC34PK-SR-TG

Figure 7-9. Mating Connectors

Physical Pin Locations

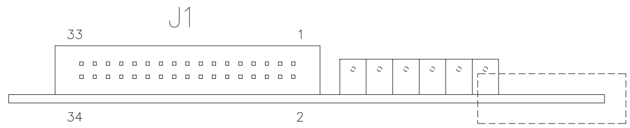


Figure 7-10. I/O Connector Physical Pin Locations

Connector Pinout

The table below shows the pinout for the analog I/O connector. See page 3-3 for detailed information.

J1 — Analog Input/Output Connector

J1 Pin	Single Ended or Pseudo-Differential	Differential
1	Channel 0	Channel 0–
2	Channel 8	Channel 0+
3	Analog Ground	Analog Ground
4	Channel 9	Channel 1+
5	Channel 1	Channel 1–
6	Analog Ground	Analog Ground
7	Channel 2	Channel 2–
8	Channel 10	Channel 2+
9	Analog Ground	Analog Ground
10	Channel 11	Channel 3+
11	Channel 3	Channel 3–
12	Analog Ground	Analog Ground
13	Channel 4	Channel 4–
14	Channel 12	Channel 4+
15	Analog Ground	Analog Ground
16	Channel 13	Channel 5+
17	Channel 5	Channel 5–
18	Analog Ground	Analog Ground
19	Channel 6	Channel 6–
20	Channel 14	Channel 6+
21	Analog Ground	Analog Ground
22	Channel 15	Channel 7+
23	Channel 7	Channel 7–
24	Analog Ground	Analog Ground
25	PD	N/C
26	Analog Ground	Analog Ground
27	Analog Ground	Analog Ground
28	Analog Ground	Analog Ground
29	DAC0 (VL-1225 Only)	DAC0 (VL-1225 Only)
30	Analog Ground	Analog Ground
31	Analog Ground	Analog Ground
32	DAC1 (VL-1225 Only)	DAC1 (VL-1225 Only)
33	Analog Ground	Analog Ground
34	Analog Ground	Analog Ground

Figure 7-11. J1 – Analog Input/Output Connector Pinout

Decimal / Hex / ASCII Conversion Chart

The chart below is useful for both ASCII and decimal / hex conversion. The “^” symbol denotes control characters. “^A” represents control-A, etc.

Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL	32	20	SPACE	64	40	@	96	60	‘
1	01	SOH ^A	33	21	!	65	41	A	97	61	a
2	02	STX ^B	34	22	“	66	42	B	98	62	b
3	03	ETX ^C	35	23	#	67	43	C	99	63	c
4	04	EOT ^D	36	24	$	68	44	D	100	64	d
5	05	ENQ ^E	37	25	%	69	45	E	101	65	e
6	06	ACK ^F	38	26	&	70	46	F	102	66	f
7	07	BEL ^G	39	27	‘	71	47	G	103	67	g
8	08	BS ^H	40	28	(	72	48	H	104	68	h
9	09	HT ^I	41	29	)	73	49	I	105	69	i
10	0A	LF ^J	42	2A	*	74	4A	J	106	6A	j
11	0B	VT ^K	43	2B	+	75	4B	K	107	6B	k
12	0C	FF ^L	44	2C	,	76	4C	L	108	6C	l
13	0D	CR ^M	45	2D	–	77	4D	M	109	6D	m
14	0E	SO ^N	46	2E	.	78	4E	N	110	6E	n
15	0F	SI ^O	47	2F	/	79	4F	O	111	6F	o
16	10	DLE ^P	48	30	0	80	50	P	112	70	p
17	11	DC1 ^Q	49	31	1	81	51	Q	113	71	q
18	12	DC2 ^R	50	32	2	82	52	R	114	72	r
19	13	DC3 ^S	51	33	3	83	53	S	115	73	s
20	14	DC4 ^T	52	34	4	84	54	T	116	74	t
21	15	NAK ^U	53	35	5	85	55	U	117	75	u
22	16	SYN ^V	54	36	6	86	56	V	118	76	v
23	17	ETB ^W	55	37	7	87	57	W	119	77	w
24	18	CAN ^X	56	38	8	88	58	X	120	78	x
25	19	EM ^Y	57	39	9	89	59	Y	121	79	y
26	1A	SUB ^Z	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL

Figure 7-12. Decimal / Hex / ASCII Conversion Chart

STD 80 Bus Pinout

COMPONENT SIDE

Pin	Signal	Flow	Description
P01	+5VDC	In	Logic Power
P03	GND	In	Logic Ground
P05	VBAT	—	Battery Power
P07	A19/D3	I/O	Address/Data
P09	A18/D2	I/O	Address/Data
P11	A17/D1	I/O	Address/Data
P13	A16/D0	I/O	Address/Data
P15	A07	In	Address
P17	A06	In	Address
P19	A05	In	Address
P21	A04	In	Address
P23	A03	In	Address
P25	A02	In	Address
P27	A01	In	Address
P29	A00	In	Address
P31	WR*	In	Write Mem or I/O
P33	IORQ*	In	I/O Address Select
P35	IOEXP	In	I/O Expansion
P37	INTRQ1*	Out	Interrupt Request 1
P39	STATUS1*	—	CPU Status 1
P41	BUSAK*	—	Bus Acknowledge
P43	INTAK*	—	Interrupt Acknowledge
P45	WAITRQ*	—	Wait Request
P47	SYSRESET*	In	System Reset
P49	CLOCK*	—	Clock
P51	PCO	Out	Priority Chain Out
P53	AUX GND	—	AUX Ground
P55	AUX +V	—	AUX Positive (+12VDC)

SOLDER SIDE

Pin	Signal	Flow	Description
P02	+5VDC	In	Logic Power
P04	GND	In	Logic Ground
P06	DCPDN*	—	DC Power Down
P08	A23/D7	I/O	Address/Data
P10	A22/D6	I/O	Address/Data
P12	A21/D5	I/O	Address/Data
P14	A20/D4	I/O	Address/Data
P16	A15	In	Address
P18	A14	In	Address
P20	A13	In	Address
P22	A12	In	Address
P24	A11	In	Address
P26	A10	In	Address
P28	A09	In	Address
P30	A08	In	Address
P32	RD*	In	Read Mem or I/O
P34	MEMRQ*	—	Memory Address Select
P36	BHE* (MEMEX)	In	Byte High Enable (Mem Expansion)
P38	ALE*	—	Address Latch Enable
P40	STATUS0*	—	CPU Status 0
P42	BUSRQ*	—	Bus Request
P44	INTRQ*	Out	Interrupt Request
P46	NMIRQ*	—	Non-maskable Interrupt Request
P48	PBRESET*	—	Push-Button Reset
P50	CNTRL* (INTRQ2*)	—	Aux Timing
P52	PCI	In	Priority Chain In
P54	AUX GND	—	AUX Ground
P56	AUX –V	—	AUX Negative (–12VDC)

* Denotes an active low signal.
— Denotes signal not used on this board.

Figure 7-13. STD 80 Bus Pinout

STD 32 Bus Pinout Extension

COMPONENT SIDE				SOLDER SIDE			
Pin	**Signal**	**Flow**	**Description**	**Pin**	**Signal**	**Flow**	**Description**
E01	GND	—	Logic Ground	E02	RSVD	—	Reserved
E03	XA19	—	Address	E04	XA23	—	Address
E05	XA18	—	Address	E06	XA22	—	Address
E07	XA17	—	Address	E08	XA21	—	Address
E09	XA16	—	Address	E10	XA20	—	Address
E11	NOWS*	—	No Wait States	E12	RSVD	—	Reserved
E13	+5VDC	In	Logic Power	E14	+5VDC	In	Logic Power
E15	DAKx*	—	DMA Acknowledge	E16	DREQx*	—	DMA Request
E17	GND	In	Logic Ground	E18	GND	In	Logic Ground
E19	D27	—	Data	E20	D31	—	Data
E21	D26	—	Data	E22	D30	—	Data
E23	D25	—	Data	E24	D29	—	Data
E25	D24	—	Data	E26	D28	—	Data
E27	D23	—	Data	E28	GND	—	Logic Ground
E29	D22	—	Data	E30	D15	—	Data
E31	D21	—	Data	E32	D14	—	Data
E33	D20	—	Data	E34	D13	—	Data
E35	GND	—	Logic Ground	E36	D12	—	Data
E37	D19	—	Data	E38	D11	—	Data
E39	D18	—	Data	E40	D10	—	Data
E41	D17	—	Data	E42	D09	—	Data
E43	D16	—	Data	E44	D08	—	Data
E45	GND	—	Logic Ground	E46	MASTER 16*	—	Master 16-Bit
E47	IRQx	Out	Interrupt Request	E48	AENx*	—	Address Enable
E49	BE1*	—	Byte Enable 1	E50	BE3*	—	Byte Enable 3
E51	BE0*	—	Byte Enable 2	E52	BE2*	—	Byte Enable 2
E53	MEM16*	—	Memory 16-Bit	E54	GND	—	Logic Ground
E55	M–IO	—	Memory or I/O	E56	W–R	—	Write or Read
E57	DMAIOW*	—	DMA I/O Write	E58	DMAIOR*	—	DMA I/O Read
E59	IO16*	—	I/O 16-Bit	E60	EX8*	—	Exchange 8-Bit
E61	CMD*	—	Command	E62	START*	—	Start
E63	EX16*	—	Exchange 16-Bit	E64	EX32*	—	Exchange 32-Bit
E65	EXRDY	—	Exchange Ready	E66	T–C	—	Terminate or Count
E67	LOCK*	—	Lock	E68	+5VDC	—	Logic Power
E69	MAKx*	—	Master Acknowledge	E70	MREQx*	—	Master Request
E71	SLBURST*	—	Slave Burst	E72	MSBURST*	—	Master Burst
E73	XA27*	—	Address	E74	XA31*	—	Address
E75	XA26*	—	Address	E76	XA30*	—	Address
E77	XA25*	—	Address	E78	XA29*	—	Address
E79	XA24*	—	Address	E80	XA28*	—	Address

* Denotes an active low signal.
— Denotes signal not used on this board.

Figure 7-14. STD 32 Bus Pinout Extension

VL-1225 Parts Placement Diagram

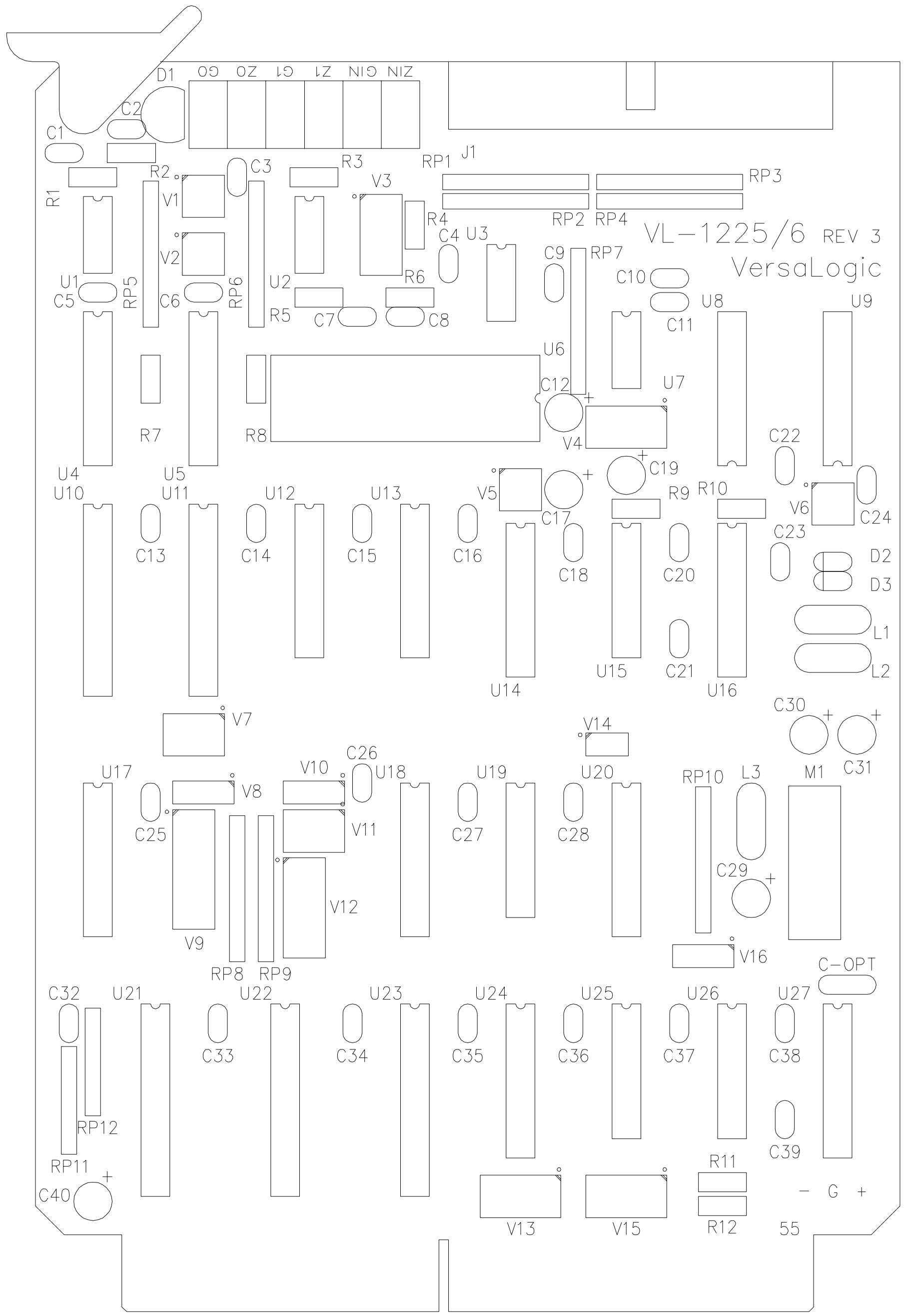
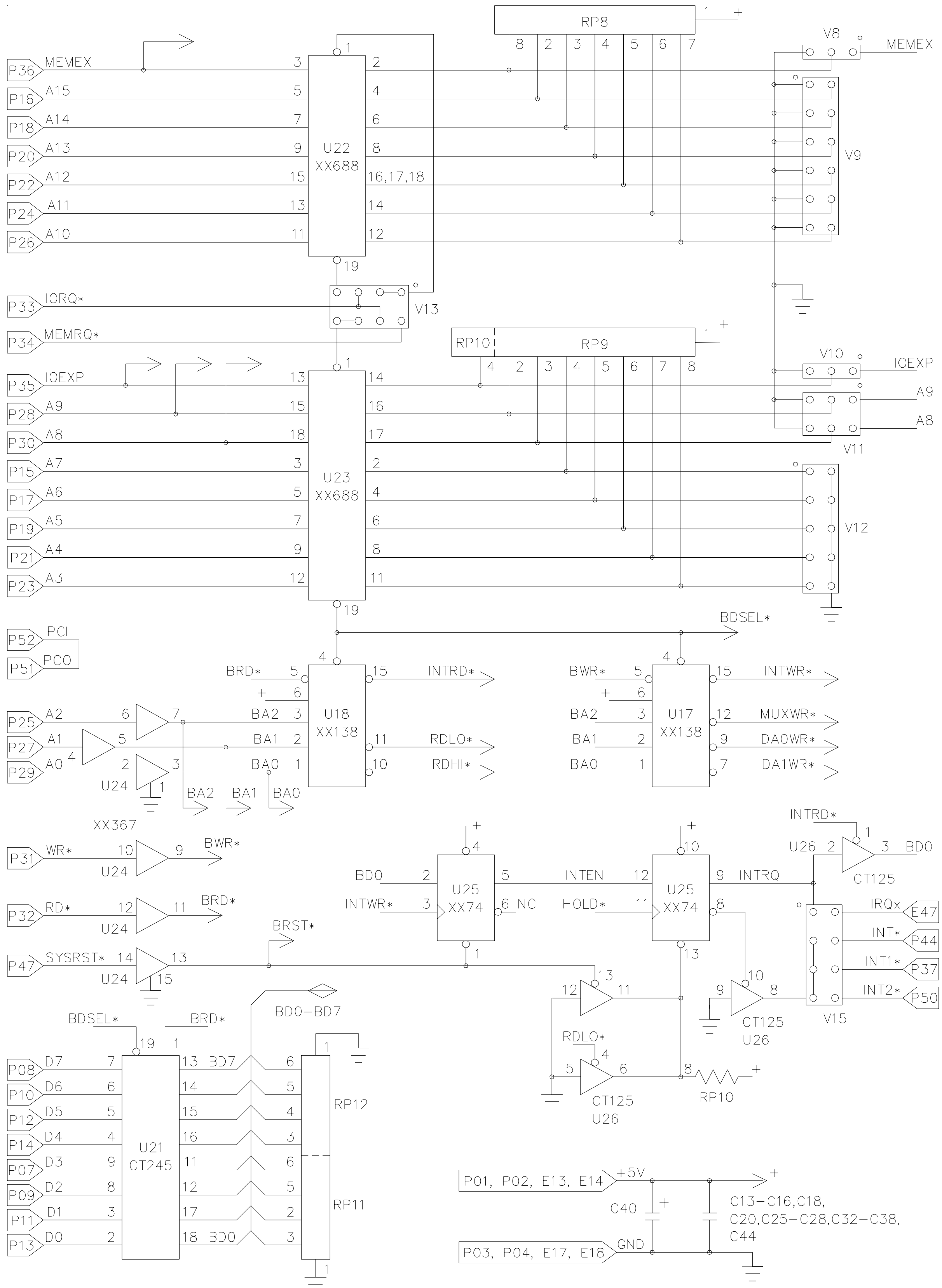


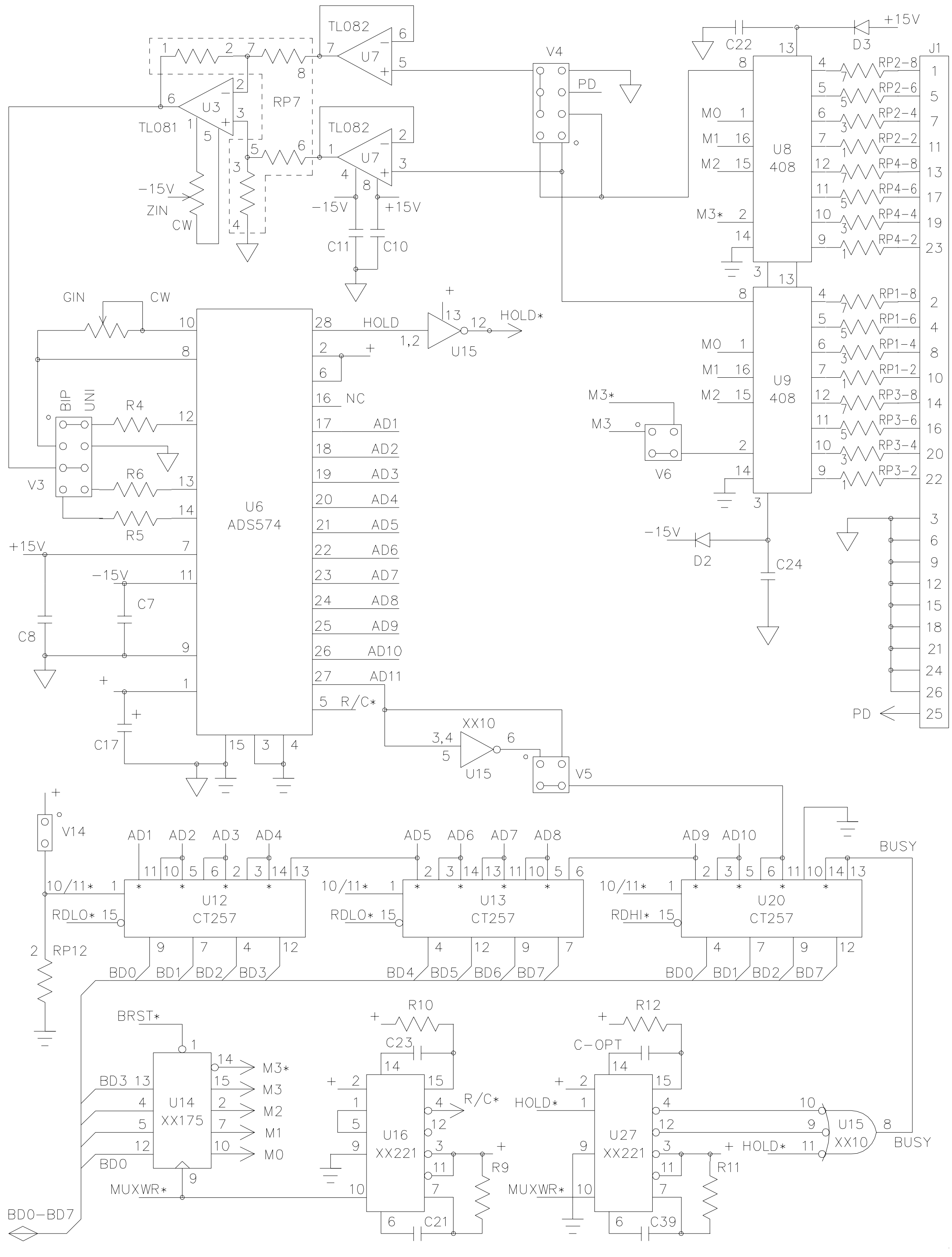
Figure 7-15. VL-1225 parts Placement Diagram

VL-1225 Schematic



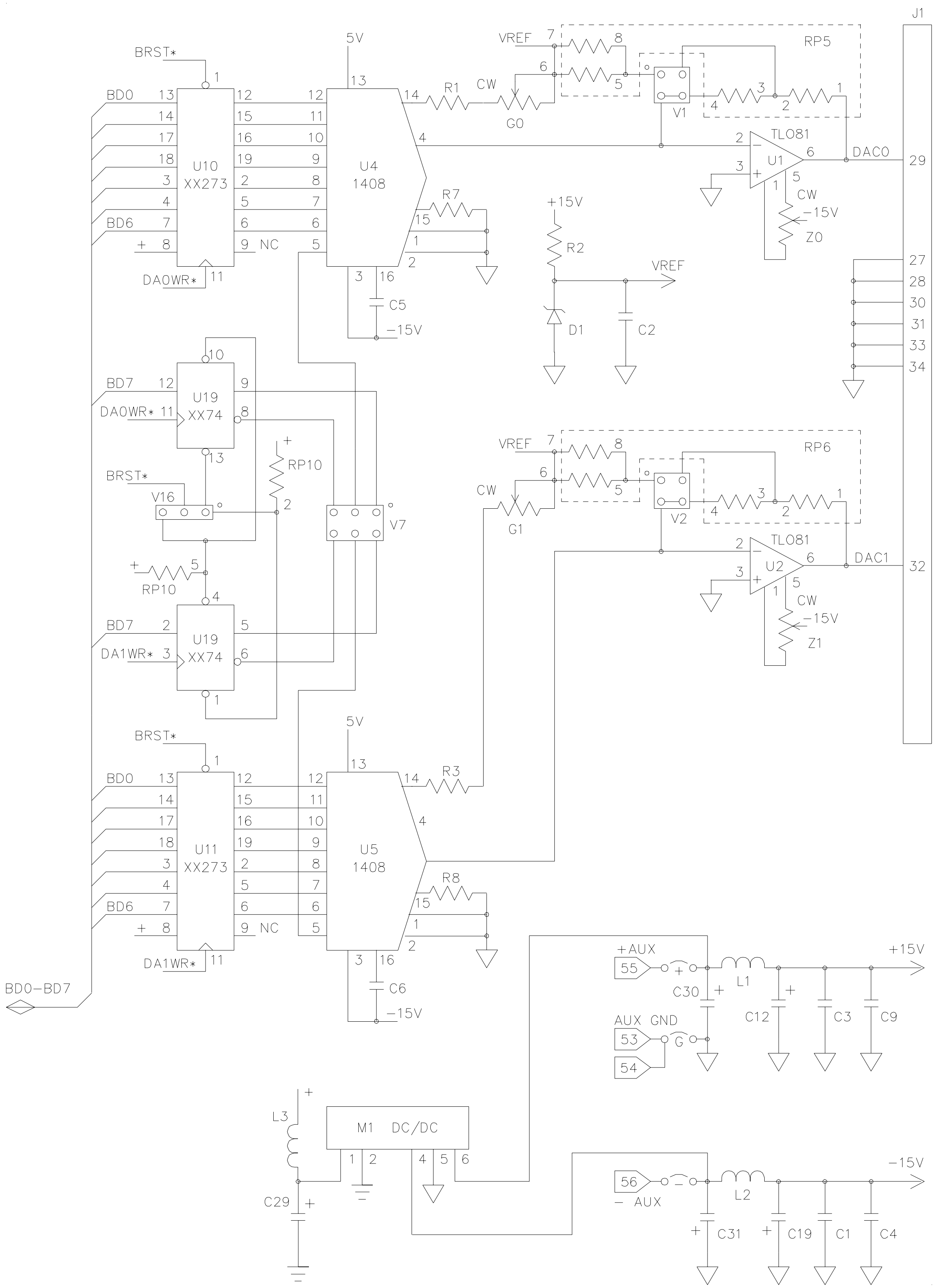
03/09/93 REV3

VL-1225 Schematic



03/09/93 REV3

VL-1225 Schematic



03/09/93 REV3

VL-1225 Parts List

Rev. 3.03

Capacitors

C1-C4,C7-C12,C13-C16,C18-C20	
C22,C24,C25-C28,C30-C38	.1 µf Z5U
C5,C6,C21,C23,C39	270 pf NPO
C17	10 µf, 16V tantalum
C29	100 µf 6.3V Elect., radial
C40	22 µf 25V Elect., radial

Inductors

L1,L2	10 µH, 250 mA
L3	47 µH, 190 mA

Integrated Circuits

U1,U2,U3	TL081CP
U4,U5	MC1408-8
U6	ADS574J
U7	TL082CP
U8,U9	DG408
U10,11	74HCT273
U12,U13,U20	74HCT257
U14	74HCT175
U15	74LS10
U16,U27	74LS221
U17,U18	74LS138
U19,U25	74HCT74
U21	74ACT245
U22,U23	74HCT688
U24	74LS367
U26	74ACT125

Resistors

R1,R3,R7,R8	2.2K Ω, 5%, ¼W
R2	3.3K Ω, 5%, ¼W
R4,R6	49.9 Ω, 1%, ¼W
R5	100 Ω, 1%, ¼W
R9	82K Ω, 5%, ¼W
R10	10K Ω, 1%,¼W
R11	100K Ω, 5%, ¼W
R12	66.5K Ω, 1%,¼W
G0,GI,GIN	500 Ω pot
Z0,Z1,ZIN	100K Ω pot
RP1-RP4	1K Ω, 4 resistor SIP
RP5-RP7	10K Ω, 4 resistor SIP, 1%
RP8-RP10	10K Ω, 7 resistor SIP
RP11,RP12	10K Ω, 5 resistor SIP

Semiconductors

D1	LM336Z-2.5
D2,D3	1N4148

Miscellaneous

M1	+5V to ±15V DC/DC (HPR105)
J1	34 pin R/A header
U1,U2	8 pin DIP socket
U8,U9	16 pin DIP socket
U6	28 pin DIP socket
V1,V2,V5,V6	2 x 2 pin straight header
V3,V4,V13,V15	2 x 4 pin straight header
V8,V10,V16	1 x 3 pin straight header
V9	2 x 6 pin straight header
V7,V11	2 x 3 pin straight header
V12	2 x 5 pin straight header
V14	2 x 1 pin straight header

VL-1226 Parts Placement Diagram

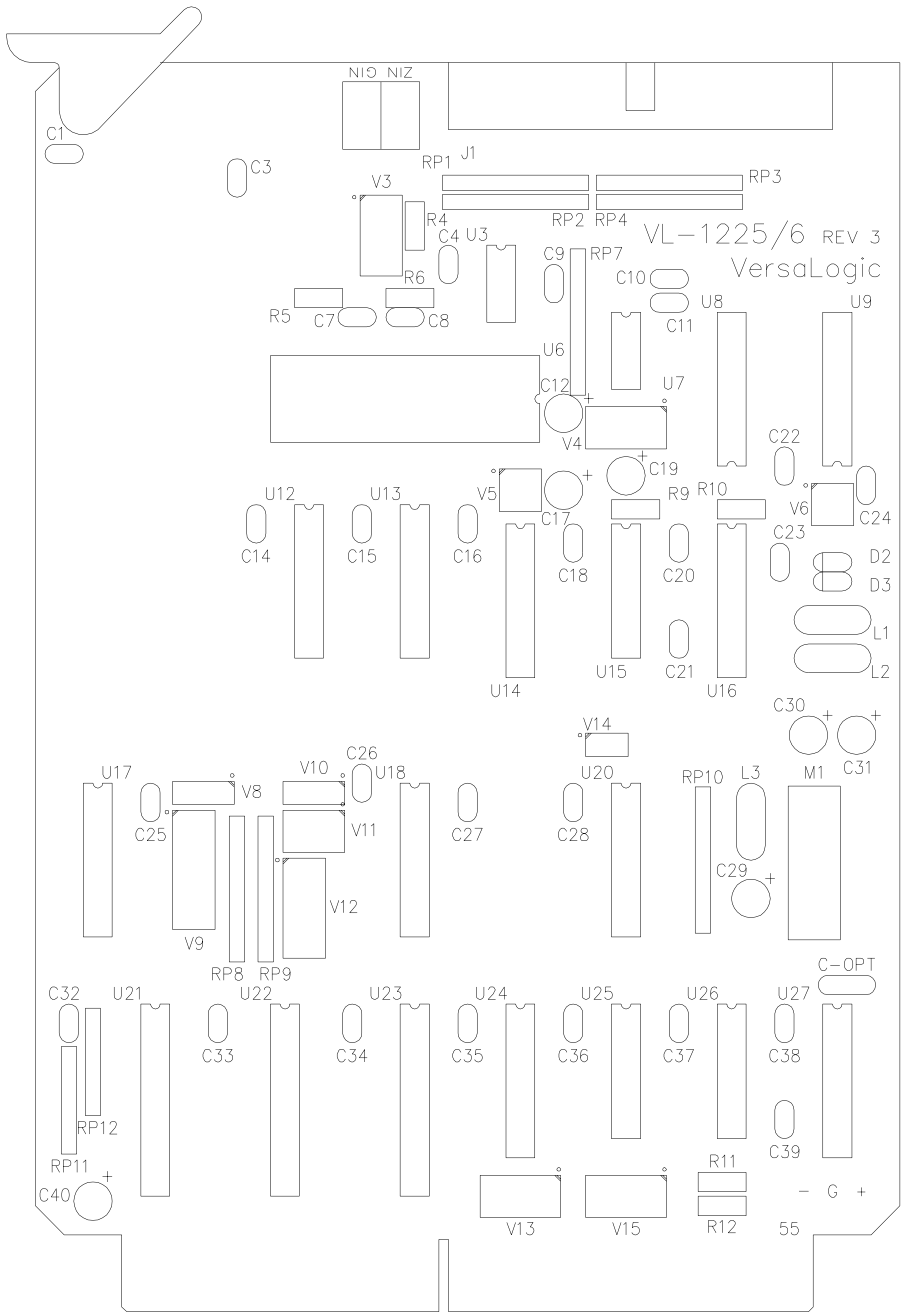
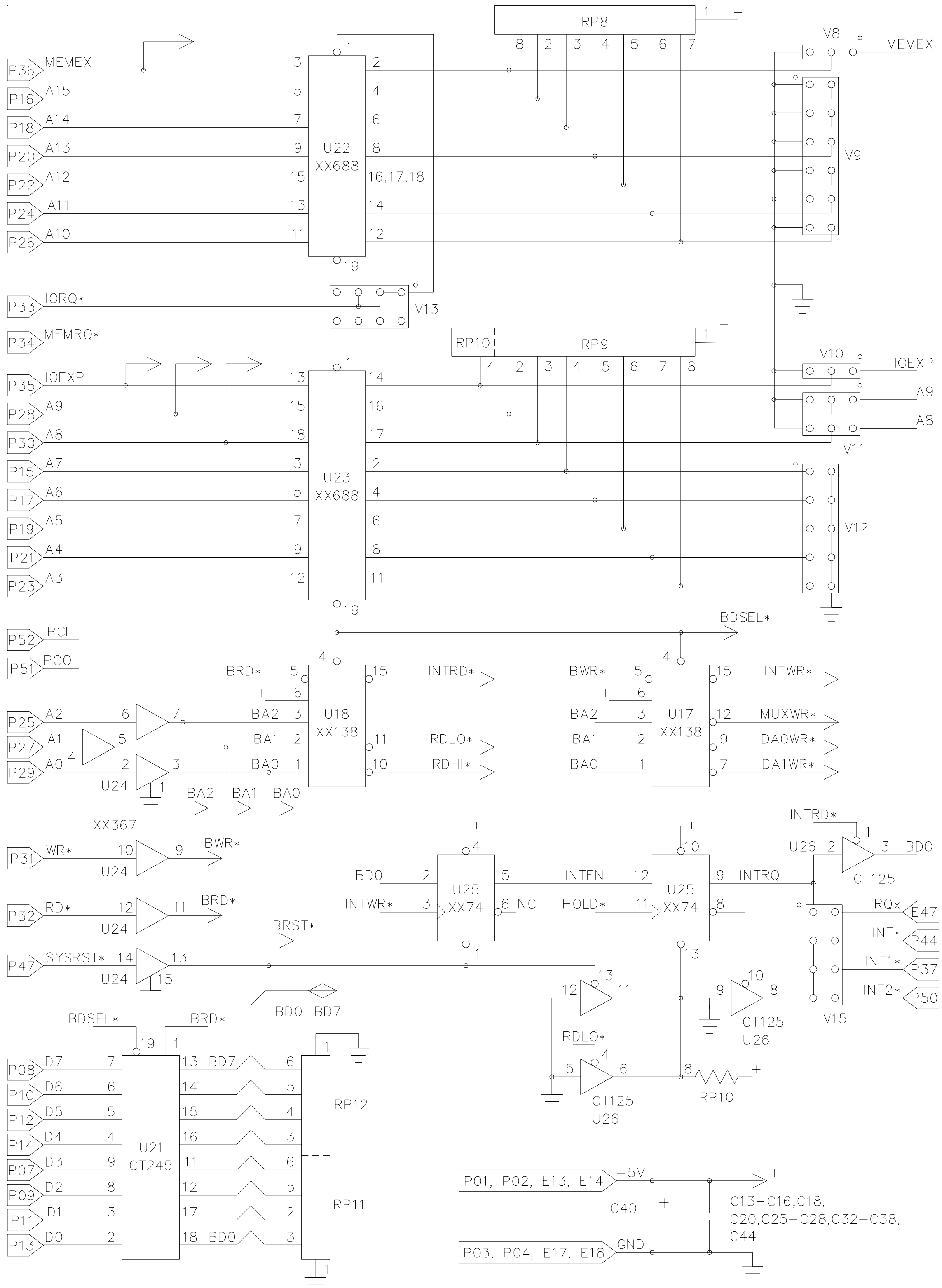


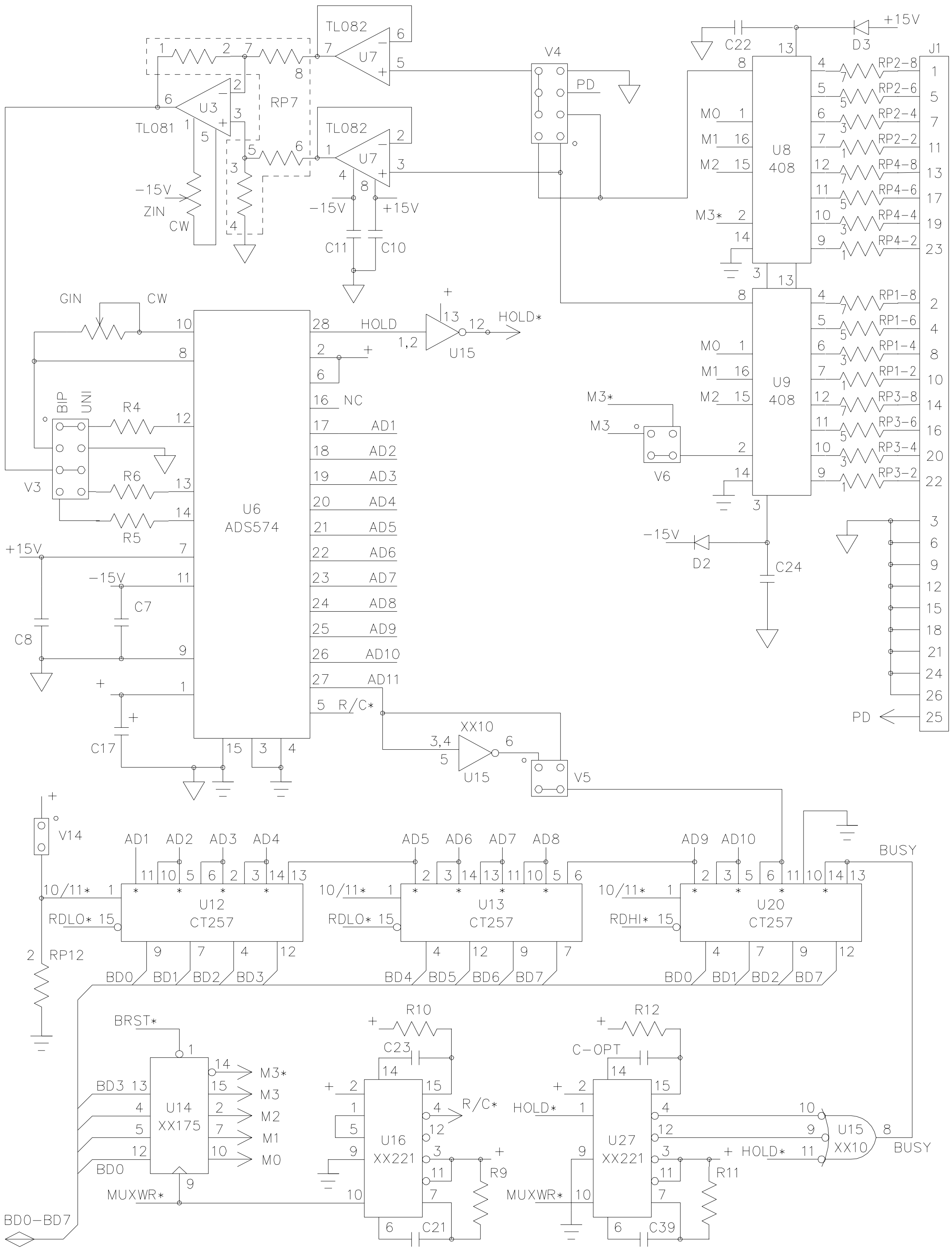
Figure 7-16. VL-1226 parts Placement Diagram

VL-1226 Schematic



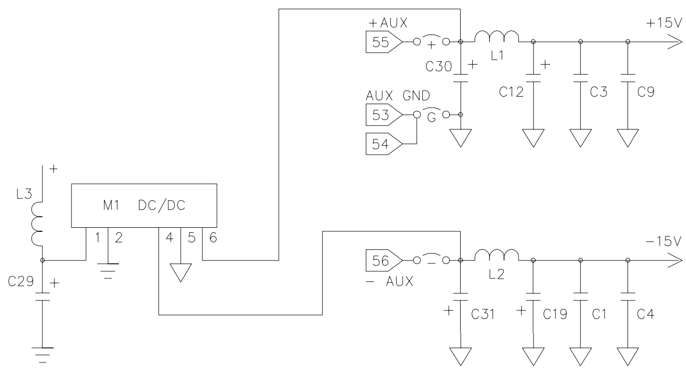
03/09/93 REV3

VL-1226 Schematic



03/09/93 REV3

VL-1226 Schematic



03/09/93 REV3

VL-1226 Parts List

Rev. 3.03

Capacitors

C1,C3,C4,C7-C12,C14-C16,C18-C20	
C22,C24,C25-C28,C30-C38	.1 µf Z5U
C21,C23,C39	270 pf NPO
C17	10 µf, 16V tantalµm
C29	100 µf, 6.3V electrolytic
C40	22 µf 25V electrolytic

Inductors

L1,L2	10 µH, 250 mA
L3	47 µH, 190 mA

Integrated Circuits

U3	TL081CP
U6	ADS574J
U7	TL082CP
U8,U9	DG408
U12,U13,U20	74HCT257
U14	74HCT175
U15	74LS10
U16,U27	74LS221
U17,U18	74LS138
U25	74HCT74
U21	74ACT245
U22,U23	74HCT688
U24	74LS367
U26	74ACT125

Resistors

R4,R6	49.9 Ω, 1%, ¼W
R5	100 Ω, 1%, ¼W
R9	82K Ω, 5%, ¼W
R10	10K Ω, 1%,¼W
R11	100K Ω, 5%, ¼W
R12	66.5K Ω, 1%,¼W
GIN	500 Ω pot
ZIN	100K Ω pot
RP1-RP4	1K Ω, 4 resistor SIP
RP7	10K Ω, 4 resistor SIP, 1%
RP8-RP10	10K Ω, 7 resistor SIP
RP11,RP12	10K Ω, 5 resistor SIP

Semiconductors

D2,D3	1N4148

Miscellaneous

M1	+5V to ±15V DC/DC (HPR105)
J1	34 pin R/A header
U8,U9	16 pin DIP socket
U6	28 pin DIP socket
V5,V6	2 x 2 pin straight header
V3,V4,V13,V15	2 x 4 pin straight header
V8,V10	1 x 3 pin straight header
V9	2 x 6 pin straight header
V11	2 x 3 pin straight header
V12	2 x 5 pin straight header
V14	2 x 1 pin straight header